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BATTERYLESS RF TRANSCEIVER FOR WIRELESS SENSOR NETWORKS

Ph.D. Thesis

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To my mother

Table of Contents

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Giuseppe Papotto

Abstract

Wireless sensor network (WSN) is a fast growing research area which has attracted considerable attentions both in industrial and academic environments in the last few years. The recent technological advances in the development of low-cost sensor devices, equipped with wireless communication interfaces, open up several applications in different fields. Prototypes exist for applications such as early detection of factory equipment failure, optimization of building energy use, structural integrity monitoring, etc. Other addressable market segments are healthcare, home automation, automotive and radio frequency identification (RFID).

However, some barriers to widespread adoption of WSNs still remain. The most critical issue is related to the extension of the *battery lifetime* of sensor nodes. Indeed, conventional wireless platforms rely on internal batteries, which suffer from a limited lifetime. On the other hand, in typical WSN application scenarios, periodical battery replacement is impractical because of either the large number of deployed devices or inaccessible node placement (e.g. implanted in human body or embedded into the structures to be monitored). The need for low-cost hardware is a critical issue as well, since it affects the overall network costs. This work is aimed at drastically facing these critical issues by recourse to an innovative node concept, which is quite different from traditional architecture approaches.

In particular, in this work a RF transceiver is presented, which is conveniently lacking both the *battery* and the *frequency synthesizer* (commonly adopted to provide the LO signal to the RX and TX sections of the front-end). *Battery-less* operation is achieved by recourse to a RF energy harvesting system. It allows the nodes to collect the needed supply power from the RF carrier transmitted by a network *hub*, which also acts as a gateway for the data stream. Such solution radically solves the battery-lifetime problem, since *RF-powered* devices are ideally free of maintenance. Moreover, as above mentioned, the use of the frequency synthesizer is avoided as well. Such target is achieved by adopting a PLL-based RF front-end. Indeed, the RX section of the designed front-end is able both to recover incoming data and synthesize the TX carrier from the input RF signal. Incidentally, the adopted front-end architecture enables sparing the quartz resonator which is normally exploited as a frequency reference. This results in an highly integrated and low-complexity/low-cost transceiver solution, which is particularly suitable for WSN applications.

This dissertation is organized as follows. In chapter I, after a brief overview about WSNs and their applications, the system architecture is presented and discussed. A prototype of the proposed RF transceiver was designed and manufactured in a 90-nm CMOS technology by TSMC. The IC design is discussed in chapter II, while experimental results are reported in chapter III, then conclusions are drawn.

This project was carried out within the RFADC (Radio Frequency Advanced Design Center), a joint research group supported by the University of Catania and STMicroelectronics.

Chapter I

RF-powered transceivers for WSNs

A *sensor* is a device which is able to convert a physical quantity into an electrical signal. This signal may be passed to a measurement or processing system for storage and analysis, or used as input to some controlled process. Sensors integrated into structures, machines and the environment, coupled with an efficient delivery system of the sensed data, could provide great benefits in several application fields [1]. Several market segments can be potentially covered, including safety, environmental and structural monitoring, healthcare, radio frequency identification (RFID), automotive, home automation, etc. However, some barriers to widespread use of sensors still remain. The deployment of wired sensor networks entails significant and long term maintenance costs, limiting the number of sensors that may be deployed, thus reducing the overall system quality. On the other hand, the adoption of a wireless communication interface allows lowering the deployment costs, but the maintenance issue remains.

Indeed, sensor nodes of a wireless sensor network (WSN) typically rely on internal batteries for their operation. Unfortunately, batteries suffer from a limited lifetime, thus they need to be periodically replaced. The extension of the battery lifetime is the most critical challenge concerning the implementation of WSNs. This issue is even more crucial for all those scenarios in which periodical node battery replacement is impractical because of either a large number of devices or inaccessible node placement.

Recently several works have been addressed to the development of *autonomous* sensor nodes, which are able to derive the energy needed for their operation from the environment by exploiting an *energy harvesting system* [2]-[5]. The greatest innovation of these devices lies in the battery-free operation which enables applications that would be prohibitively expensive due to the maintenance costs. The implementation of autonomous WSNs requires both the minimization of the power consumption of the node hardware, by means of ultra-low power *IC* design, and the adoption of proper power management strategies. The most power-hungry component of a sensor node is its wireless interface. Therefore, designing low-power low-complexity transceivers is the main challenge concerning the implementation of autonomous WSNs.

This dissertation deals with the design and characterization of a battery-less transceiver for WSN applications, which includes a RF energy harvesting module, a power management unit and an ultra-low power RF front-end. In this chapter, the design challenges are discussed along with the related state-of-art solutions. Finally, the proposed solution is presented and discussed.

1.1 Wireless sensor networks

A wireless sensor network generally consists of a *base station* (or "*gateway*") which is able to communicate with a number of wireless sensors via a radio link. Data is collected at the sensor node and transmitted to the gateway. The transmitted data are then processed by the system. A block diagram of a wireless sensor node is shown in Fig. 1.1.

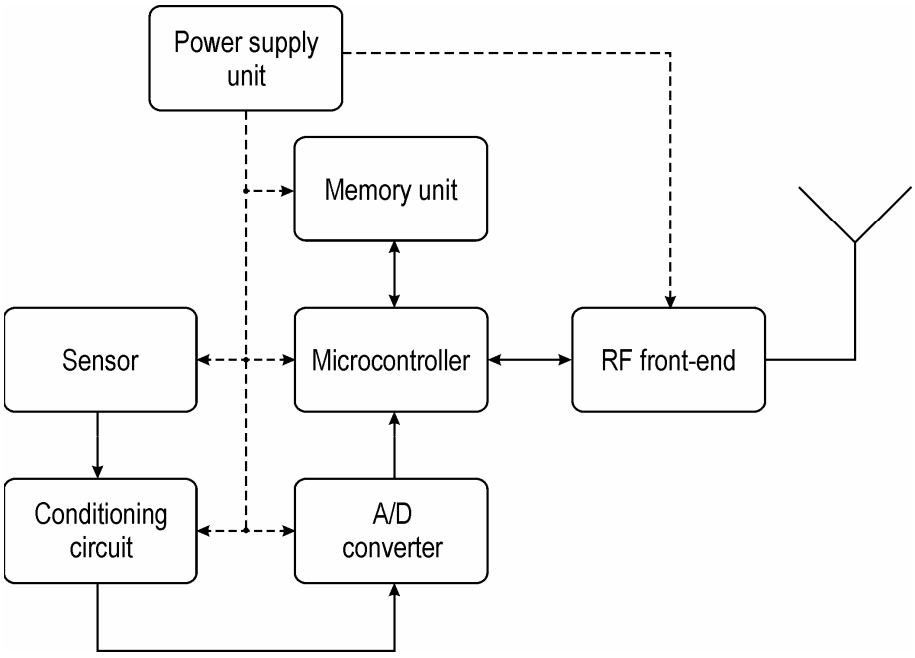


Fig. 1.1. Block diagram of a wireless sensor node.

A modular design approach is usually adopted in order to provide a flexible and versatile platform which is able to address the needs of different applications. For instance, the conditioning circuit may be programmed or replaced according to the sensing unit. The use of a memory unit allows the node to acquire data on command from the base station or when an event happens. The system is also

equipped with a microcontroller, whose main task is to manage the communication protocol.

A key issue concerning the design of a wireless sensor node is to minimize its power consumption. Generally, the radio subsystem requires the largest amount of power. Thus, it is advantageous to transmit data only when needed. Accordingly, a duty-cycled operation of the RF front-end is usually implemented. As regard the node power supply, it is worth nothing that, today batteries represent the dominant energy source. Thanks to the advances in battery technology, their energy density with respect to volume and weight (volumetric and gravimetric energy density) has increased by a factor of three in the past 15 years [6][7]. Table 1.1 shows some typical values of energy densities and self-discharge values for commercial batteries.

Table 1.1. Characteristic of batteries.

Battery type	Vol. Energy density Wh/dm^3	Grav. Energy density Wh/Kg	Self-discharge % per year
Alkaline	300	125	4
Ni-Cd	100	30-35	15-20
Ni-MH	175	50	20
Li-ion	200	90	5-10

Nevertheless, battery lifetime is a crucial issue which has up to now limited the widespread adoption of WSNs, in which there are usually dozens or hundreds of small devices to power up. To overcome such limitation, alternative solutions to batteries have been investigated. One possibility is to replace them with energy

storage systems featuring larger energy density. Concerning this, one promising technology is miniaturized fuel cells [8]. Basically, a fuel cell is a power generator that use chemical fuels (i.e. hydrogen or methanol). The gravimetric energy density of these systems is expected to be three to five times larger than Li-ion batteries. However, the maintenance issue is not solved since these cells need to be refuelled.

Recently the power supply issue has been faced by recourse to energy harvesting systems, which are able to collect the needed power from the environment (e.g. from vibrational energy, thermal energy, solar energy or RF radiation). This energy is stored in a capacitor and used to supply the whole system. Such approach enables battery-free operation allowing the deployment of potentially maintenance-free wireless sensor networks.

1.1.1 Applications

Wireless sensor network is an emerging technology with a great potential. The ability to add remote sensing points, without the cost of running wires, results in numerous benefits including energy and material savings. Several application fields may benefit from WSNs. For instance, wireless sensor network is a promising technology for medical applications. Recent years have seen the multiplication of body sensor network platforms, and a number of wireless sensor nodes for the monitoring of various biological and physiological signals ca be found [9]. These sensor nodes differ by form factor, autonomy, and their building blocks, but they all face the same technological challenges such as autonomy, functionality and manufacturing costs.

A leading sector concerning the development of wireless sensor networks is the automotive one. More and more sensors will be placed in the future cars. Tire pressure monitoring systems (TPMSs) are examples of WSNs used for safety [10]. Today such systems are powered by relatively large batteries, which limit both data transmission frequency and the system lifetime.

Fig. 1.2. Tire pressure monitoring system.

To overcome such limitations, the next-generation TPMS should be powered by energy harvesting systems. Structural monitoring is another important application field of WSNs. Sensors embedded into machines and structures enable condition-based maintenance of these assets. Typically, structures or machines are inspected at regular time intervals, and components are repaired or replaced based on their hours in service or on their working conditions. However, this approach is expensive if the components are in good working order or if a damage occurs

between two inspection intervals. Thanks to wireless sensing assets may be inspected when it is needed, reducing maintenance costs and preventing possible catastrophic failures. As regards the structural monitoring, one of the most recent applications of WSNs is related to the monitoring of large civil infrastructures, such us the Ben Franklin Bridge (Fig. 1.3).

Fig. 1.3. Ben Franklin Bridge.

The strain suffered by this structure is monitored by a network of wireless sensors powered by lithium batteries, which are able to provide more than one year of continuous operation [1].

Other application fields are home automation (WSNs are keys building blocks for smart homes), environmental monitoring (random deployment on large-scale areas makes monitoring of agriculture easier) industrial automation (WSNs may replace traditional cabling in monitoring and control systems), assets tracking (radio frequency identification tags may be placed onto or into objects

and products to perform remote identification and tracking by means of radio waves) [11].

1.2 Energy harvesting systems

Energy harvesting systems can be grouped into three categories according to the type of energy they use, which may be kinetic, thermal or electromagnetic energy (including both solar and RF radiation).

Kinetic energy is converted to electrical energy by exploiting the displacement of a moving part or the mechanical deformation of some structures inside the energy harvesting module. For converting this displacement or deformation the established transduction mechanisms are electrostatic, piezoelectric or electromagnetic. In electrostatic transducers, the distance or overlap of two electrodes of a polarized capacitor changes due to the movement or the vibration of a movable electrode. This motion produces a voltage change across the capacitor and results in a current flow in an external circuit. In piezoelectric transducers, vibrations cause the deformation of a piezoelectric structure, which generates a voltage proportional to the applied strain. In electromagnetic transducers, the relative motion of a magnetic mass with respect to a coil causes a change in the magnetic flux that generates an AC voltage across the coil [12]. For a given vibrational energy source, the highest power output is achieved by piezoelectric conversion. Recent advances in *MEMS* technology allow piezoelectric-based energy harvesting systems to be miniaturized (Fig. 1.4) opening up their adoption by WSNs [13][14].

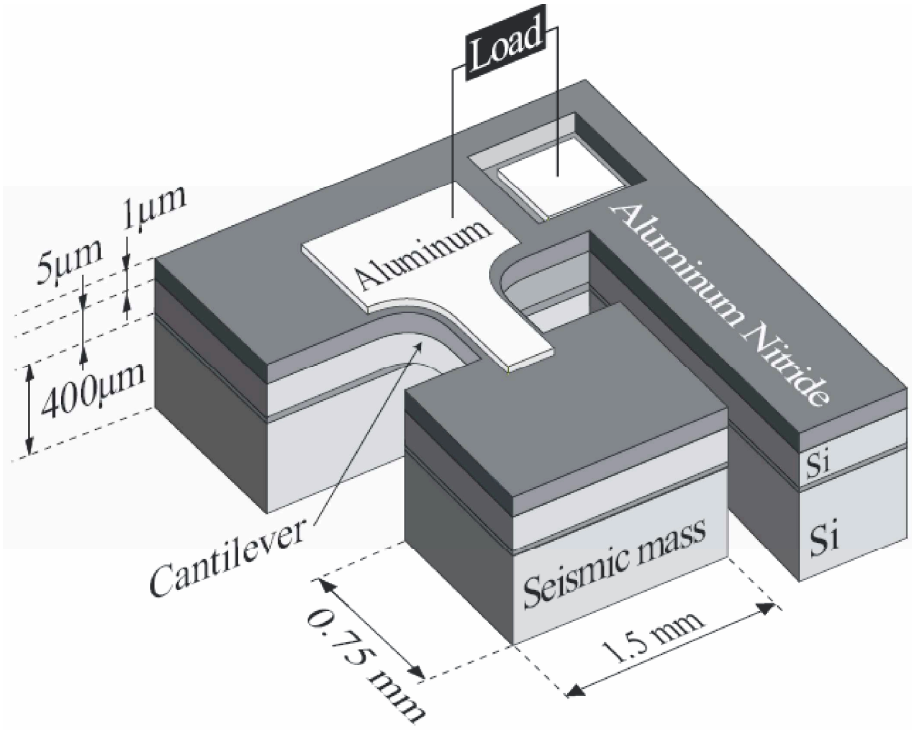


Fig. 1.4. Schematic of a piezoelectric micro-power generator [14].

However, such systems, which are particularly suitable in industrial environments (where a large amount of vibrational energy is present), may prove ineffective for other applications, such as home automation or structural and environmental monitoring. Thermal energy harvesting devices may use the thermal energy coming from different environmental sources: persons, animals, machines. A thermoelectric generator basically consists of a *thermocouple*, comprising a p-type and n-type semiconductor connected electrically in series and thermally in parallel. The *thermogenerator* (based on the Seebeck effect) provides an electrical current proportional to the temperature difference between its hot and cold junctions. An electrical load is then connected in series with the thermogenerator creating an electric circuit [12]. The most widely used material for the fabrication of thermoelectric generators operating at room temperature is

Bi_2Te_3. Poly-SiGe has also been used, especially for micro-machined thermopiles [15]. Moreover, research on nano-structured materials is ongoing worldwide in order to optimize thermoelectric generator performance.

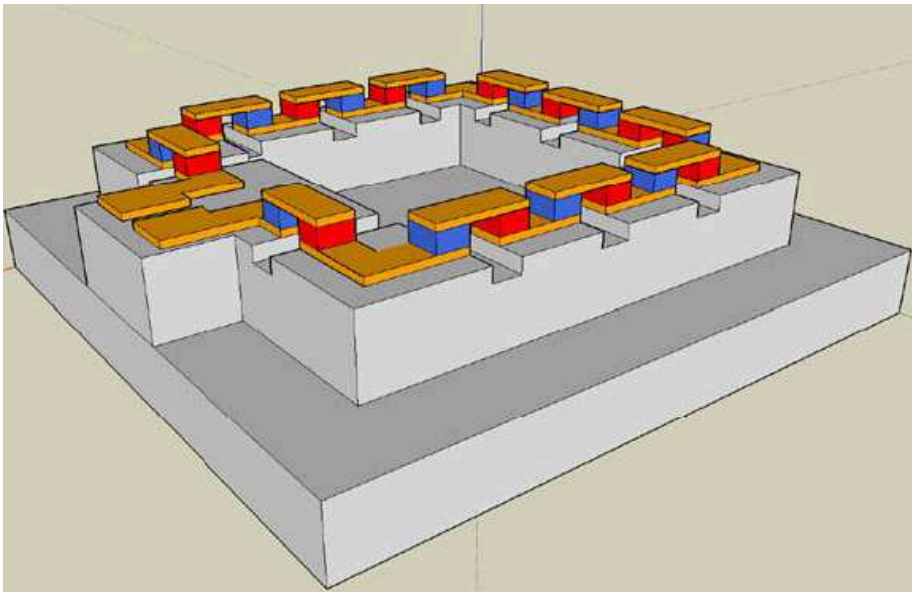


Fig. 1.5. Micro-machined thermopile [15].

Another energy source which is profitably used to perform energy harvesting is the electromagnetic radiation, either in the form of *light* (known as solar energy), or *lower frequency* RF radiation. Both methods are extensively used in many present devices.

Solar energy is a mature technology. Photovoltaic systems are found from the megawatt to the milliwatt range producing electricity for a wide range of applications. Outdoor they are a viable energy source for self-powered systems. Indoor the illumination levels are much lower (10-100 $\mu W/cm^2$), which requires a fine-tuning of the cell design to the different spectral composition of the light and the lower level of illumination. The described energy harvesting systems share the

common limitation of being reliant on ambient sources generally beyond their control.

RF energy harvesting systems overcome such limitation [16]. Indeed, RF power can be easily provided when needed, in every location. To this aim, RF harvesting systems rely on a RFID-like approach, in which power is delivered to passive tags through the radio waves transmitted by a reader. This solution gives great flexibility to the system. RF-powered devices can be located in inaccessible or hazardous areas, or locations where battery replacement is highly impractical. For this reason, a RF-powered approach was chosen as the best solution for the design of a *battery-free transceiver* for wireless sensor network applications. A description of the main features of a RF-powered sensor network is provided in the next section.

1.3 RF-powered sensor networks

RF-powered devices provide an enabling technology for the deployment of low-cost wireless sensor networks. Such devices rely on the extraction of energy from propagating radio waves instead of internal power sources. Today, RF-powered devices are widely used in passive radio frequency identification (RFID) systems. Furthermore, many biomedical implanted equipments exploit radio waves to extend their lifetime. Possible applications also include telemetry systems, structural monitoring, and home automation. As shown in Fig. 1.6 RF-powered sensor network architectures rely on the use of a central *hub*, which is able to provide the nodes with both the needed supply power and the reference

frequency through a RF carrier, besides operating as a gateway for the data stream.

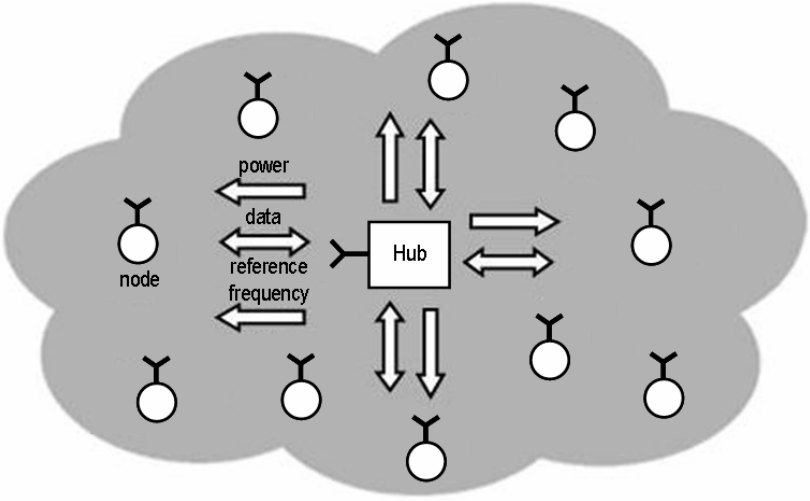


Fig. 1.6. RF-powered sensor network.

Adopting such network concept radically solves the problem of battery lifetime, since RF-powered nodes are ideally free of maintenance.

1.3.1 Frequency bands

Low-power RF devices, such as wireless sensor nodes, usually operate within unlicensed bands, which are often referred to as ISM bands. These are portions of the frequency spectrum reserved internationally for the use of radio frequency waves for industrial, scientific and medical purposes. Unlicensed means that the user of these products doesn't need for an individual license from the telecommunication regulatory authorities, but it doesn't mean unregulated. On the contrary, wireless devices need to meet strict regulations on the operating frequencies, output power, spurious emissions, among other things.The ISM

bands are defined by the ITU-R (International Telecommunication Union Radiocommunication Sector), which is responsible for the development of standards for radio-communication systems. The designed bands are listed in Table 1.2 [17].

Table 1.2. ISM frequency bands.

Frequency range	Center frequency
6.765-6.795 MHz	6.78 MHz
13.553-13.567 MHz	13.56 MHz
26.957-27.283 MHz	27.12 MHz
40.66-40.7 MHz	40.68 MHz
433.05-434.79 MHz	433.92 MHz
902-928 MHz	915 MHz
2.4-2.5 GHz	2.45 GHz
5.725-5.875 GHz	5.8 GHz
24-24.25 GHz	24.125 GHz
61-61.5 GHz	61.25 Ghz
122-123 GHz	122.5 GHz
244-246 GHz	245 GHz

The individual countries' use of these bands may differ due to variations in national radio regulations.

1.3.2 Data rate

The communication requirements of WSNs are quite different from those of traditional wireless links. For instance, in WLAN networks, data are transmitted at a rate as high as possible. Similarly, in mobile phone networks, data rate must be high enough to ensure a good quality of service (QoS). In contrast, in WSNs, data traffic is limited to prevent flooding of the hub with raw data and to save energy.

To this aim, duty-cycled operation schemes are usually adopted at the node level in order to reduce as much as possible the use of the wireless interface, which is the most power-hungry component of a wireless sensor node. Moreover, an investigation of the data flow in WSNs reveals that the operation of wireless sensor nodes is usually event-driven, namely data transmission occurs only when the monitored physical quantity changes or a request from the hub is received. On the other hand, in most application scenarios, slowly variable phenomena are monitored. Therefore, each node transmits a few packets/second. Moreover these packets are relatively short (typically less than 200 bits/packet). As a result, the average data rate of each wireless sensor node usually doesn't exceed 1 Kbps [18].

1.3.3 Operating range

A key parameter of a wireless sensor network is the operating range, i.e. the maximum allowed distance between the hub and the sensor node. In most application scenarios an operating range of about 10 m is required.

In a RF-powered sensor network, two conditions must be fulfilled to ensure communication between the hub and each sensor node. First, the available input power at the antenna connector of the node must be sufficient to guarantee proper operation of its equipment. As a matter of fact, RF-powered devices rely on the extraction of the needed DC power from the radio waves transmitted by the hub. Furthermore, the signal transmitted by the node must be sufficiently strong when it reaches the hub, so that it can be received without errors. Traditionally, RF-powered devices (such as. passive RFID tags) are *downlink* (hub to node path)

limited, namely the system operating range is limited by the power that the device can harvest from the radio waves transmitted by the hub. However, such systems use a backscattering-based transmission scheme for the *uplink* communication (from node to hub). According to this approach, sensor nodes should transmit data to the hub in a passive way, by simply reflecting the incident RF power coming from the hub. In this case, the hub sensitivity plays an important role in the definition of the system operating range [19]. Indeed, in a RF-powered network architecture, the transmitter of the hub must be permanently on to ensure proper operation of the network nodes. Therefore, it induces a significant amount of noise to the receiver input of the hub itself, lowering the signal to noise ratio (SNR). This problem, which is referred to as *self-jamming*, is even more relevant considering that the backscattered signal lies in the same band of the signal transmitted by the hub. In this case, the node's signal should lie no more than 100 dB below the level of the hub's carrier signal to be correctly received [20]. As increasingly efficient RF energy harvesting systems are being introduced, the downlink operating range progressively extends and the uplink power budget turns out to be the bottleneck of the backscattering-based systems.

1.4 RF-powered transceiver

The main challenge in the implementation of a RF-powered sensor network is to design an ultra-low power RF transceiver, which is able both to efficiently harvest the power needed for the node operation and to perform the communication task. Several works have been reported in literature about this

topic. A first proposed approach basically relies on a RFID-like platform equipped with an ASK demodulator and a backscattering-based transmitter [21][22]. Such solution ensures low power consumption, since most part of the system is passive. Combining low-power ICs with improved RF energy harvesting systems allows extending the downlink operating range. On the other hand, as above explained, backscattering-based systems suffer from the hub self-jamming, which limits the uplink operating range.

To overcome such limitation, RF-powered transceivers have been proposed which exploit an active transmission scheme. RF-powered transceivers equipped with UWB transmitters are presented in [23]-[25]. These devices are remotely powered through an UHF signal, which is also used to perform the downlink communication. Conversely, an UWB transmission scheme is used for the uplink communication with the aim of achieving both high data rates and low current consumption through very simple (crystal-less) circuit architectures at the sensor node side. However, adopting an UWB transmission approach considerably challenges the receiver section of the hub, thus potentially resulting in a net increase of the overall system complexity [18].

Batteryless telemetry nodes with narrowband active transmission have also been demonstrated in [26] and [27]. Nevertheless, these circuits are not suitable for advanced communication functionalities (e.g., tag addressing, polling or control) due to the lack of a proper receiver section. In this work the design and characterization of a RF-powered transceiver for WSNs is presented. It includes a fully functional receiver and exploits a narrowband active transmission to improve

the uplink operating range without burdening the hub complexity. A description of the proposed solution is given in the following section.

1.4.1 Proposed solution

The implementation of a RF-powered sensor network entails some non-trivial tasks to be accomplished, namely the efficient extraction and management of the DC power from the incoming RF carrier, the reconstruction of the reference frequency, the design of ultra-low power circuits for the RF-front end. The need for low-complexity low-cost node implementations is a critical issue as well. Such tasks have been addressed by using the node architecture sketched in Fig. 1.7.

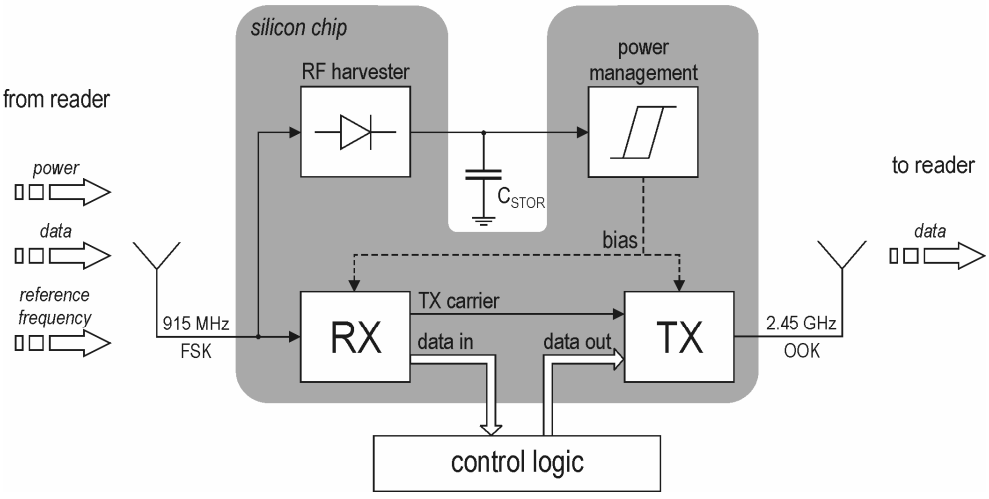


Fig. 1.7. Block diagram of the proposed batteryless RF transceiver.

The system receives a FSK-modulated carrier from the hub through the ISM-band 915-MHz antenna. Incident power is fed to the input of a RF energy harvester implementing a RF-DC conversion. Scavenged DC power is

accumulated in a storage capacitor and then used to supply the whole system through a power management unit. The incoming RF signal is also processed by a dedicated receiver, which is able to derive both data and reference frequency from the modulated carrier. The extracted carrier is then exploited by the TX section of the RF front-end operating in OOK mode in the 2.45-GHz ISM band. Of course, active transmission requires a relevant energy budget for the transceiver, which is easily accomplished by adopting a convenient power management strategy based on a discontinuous operation of the RF front-end.

The proposed architecture offers several benefits. It allows performing the communication task without requiring a *frequency synthesizer*. Incidentally, this enables sparing the quartz resonator, which is normally used as frequency reference. Crystal-less operation leads to the implementation of a highly integrated low-cost wireless platform. Moreover, the adoption of a constant envelop modulation scheme (FSK, as mentioned) results in improved downlink power transfer. Finally, the adopted active transmission scheme allows improving the uplink operating range. Incidentally, by decoupling the frequencies used for power and data telemetry, the receiver sensitivity requirements at the hub side may be relaxed.

A complete description of the adopted circuital solutions and the related design strategies is provided in the next chapter.

Chapter II

Batteryless RF transceiver design

In chapter I the main design challenges related to the implementation of a batteryless platform for remotely powered WSNs were identified, namely the efficient extraction and management of the needed DC power from the incoming RF signal, the reconstruction of the reference frequency and the design of ultra-low power circuits for the proposed transponder. This chapter deals with the circuital solutions and related design strategies that have been adopted to address these issues.

For the sake of clarity, the designed circuits are grouped into three functional blocks: the energy harvesting module (converting the AC power from the antenna into a non-regulated DC voltage), the power management circuit, and the RF front-end (comprising both receive and transmit functions).

The system was designed in a 90-nm CMOS technology by TSMC. Simulations were performed in Spectre circuit simulator within Cadence CAD environment.

2.1 RF harvesting module

As explained in chapter I, remotely powered devices rely on the extraction of the needed DC power from the radio waves transmitted by an hub or base station, which also acts as a gateway for the data stream. As the hub radiates power, each sensor node starts harvesting the DC power, which is accumulated in a storage capacitor and used to supply the whole system through a power management unit. The RF-to-DC power conversion is performed through an energy harvesting module. Fig. 2.1 shows the simplified block diagram of a RF energy harvesting system, which generally consists of an antenna to pick up the power transmitted by the hub, an impedance matching network to perform a passive amplification of the input voltage and a rectifier circuit which implements the RF-to-DC conversion.

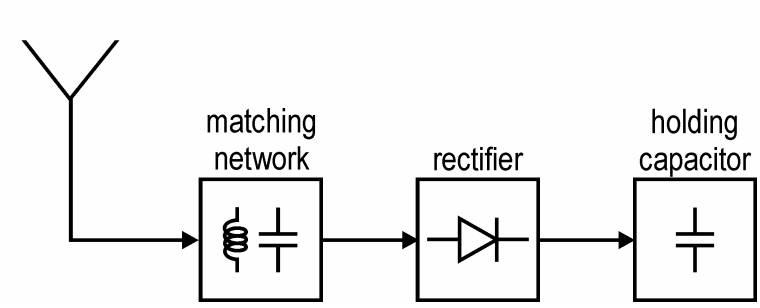


Fig. 2.1. Block diagram of a RF energy harvesting system.

Most conveniently, the industrial, scientific, and medical (ISM) band at 902-928 MHz can be exploited for RF energy harvesting. Indeed, in this frequency range, a high 4-W effective isotropic radiated power (EIRP) is allowed by regulatory bodies [28] and the radiated power experiences a lower *path loss*

with respect to higher frequency band (e.g. 2.45-GHz band), resulting in an extended node distance from the hub.

According to the Fiis equation [20] for free-space propagation, the available power at the antenna connector is:

$$P_{S,AV} = P_{EIRP}\, G_{RX} \left(\frac{\lambda}{4\pi\, d} \right)^2 \tag{2.1}$$

where P_{EIRP} is the transmitter EIRP, G_{RX} is the receiver antenna gain, λ is the wavelength, and d is the link distance. Therefore, the available power at each sensor node decreases by 6 dB for every doubling of distance from the radiating source. This issue is even more critical as multi-path fading comes into play as typical for indoor scenarios, where power drop off at a much faster rate than $1/d^2$. Indeed, in such conditions, the standard ITU propagation model [29] estimates a decrease rate roughly proportional to $1/d^3$, resulting in a μW-level power budget for remote RF-powered network nodes.

In such a scenario, it is mandatory that the input power threshold of the RF energy harvesting module be as low as possible in order to maximize the network coverage area.

Since a RF harvester basically consists of a multi-stage rectifier, its sensitivity, i.e. the minimum incident power that the circuit is able to convert into DC, is primarily set by the threshold voltage of the rectifying devices (diodes or transistors). To overcome such limitation, several low-threshold schemes have been proposed [26],[30]-[35] either relying on technology solutions or based on proper compensation circuits. Although effective, such solutions are unsuitable

for batteryless platforms. Therefore, a novel CMOS RF energy harvester was designed, which is based on an improved fully-passive multi-stage rectifier for efficient AC-DC conversion. The issue of threshold voltage compensation was successfully addressed by a simple yet effective topology arrangement, which guarantees improved performance compared to prior art solutions, without requiring any additional *ad hoc* circuitry.

Moreover, a design methodology was developed which allows an optimum trade-off among matching losses, power reflection, and rectifier's efficiency to be achieved.

2.1.1 Multi-stage rectifiers for RF harvesting systems

Traditionally, CMOS multi-stage rectifiers are implemented exploiting the Dickson's topology [36], which relies on the use of diode-connected transistors as pumping devices. Such common precursor is shown in Fig. 2.2 (NMOS version), with its DC input grounded as required in fully passive harvesting applications.

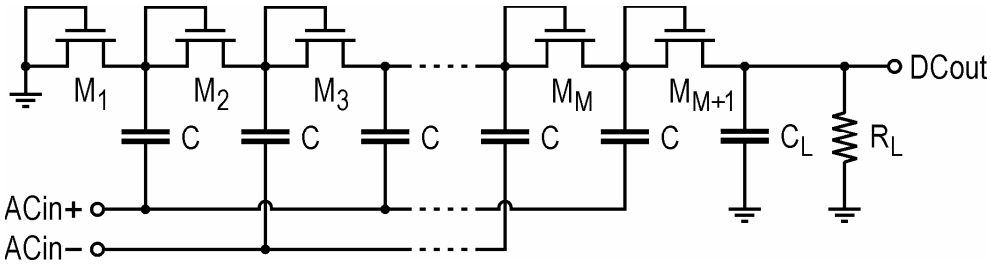


Fig. 2.2. Schematic of a conventional Dickson multi-stage rectifier.

The performance of such a circuit is mainly limited by the threshold voltage of the pumping devices, which reduces the AC-DC conversion efficiency and sets

a minimum input voltage needed to turn the circuit on. Indeed, the DC output voltage of a Dickson rectifier with *M + 1* pumping devices can be expressed as:

$$V_{O} = M\left(\frac{C}{C+C_{P}}V_{AC} - \frac{I_{O}}{f(C+C_{P})} - V_{TH}\right) - V_{TH} \tag{2.2}$$

where V_{AC} is the peak-to-peak voltage of the AC input signals, C is the coupling capacitor, C_P is the parasitic capacitance at each pumping node (not shown in Fig. 2.2), I_O is the average current drawn by the output load, f is the operating frequency, and V_{TH} is the transistors' threshold voltage.

According to (2.2), the following condition is to be satisfied for a proper operation of the Dickson circuit:

$$V_{AC} > \frac{C+C_{P}}{C}\frac{M+1}{M}V_{TH} + \frac{I_{O}}{f\,C} \tag{2.3}$$

Therefore, even with negligible output currents, a minimum AC input voltage level must be guaranteed, such level being higher for larger V_{TH} values. This results in an input power threshold, which characterizes the well-known "dead zone" of voltage rectifiers.

The problem of rectifiers' dead zone can be faced by recourse to specific technology options providing the designer with low-voltage pumping devices. For instance, Schottky diodes and zero-V_{TH} transistors are exploited as rectifying components in [30] and [33], respectively. However, the use of non-standard technology options entails higher production costs. On the other hand, low-V_{TH} transistors are commonly available in standard CMOS processes and can be used

to the same purpose [26], though attaining a comparatively lower performance in terms of dead zone compensation.

As an alternative to technology-based approaches, smart circuit solutions can be exploited to compensate the rectifying devices' threshold voltage. Such compensation can be ideally performed by supplying a static bias offset V_C between the gate and drain terminals of each transistors of the pumping chain, as displayed in Fig. 2.3. Note that, hereafter the "drain" and "source" terminals of a transistor are identified by reference to its conduction phase.

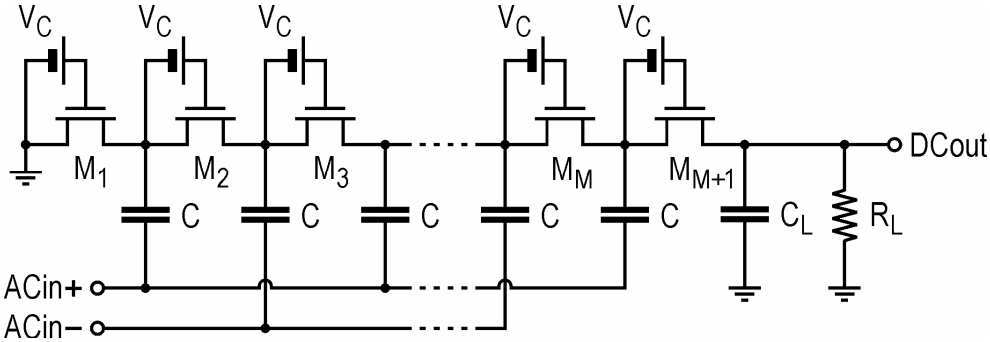


Fig. 2.3. Concept representation of a Dickson rectifier with compensation of the threshold voltage.

This arrangement has the same effect of a net reduction of the transistors' threshold voltage, thus improving the rectifier performance. Several circuital solutions have been proposed according to this general approach.

A threshold compensator is suggested in [31], which relies on a bias voltage generator and distributor as shown in Fig. 2.4. The voltage distributor consists of two pairs of pass transistors for each pumping device. Each couple of pass transistors is driven by control signals with opposite phase in order to provide the

rectifying devices with the desired compensation voltage without affecting the potential at the node of the pumping chain.

The voltage generator V_{bth} is implemented exploiting a diode connected NMOS transistor and a reference current, so as to generate a voltage reference equal to the rectifying devices' threshold voltage, irrespective to its absolute variation among the integrated chips (ICs).

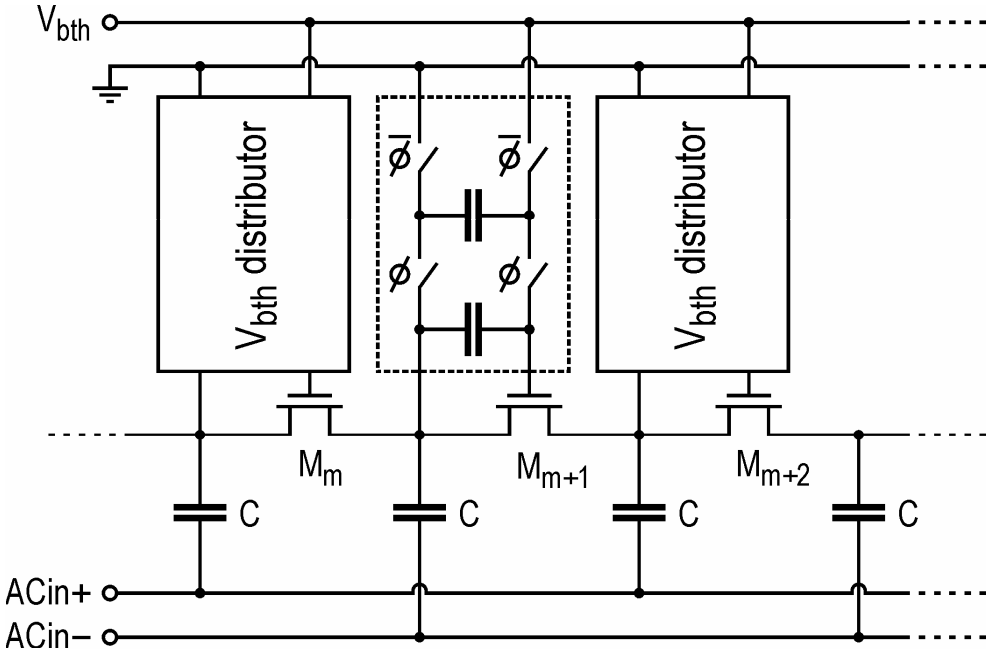


Fig. 2.4. Multi-stage rectifier with threshold compensation through voltage generator and distributor [31].

Nevertheless, this compensator calls for a secondary battery, which is exploited to generate both the needed compensation voltage and the pass transistor control signals. Being active, this compensator is unsuitable for batteryless platforms.

A rectifier exploiting a passive threshold compensator is proposed in [32]. In this solution a mirror-like configuration (Fig. 2.5) allows the desired compensation voltage to be generated by exploiting the node voltages of the rectifying circuit.

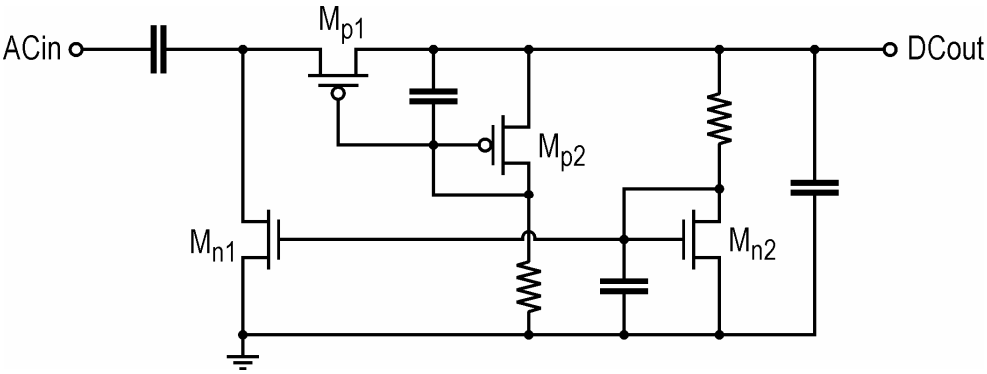


Fig. 2.5. Rectifier with passive mirror-like threshold compensator [32].

However this approach entails the use of high capacitance and resistance values, potentially resulting in a large silicon area occupation for multi-stage implementations.

Pseudo-floating-gate transistors are used in [34] to enhance rectifier performance. In a CMOS technology, floating gate devices may be designed by placing a MOS capacitor in series with the gate of the transistors. The gate of the transistor and the gate of the MOS capacitor are connected together to obtain a high impedance node, which allows charges to be trapped in the floating gate. Fixing the charge in the floating gate results in a voltage bias across the MOS capacitor, which reduces the effective threshold voltage of the transistor.

The multi-stage rectifier exploiting pseudo-floating-gate transistors as pumping devices is shown in Fig. 2.6.

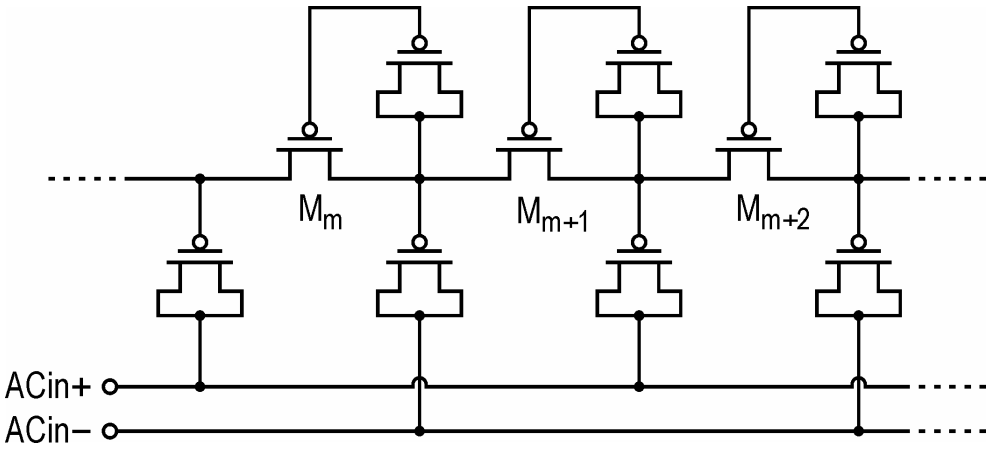


Fig. 2.6. Dickson's rectifier with pseudo-floating-gate transistors [34].

Although effective, this solution calls for an initial programming phase, needed to trap the charges in the floating gates. Basically, the charge must be injected via Fowler-Nordheim (F-N) tunnelling which requires a large sinusoidal signal to be applied to the input of the rectifier. Obviously, this makes the described solution unsuitable for batteryless platforms.

Finally, an auxiliary rectification chain is exploited in [37] (Fig. 2.7) to generate the bias offset voltages needed to compensate the threshold voltage of the transistors of the rectifying chain. Although this arrangement can effectively reduce the dead zone of a RF harvester, it should be considered that the auxiliary chain and associated coupling capacitors involve substantial increase of the circuit physical size and potentially augment power dissipation lowering the whole system efficiency.

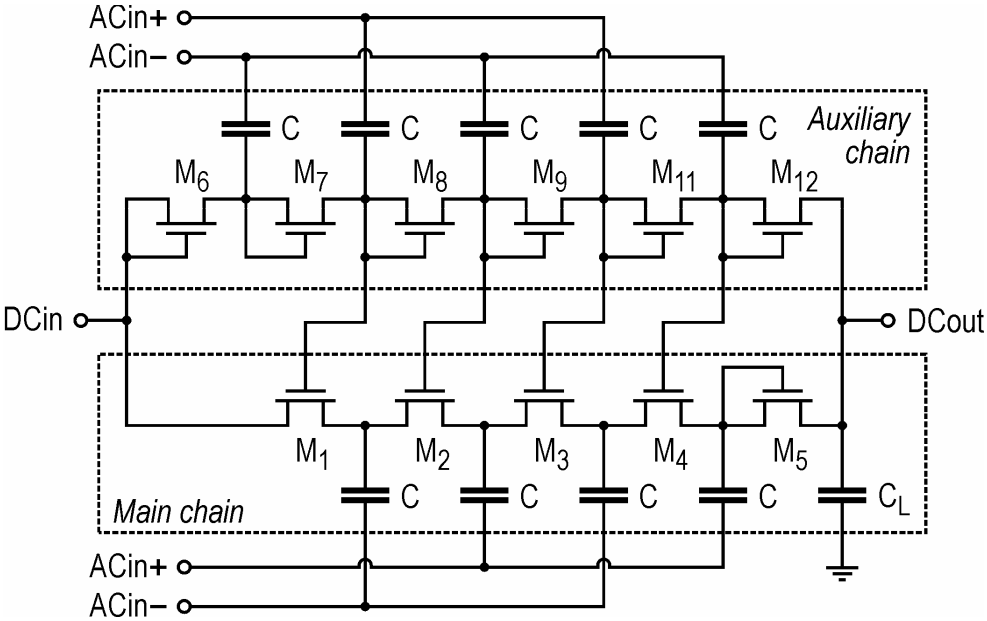


Fig. 2.7. Multi-stage rectifier with auxiliary chain for the threshold voltage compensation [37].

2.1.2 Threshold self-compensated rectifier

As shown in the previous section, state-of-art rectifiers for RF energy harvesting systems are unsuitable for batteryless platforms since they rely on either a pre-programming phase or secondary batteries to enhance the system performance. In contrast, the adopted solution allows the desired compensation to be achieved in a fully passive way.

The basic idea is to perform the desired threshold compensation by profitably exploiting the inherent properties of the voltage waveforms at the nodes of the rectifying chain. Indeed, it should be noted that such voltages have:

- equal AC amplitudes (as long as coupling capacitors C are shorted at RF),
- alternating phases,

- progressively increasing DC components from the input to the output of the rectifying chain.

The latter properties suggests that the bias offset required by each gate terminal can be found in the following nodes of the multiplication chain, rather than calling on auxiliary compensation circuitry. The simplest embodiment of such *self-compensation* concept was first disclosed in [38]. In this patent, a simple yet effective threshold compensation is achieved by merely connecting the gate of each transistor of the pumping chain to the source of the right-adjacent one instead of shorting it to the drain of the same device, as shown in Fig. 2.8.

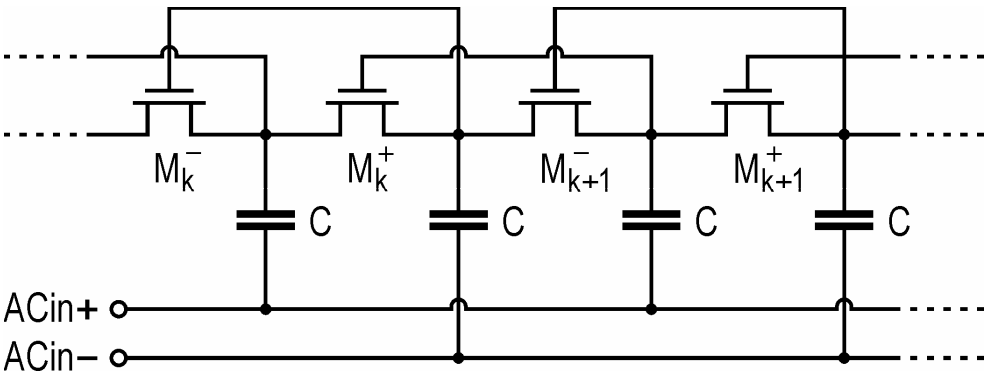


Fig. 2.8. Basic implementation of the threshold self-compensation concept [38].

However, this basic implementation may not guarantee substantial performance improvement. Indeed, it provides a bias offset V_C equal to the DC voltage increment due to each doubler stage (i.e. two adjacent rectifying devices), that is roughly V_O/N, where V_O is the rectifier output voltage and N is the number of cascaded doubler stages. Therefore, for designs with a large number of stages

and/or low nominal output voltage, the described solution may prove ineffective because of a quite modest compensation voltage (V_C).

Nevertheless, this approach can be easily generalized thus overcoming its inherent limitations. To this aim, we adopted a self-compensation methodology [39][40], which consists in further extending the length of the compensating bridges to the purpose of increasing the obtained gate bias offset. The "order" of such compensation (i.e. the length of gate connections) is to be chosen depending on the process threshold voltage and the required output voltage. According to this generalized approach the implementation reported in Fig. 2.8 can be considered as an order-2 compensation topology.

It is worth noting that, only even-order compensations are allowed because of the alternating node phases. Indeed, achieving the desired compensation requires the gate terminal of each transistor is connected to a following node of the pumping chain, whose voltage waveform is in phase with that one at the drain of the same device. Order-4 and order-6 solutions are shown in Fig. 2.9 and Fig. 2.10, respectively.

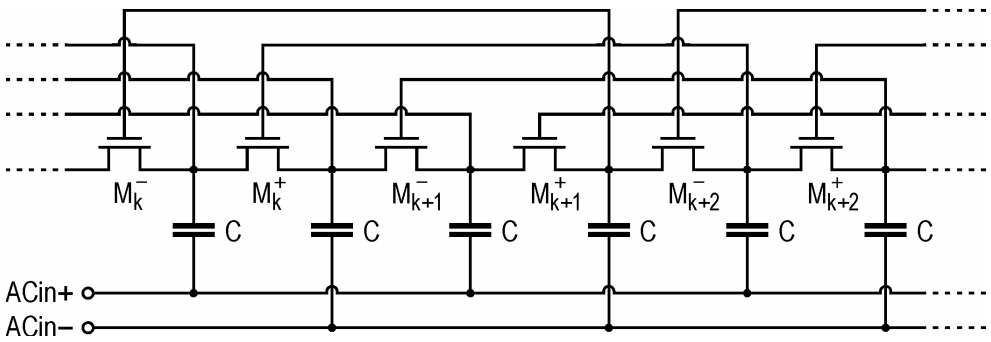


Fig. 2.9. Generalized self-compensation methodology: order-4 compensation.

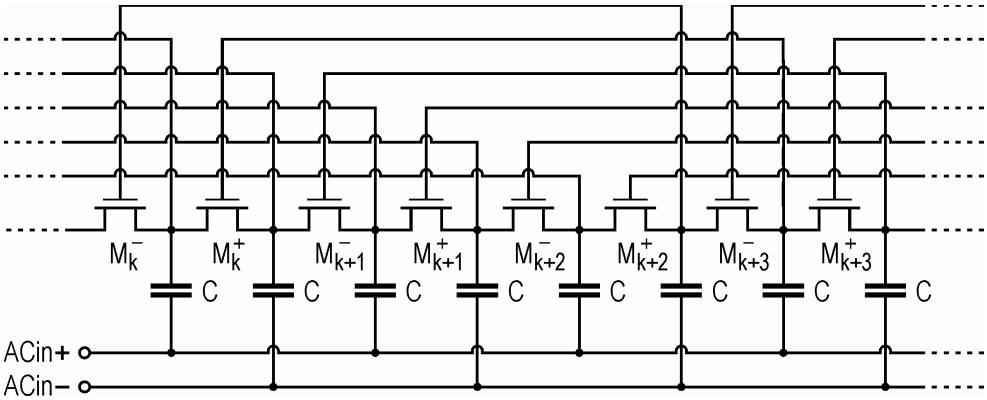


Fig. 2.10. Generalized self-compensation methodology: order-6 compensation.

The bias offset V_C provided by a an order $-n$ compensation topology can be roughly estimated by assuming that in steady-state conditions the average output voltage of the chain is evenly shared among the rectifying devices. Under such assumption, V_C can be easily calculated as:

$$V_C = \frac{nV_O}{2N} \tag{2.4}$$

As shown in (2.4) the proposed methodology allows the bias offset to be increased by merely extending the length of the compensating bridges.

2.1.3 System design considerations

A block diagram of the RF harvesting system is illustrated in Fig. 2.11 along with the reference notation adopted to the purpose of the circuit analysis. As already explained, the system consists of a receiving antenna to draw the RF power radiated by the hub, an impedance matching network to optimize the power

transfer between the antenna and the rectifying chain, and a voltage rectifier to convert the RF power into DC voltage and current to the load.

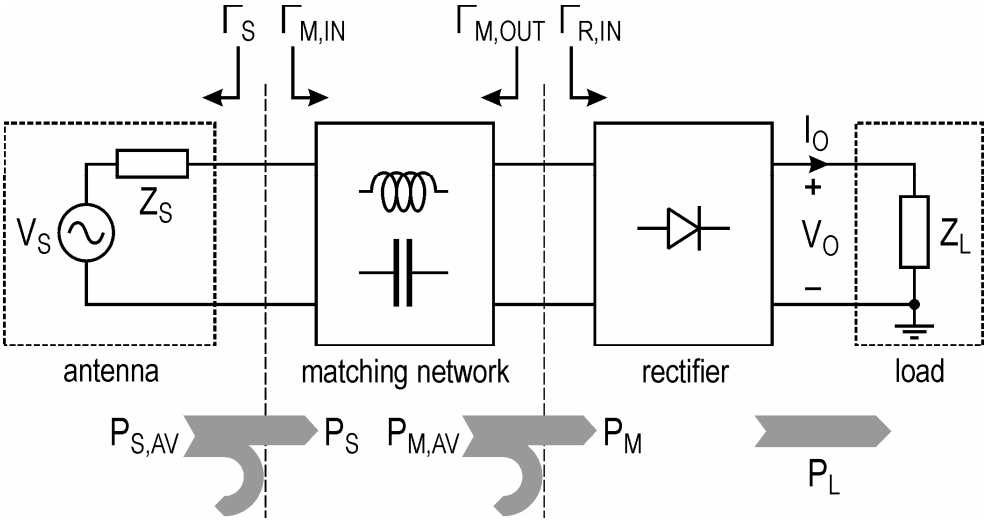


Fig. 2.11. Block diagram of the RF energy harvesting system.

The power conversion efficiency (PCE) of the harvesting system is herein defined as the ratio of the load DC power (P_L) to the available RF power from the antenna ($P_{S,AV}$):

$$\Sigma = \frac{P_L}{P_{S,AV}} \tag{2.5}$$

The main design goal is maximizing the PCE. If the antenna available power is a design constrain, optimizing the PCE results in maximizing the power delivered to a given load. More frequently, the output current and voltage levels are specified in order to comply with the load minimum requirements. Accordingly, PCE optimizations leads to a minimization of the available power at

the antenna connector resulting in the maximization of the node distance from the hub. The latter design case was chosen, as it is more pertinent to our application scenario. Useful considerations about the system can be drawn by expressing the harvester PCE as:

$$\Sigma = G_A \, T \, \eta \tag{2.6}$$

where G_A is the available power gain of the matching network (always lower than 0 dB because of resistive losses), T is the power transmission coefficient at the interface between the matching network and the rectifier, and η is the rectifier inherent efficiency, which is defined as:

$$\eta = \frac{P_L}{P_M} \tag{2.7}$$

Moreover, parameters G_A and T can be expressed by well-known formulas [41] as a function of the scattering parameters of the matching network S_{ij}:

$$G_A = \frac{P_{M,AV}}{P_{S,AV}} = \frac{1-\left|\Gamma_S\right|^2}{\left|1-S_{11}\Gamma_S\right|^2} \left|S_{21}\right|^2 \frac{1}{1-\left|\Gamma_{M,OUT}\right|^2} \tag{2.8}$$

$$T = \frac{P_M}{P_{M,AV}} = \frac{\left(1-\left|\Gamma_{M,OUT}\right|^2\right)\left(1-\left|\Gamma_{R,IN}\right|^2\right)}{\left|1-\Gamma_{M,OUT}\Gamma_{R,IN}\right|^2} \tag{2.9}$$

As apparent from (2.8) and (2.9), G_A is a function of the matching network and antenna impendence, whereas η is only dependent on the rectifier design

parameters. Conversely, coefficient T is a function of both the matching network and rectifier parameters. Therefore, according to (2.6), the design of the whole harvesting system cannot be split into two independent optimizations concerning the matching network and the rectifier, respectively. System *co-design* is needed for an optimum trade-off to be achieved between the rectifier efficiency and its input reflection.

In order to simplify the design task an iterative procedure was developed, which consists in alternatively and repeatedly optimizing the two circuit blocks, namely the rectifier and the matching network. To this aim proper figures of merit were chosen, namely parameters:

$$\Sigma_{\mathrm{M}} = G_{\mathrm{A}}\, T \tag{2.10}$$

$$\Sigma_{\mathrm{R}} = T\, \eta \tag{2.11}$$

Which were considered as figures of merit for the optimization of the matching network and the rectifier, respectively. The proposed design algorithm starts with the optimization of the rectifier (with the goal of maximizing Σ_{R}) for a given output voltage and current levels, assuming a source termination equal to a first-trial value of $\Gamma_{\mathrm{M,OUT}}$. Evaluated $\Gamma_{\mathrm{R,IN}}$, the optimization of the matching network can be performed (with the goal of maximizing Σ_{M}) by assuming a load termination equal to the estimated $\Gamma_{\mathrm{R,IN}}$. Then, a new value of $\Gamma_{\mathrm{M,OUT}}$ is obtained. If this new value is close enough to the initial one, the design procedure is ended, otherwise a new optimization cycle starts with the design of the rectifier assuming a source termination equal to new value of $\Gamma_{\mathrm{M,OUT}}$, and so on. It is worth noting

that the power reflection coefficient T is embedded both in Σ_M and Σ_R. Thanks to this the described iterative procedure is able to converges to the optimization of the whole system PCE splitting the initial design task into two simpler optimizations (see Appendix A), each entailing a lower number of design variables.

2.1.4 Design of the matching network

Impendence matching between the antenna and rectifier is a crucial issue for the optimization of the overall system performance and several studies have been proposed about this topic [42]-[45]. Nevertheless, power losses associated with the matching network have never been formally included in the design flow of a RF energy harvesting system. As long as high-Q components are exploited for impendence matching (e.g. off-chip components), power losses can be neglected. On the other hand, when low-Q matching components are only available and/or high impedance transformation ratio is required (as in [27]), power losses cannot be neglected and care-full co-design is needed to balance losses and reflection. The developed design strategy is the first one that includes power losses of the matching network in the design flow of a energy harvesting system. Indeed, according to (2.8), G_A is embedded into metric Σ_M which is to be optimized. It is worth nothing that the proposed methodology is broadly valid, regardless of the matching network topology, transformation ratio, or fabrication means. If power losses are negligible, $G_A \approx 1$ and $\Sigma_M \approx T$. Hence, optimizing Σ_M leads to perfect matching. Conversely, if losses are tangible, maximizing Σ_M results in an optimal trade-off between losses and reflection. In this case, the optimal solution may

eventually entail a residual impedance mismatch at the rectifier's input for the sake of losses minimization. The proposed design is a typical example of this latter case. Indeed, a general purpose 50-Ω antenna was assumed as source, which entails a large impedance transformation ratio. Moreover, on-chip components were exploited for impedance matching, hence suffering from limited Q values. Fig. 2.12 shows the schematic of the adopted matching network, which was chosen on the basis of a preliminary comparative study between different matching network topologies.

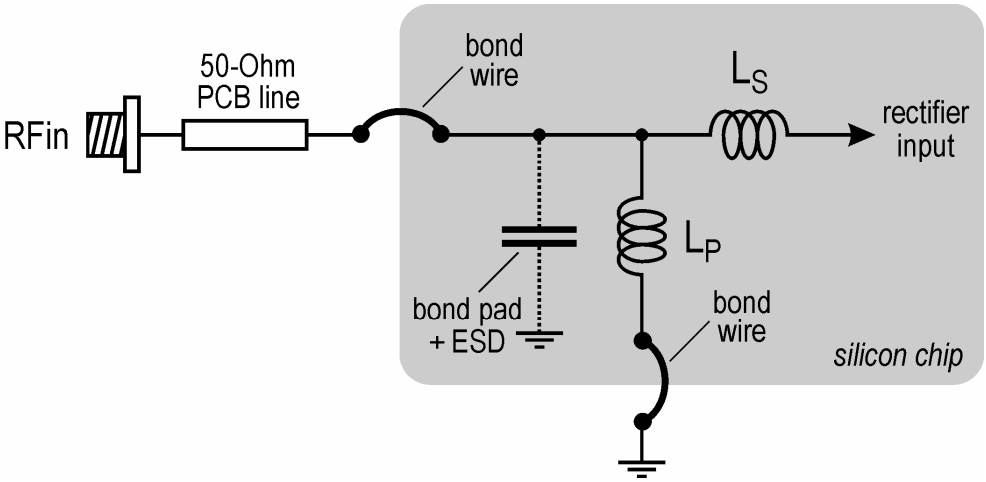


Fig. 2.12. Schematic of the adopted matching network.

According to the aforementioned design methodology, matching network is to be designed with the aim of maximizing Σ_M for a given load termination. In Fig. 2.13 is shown Σ_M as a function of L_S and L_P at 915 MHz. On-chip and package parasitics were taken into account (namely 300-fF bond-pad capacitance and 2-nH wire bonding inductance with a Q of 20 at 900 MHz). For the sake of simplicity the curves reported in Fig. 2.13 were obtained assuming a load

impedance equal to 760 Ω // 1.5 pF ($\Gamma_{R,IN}$ = 0.613 – j 0.652), which is the actual input impedance of the rectifier at the end of the design iteration.

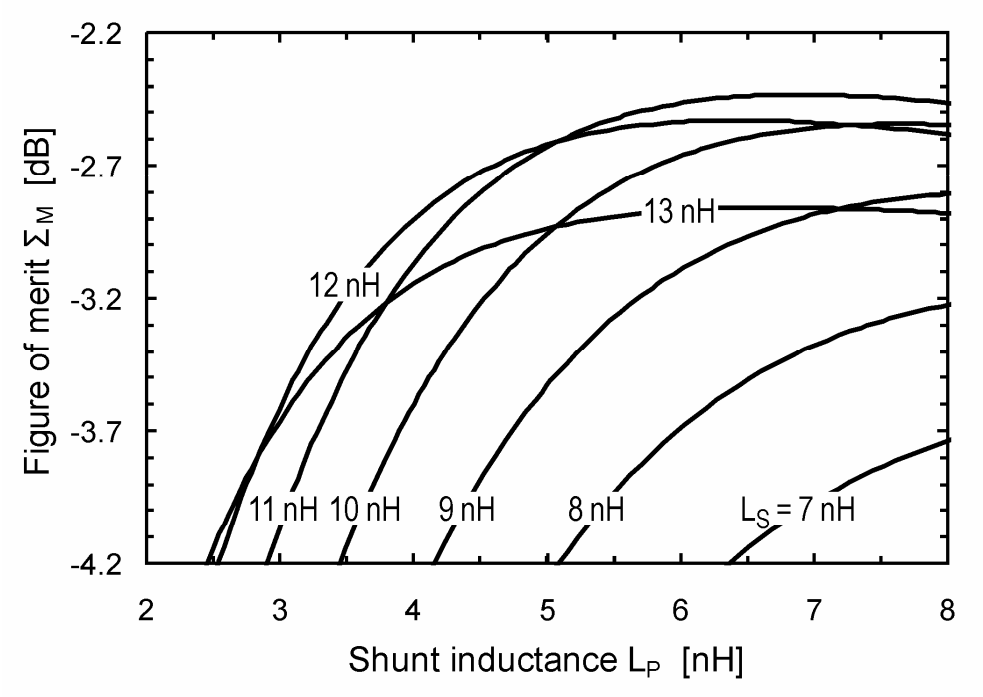


Fig. 2.13. Simulated Σ_M versus L_P for different values of L_S (f = 915 MHz, $\Gamma_{R,IN}$ = 0.613 – j 0.652).

According to the results reported in Fig. 2.13, a series inductance of 11 nH and a shunt inductance of 6.8 nH is needed for optimum design. This choice results in a maximum Σ_M of –2.45 dB with G_A = –1.56 dB and T = –0.89 dB (Fig. 2.14). Note that, the designed matching network is far from guarantee the maximum power transfer (i.e. T = 0 dB). Nevertheless, this design provides the best trade-off between losses and reflection. Basically, different values of L_S and L_P are needed to optimize T. However, the best-T solution would lead to a poorer overall system performance compared to the best-Σ_M solution.

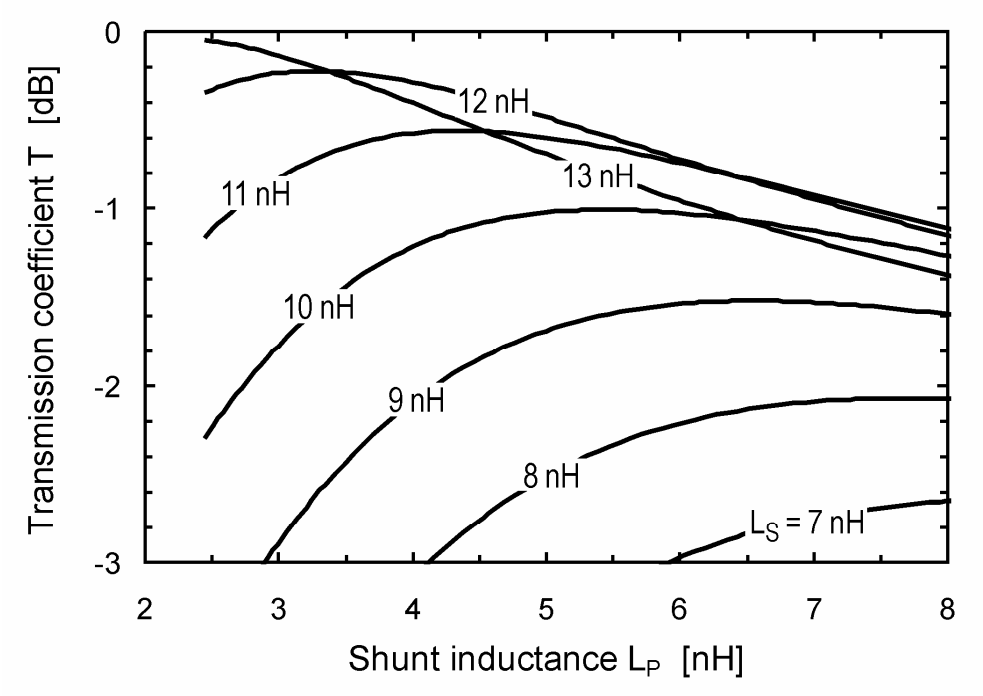


Fig. 2.14. Simulated transmission coefficient T as a function of L_P for different values of L_S (f = 915 MHz, $\Gamma_{R,IN}$ = 0.613 – j 0.652).

2.1.5 Design of the rectifier

NMOS transistors with isolated bodies were used for this design, thanks to the availability of a deep n-well layer in the adopted fabrication process. Moreover a static connection of the body to the source terminal of each pumping device was adopted, rather than exploiting a dynamic control of the well voltage as proposed in [46], since this strategy proves ineffective under very low pumping voltage conditions, as typical for micro-power RF energy harvester.

Three key parameters are to be determined for the deign of the threshold self-compensated rectifier, namely the number of cascaded stages N, the gate width of pumping devices W, and the compensation voltage V_C. The transistor gate length was set to the minimum allowed value (90-nm for the adopted CMOS

process) in order to optimize the RF performance, whereas the coupling capacitors C are large enough to avoid affecting the conversion efficiency. The design goal is maximizing Σ_R for a given source termination. As already mentioned, the output DC voltage and current levels should be considered as design constraints, according to the load minimum requirements. On the basis of a preliminary feasibility study, a 1.2-V output voltage on a 1-MΩ load (i.e. 1.2-μA output current) was assumed as the nominal design target. Thus an output-constrained parametric analysis of Σ_R was carried out according to such assumption. To ease this analysis, circuit simulations were initially performed by recourse to the simplified schematic shown in Fig. 2.15, where the threshold compensation voltage is applied through ideal DC voltage sources V_C.

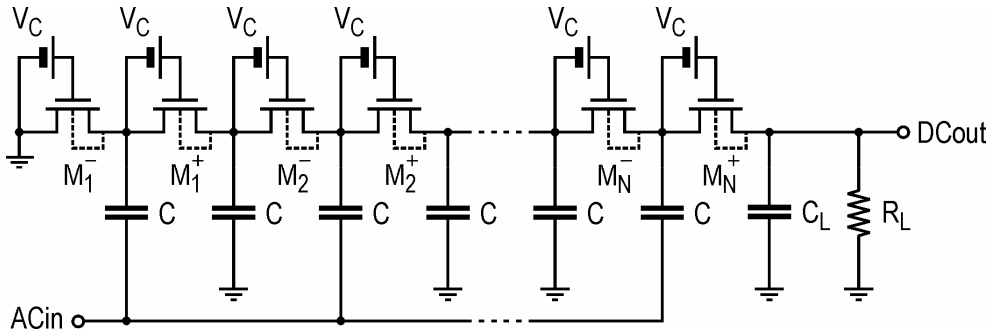


Fig. 2.15. Simplified schematic of a threshold-compensated multi-stage rectifier.

Once determined the optimum value for V_C, ideal voltage sources can be replaced by the proposed forward gate connections, compensation order being chosen in order to best fit the designed gate bias offset under nominal operating

conditions. Note that the simulated performance of the simplified topology (Fig. 2.15) is really close to the one of the real circuit with gate bridges.

Fig. 2.16 displays the typical dependence of Σ_R on N and W for a given value of V_C. The contour plots of η and T are also reported in Fig. 2.17. For the sake of simplicity these plots were calculated assuming a source impedance of 300 Ω // 20.2 nH ($\Gamma_{M,OUT}$ = 0.508 + j 0.557) which is the actual output impedance of the matching network at the end of the design flow.

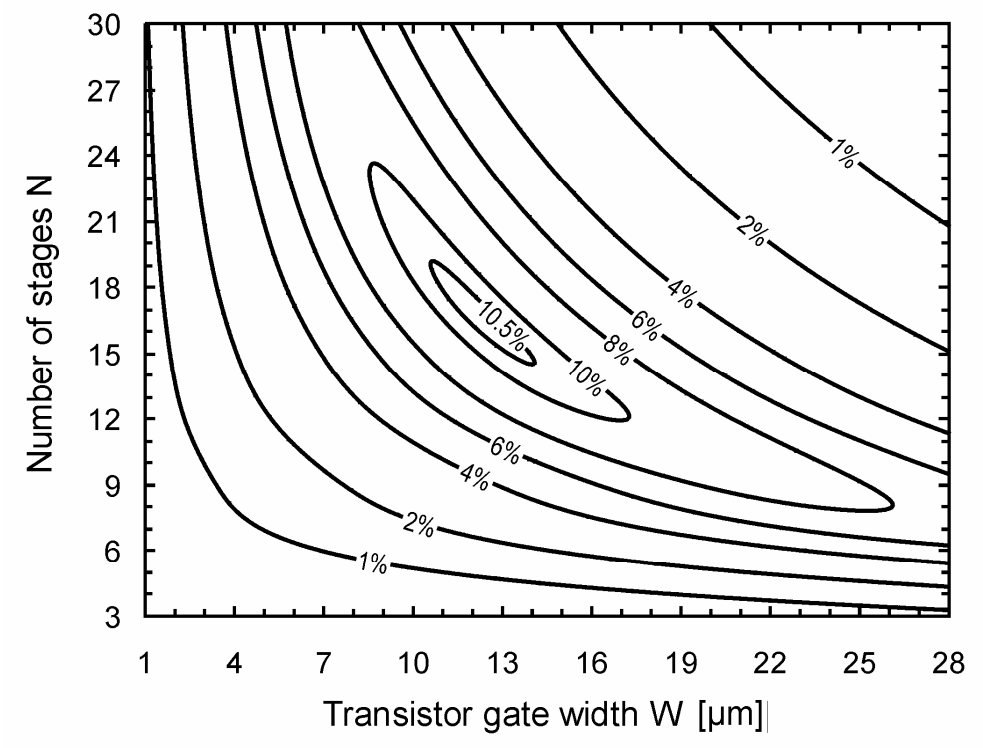


Fig. 2.16. Simulated percentage Σ_R versus N and W for a compensation voltage V_C of 240 mV (V_O = 1.2 V, R_L = 1 MΩ, L = 90 nm, C_L = 47 nF, C = 3 pF, f = 915 MHz, $\Gamma_{M,OUT}$ = 0.508 + j 0.557).

As apparent from Fig. 2.16, optimum values of both N and W can be identified for a given value of V_C.

This behaviour is well-known and consistent with previously reported analysis [33][42][43] As a matter of fact, the rectifiers' inherent efficiency decreases with the number of stages *N*, but a too low stage count would result in a excessively high input impedance, i.e. high power reflection. Similarly, increasing the transistors' gate with *W* favours direct conduction, thus increasing efficiency. However, too large devices would eventually entail excessive parasitic losses and reverse (leakage) conduction.

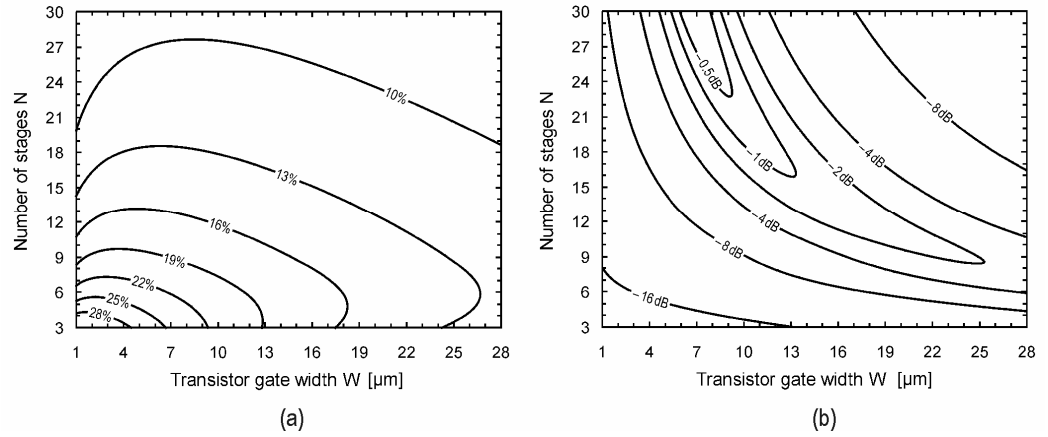


Fig. 2.17. Simulated contour plots of η (a) and T (b) as a function of N and W for a compensation voltage V_C of 240 mV (V_O = 1.2 V, R_L = 1 MΩ, L = 90 nm, C_L = 47 nF, C = 3 pF, f = 915 MHz, $\Gamma_{M,OUT}$ = 0.508 + j 0.557).

Interestingly, the peculiar dependence of Σ_R on N and W displayed in Fig. 2.16 keeps qualitatively unchanged as compensation voltage V_C is varied. Therefore a relative maximum for Σ_R exits for any V_C, as illustrated in Fig. 2.18.

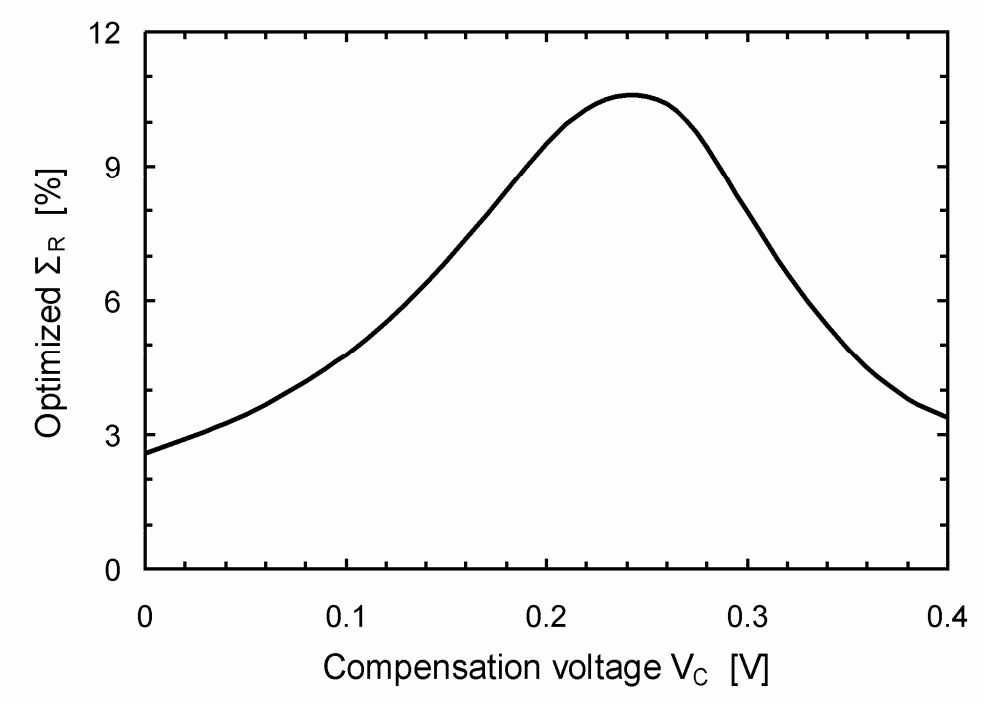


Fig. 2.18. Optimized Σ_R versus V_C (V_O = 1.2 V, R_L = 1 MΩ, L = 90 nm, C_L = 47 nF, C = 3 pF, f = 915 MHz, $\Gamma_{M,OUT}$ = 0.508 + j 0.557).

This plot reveals that an optimum value exits for V_C as well, which results in a global maximization of Σ_R. Note that, such optimum V_C value is quite far from the typical threshold voltage of the adopted technology, which is around 0.45 V. Indeed, increasing V_C improves the transistors' conductivity, but worsens their rectifier behaviour (i.e. the reverse conduction increase) [40]. Therefore a fair trade-off is needed to achieve the best performance.

According to the performed parametric analysis (Fig. 2.16 and Fig. 2.18), a 17-stage rectifier topology was adopted for optimum design along with a 12-μm transistor width and a compensation voltage of 240 mV. The latter was implemented exploiting an order-6 compensation topology (Fig. 2.10).

Concerning this, It should be observed that the gates of the last 5 transistors of a order-6 self-compensated NMOS rectifier require DC voltages higher than the delivered one. In general this problem affects the last *n*-1 transistors of an order-*n* compensated topology. This issue was addressed by cascading an additional "dummy" chain to generate higher DC voltage to be used for the threshold compensation of the last transistors of the pumping chain.

The tail end of the designed rectifier is shown in Fig. 2.19. The last transistor of the pumping chain (M_{17}^{+}) is purposely uncompensated to limit the reverse leakage current of the rectifier. For the designed rectifier, a Σ_R of 10.6% was simulated at V_O = 1.2 V on a 1-MΩ load.

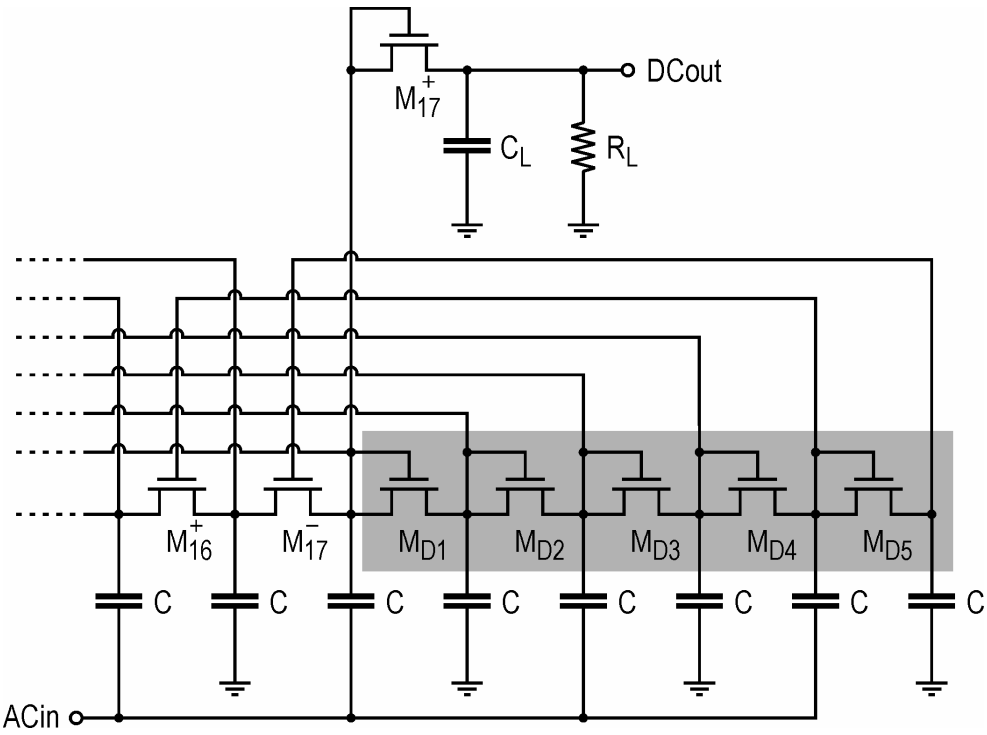


Fig. 2.19. Schematic of the rectifier's tail end with additional dummy chain.

2.1.6 Harvester simulated performance

The designed energy harvesting system consists of an improved 17-stages rectifier (Fig. 2.10),exploiting a fully passive threshold self-compensation scheme, and an integrated matching network (Fig. 2.12) which allows interfacing the rectifier with a general purpose 50-Ω antenna. The system operates in the 915-MHz ISM band. Following the developed design methodology a simulated Σ_R of 10.6% was achieved (assuming an output voltage of 1.2-V on a 1-MΩ load) with a G_A of -1.56 dB. Thus, according to (2.6) a PCE of 7.4% was estimated for the overall harvesting system. Therefore, it is able to provide a 1.2-μA output current on a 1-MΩ load with an available input power at the antenna of -17.1dBm.

2.2 Power management unit

The energy collected by the RF harvester is accumulated in a storage capacitor and properly used to supply the whole system. Implementing an active transmission scheme entails a transceiver energy budget that can only be accomplished by adopting a convenient power management strategy, which is based on a duty-cycled operation mode ("charge & burst") of the RF front-end (Fig. 2.20). As the hub illuminates the network by radiating its FSK-modulated carrier, the harvesting unit of each sensor node starts charging the storage capacitor (*charge phase*). The power management unit monitors the charge status of the storage capacitor by sensing its voltage drop and turns the RF front-end on as soon as a fair supply level is reached ($V_{STORE(high)}$ in Fig. 2.20). After being turned on, the transceiver undergoes a *listen phase* searching for a possible

interrogation by the hub. If an interrogation is detected within the code sent by the hub, a *transmit phase* follows, in order to answer to the hub.

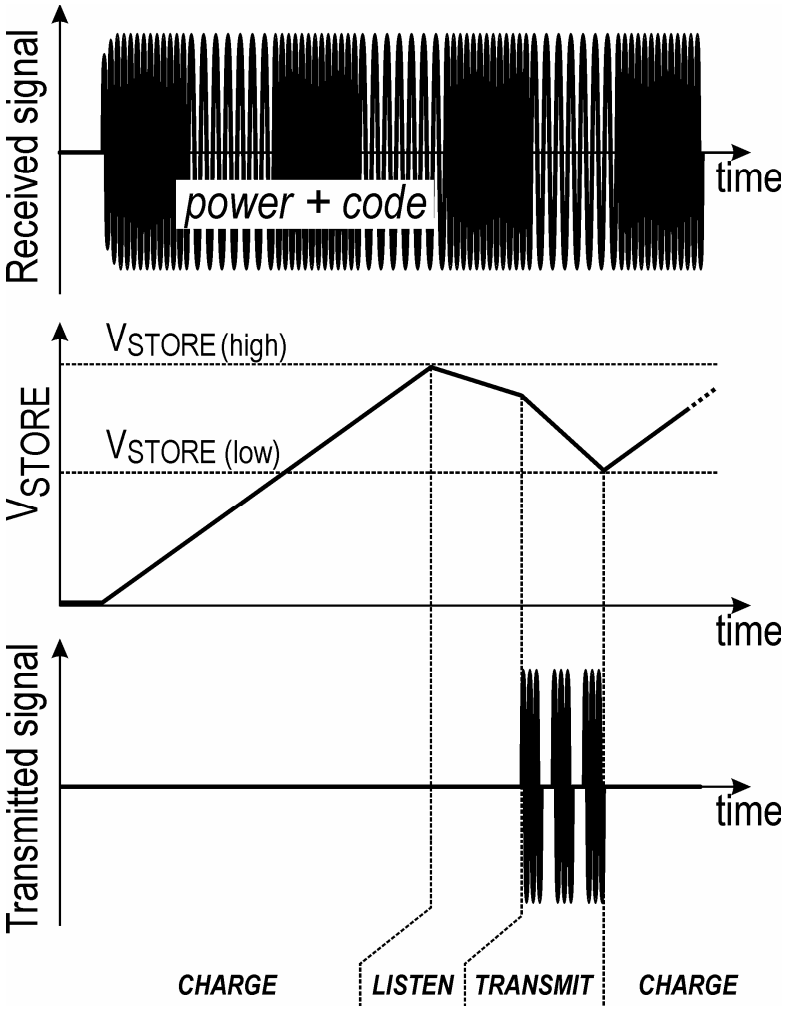


Fig. 2.20. Power management strategy (*charge & burst*).

The current consumption associated to the listen and transmit phases progressively discharges the storage capacitor, since the instantaneous supply power required by the RF front-end is much higher than the harvested one. Therefore, as the voltage drop across the storage capacitor reaches a predefined minimum value ($V_{STORE(low)}$ in Fig 2.20), the power management unit turns the RF

front-end off and a new charge phase starts. The main benefit resulting from the charge & burst procedure lies in the possibility to spend in a relatively short time interval (listen and transmit phases) the energy accumulated in a quite longer phase (charge phase). Indicating with δ the duty cycle of the transceiver on/off commutation, the adopted strategy results in an available supply power which is 1/δ times higher than the harvested one. For instance, if a 1-μW power is continuously harvested from the incoming RF signal and the system is operated with a 1‰ duty cycle, then a 1-mW power is available to supply the transceiver during the operating phase. This key feature enables active transmission at 2.45-GHz. A block diagram of the power management unit is shown in Fig. 2.21.

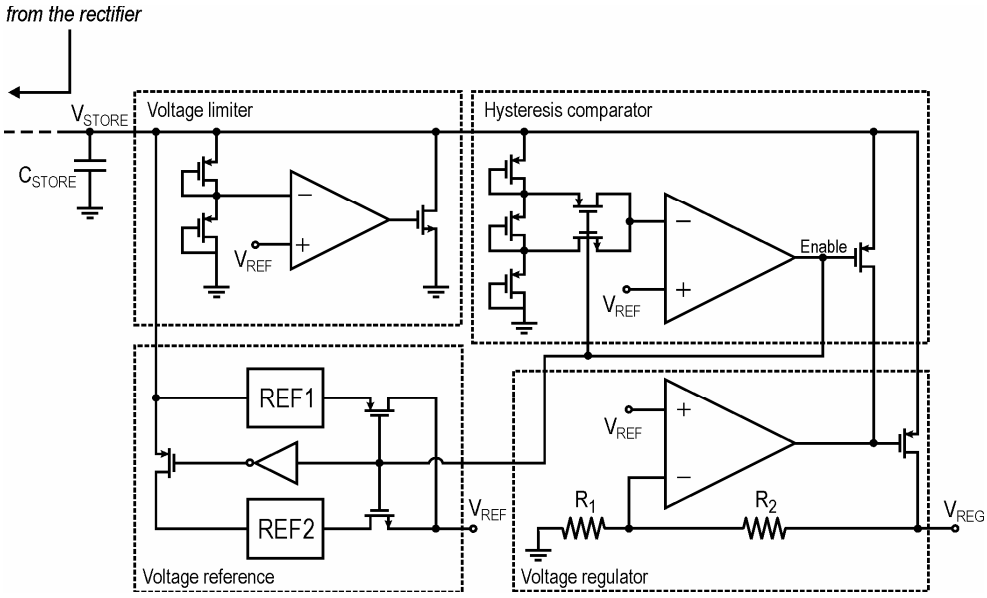


Fig. 2.21. Block diagram of the power management unit.

It manly consists of a voltage reference, an hysteresis comparator, a voltage regulator and a voltage limiter. During the charge phase, the hysteresis comparator senses the voltage drop across the storage capacitor and turns the

voltage regulator on as soon as a 1.6-V supply voltage ($V_{STORE(high)}$) is reached. After being turned on, the voltage regulator is able to deliver 1-V supply voltage to the RF front-end, with a maximum output current of 1 mA. During this phase, the storage capacitor discharges rapidly till a predefined low voltage ($V_{STORE(low)}$), set to 1.2 V. Then, the comparator turns the regulator off allowing the harvester to recharge the storage capacitor.

Nano-power circuits were extensively adopted for the power management unit design in order to guarantee negligible power consumption (lower than 100 nA) during the charge phase improving the harvester efficiency and charge rate.

Moreover, the power management unit includes a voltage limiter, which was designed to clamp the unregulated voltage (V_{STORE}) if the maximum safe level is overcome. Concerning this, ultra-thick-gate-oxide transistors were extensively used for the design of the power management unit circuits to guarantee safe operation with an unregulated voltage up to 1.8 V.

2.2.1 Voltage reference

The voltage reference is the most critical block of the power management unit. Indeed, an accurate voltage reference is needed for proper operation of the whole system. This reference should be able to operate with a low supply voltage, be independent of V_{STORE} variations, exhibit a good temperature stability and have an extremely low current consumption.

To meet all these requirements, an architecture exploiting two voltage references (*REF1* and *REF2*) with complementary electrical performance was

used. *REF1* was designed for nA-level current consumption, whereas *REF2* exhibits a better stability over temperature and supply voltage variations at the cost of a higher current consumption. The two references are alternatively enabled during each system operating cycle, specifically, *REF1* during the charge phase and *REF2* during the *discharge phase* (i.e. listen and transmit phases). This allows achieving both minimal off-state (charge phase) current leakage and high on-state (discharge phase) accuracy.

The schematics of *REF1* and *REF2* are shown in Fig. 2.22 and Fig. 2.23, respectively. *REF1* was implemented exploiting a self-biased current reference based on ΔV_{BE} and a MOS transistor (M_5) working below saturation ($PTAT^2$ configuration) [47][48], which allows an extremely low current consumption to be achieved with a substantial silicon area savings.

The ΔV_{BE}-based current mirror was designed using parasitic npn bipolar transistors (Q_1 and Q_2). Assuming that the current mirror M_1-M_2 has a ratio 1:1, the $I_{PTAT}{}^2$ current can be expressed as:

$$I_{PTAT^2} \cong \frac{2\left(K_3 \frac{W_3}{L_3}\right)^2}{K_4 \frac{W_4}{L_4}} V_T{}^2 [\ln(C)]^2 \tag{2.12}$$

Where $C = \frac{A_{E1}}{A_{E2}}$, and $K = \mu_n C_{ox}$.

To cancel the quadratic dependence from the temperature, the current $I_{PTAT}{}^2$ is fed via transistor M_3 to the diode-connected transistor M_4, which was sized in order to provide a reference voltage of 0.6 V [49]. The reference *REF1* exhibits a

simulated temperature coefficient of 160 ppm /°C at 1.6 V with an extremely low current consumption (≈ 40 nA).

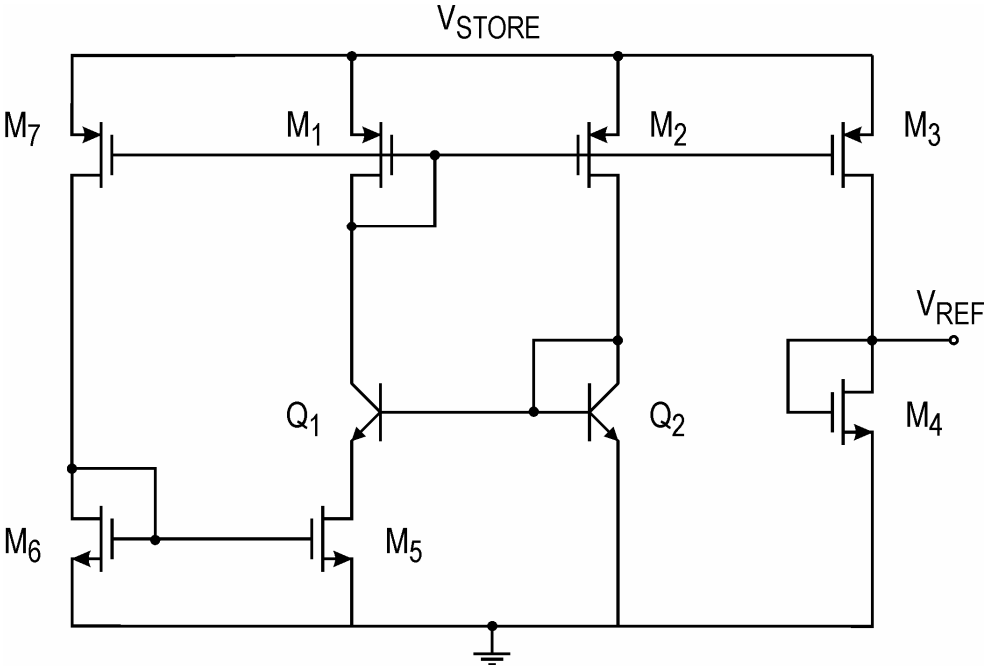


Fig. 2.22. Schematic of the nano-amp voltage reference (*REF1*).

REF2 operates during the listen and transmit phases. During this phases the unregulated supply voltage (V_{STORE}) experiences a fast and large variation, from 1.6 V to 1.2 V. Therefore, unlike *REF1* which has to be accurate just at 1.6 V, *REF2* must be able to guarantee accuracy in a wide range of supply voltage. To this purpose, a self-biased *PTAT* current reference with resistor (R) was used to implement *REF2*, as shown in Fig. 2.23.

This solution allows achieving a better accuracy and stability over supply voltage variations at the cost of a much higher current consumption. However, *REF2* is enabled only during the discharge phase, when the main contribution to the whole system current consumption is due to the RF front-end, which is the

most power-hungry component of the designed transceiver. The PTAT current is fed to a diode-connected transistor (M_4) working in sub-threshold in order to guarantee the temperature compensation with the suppression of the temperature dependence of the *charge carrier mobility* [47].

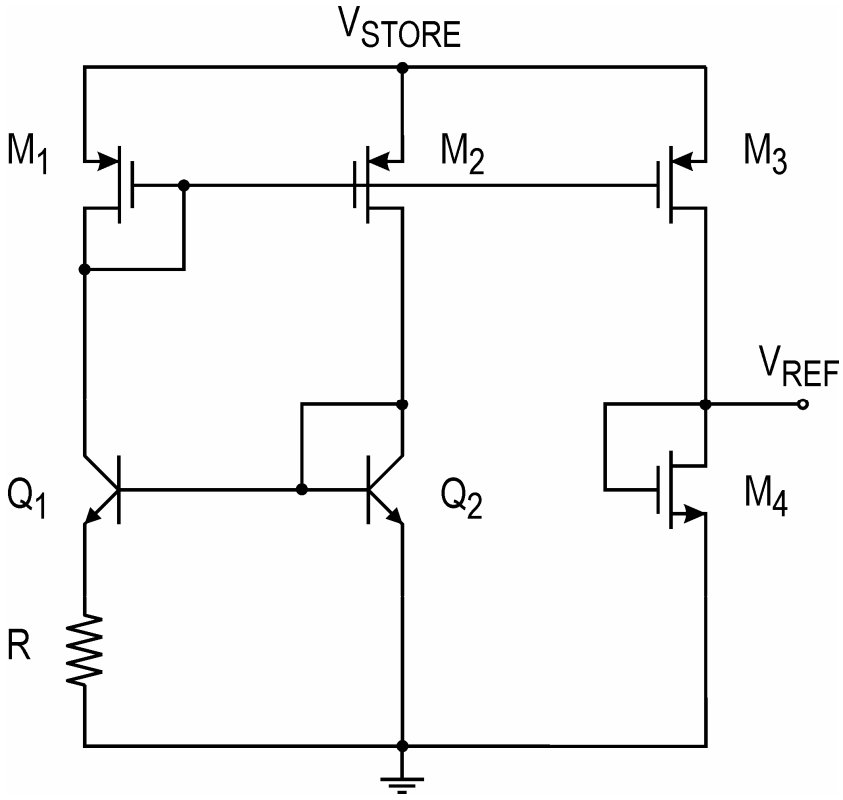


Fig. 2.23. Schematic of the PTAT-based voltage reference (*REF2*).

REF2 was designed to provide a voltage of 0.6 V and exhibits a simulated temperature coefficient of 53 ppm/°C. The simulated temperature dependence of *REF1* and *REF2* are shown in Fig. 2.24 and Fig. 2.25, respectively.

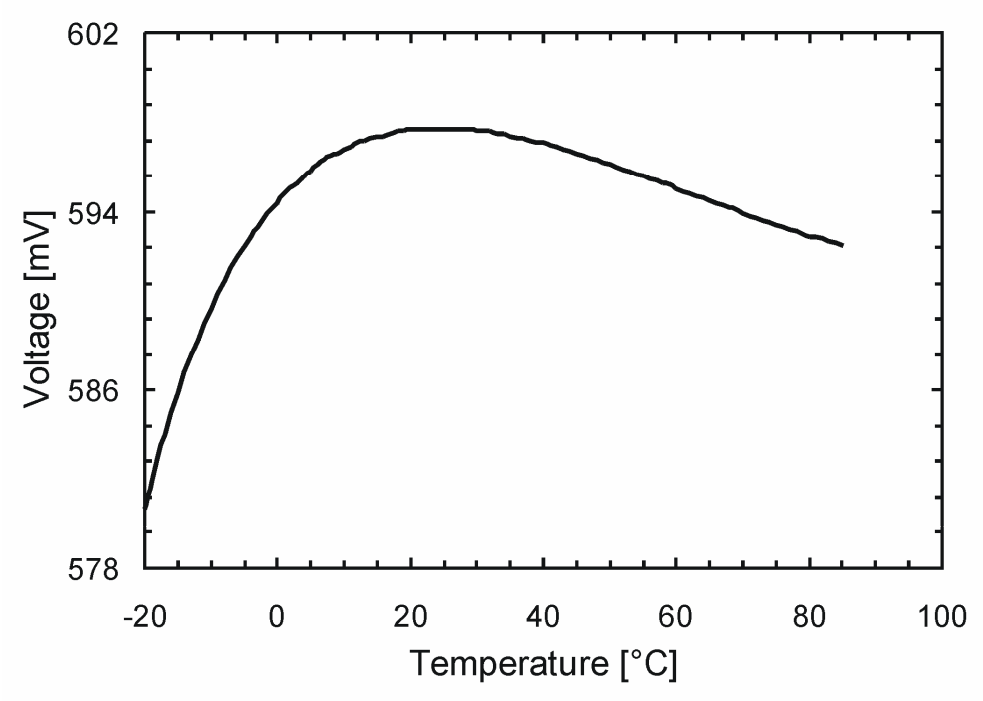


Fig. 2.24. Simulated temperature dependence of the voltage reference *REF1* (V_{STORE} = 1.6 V).

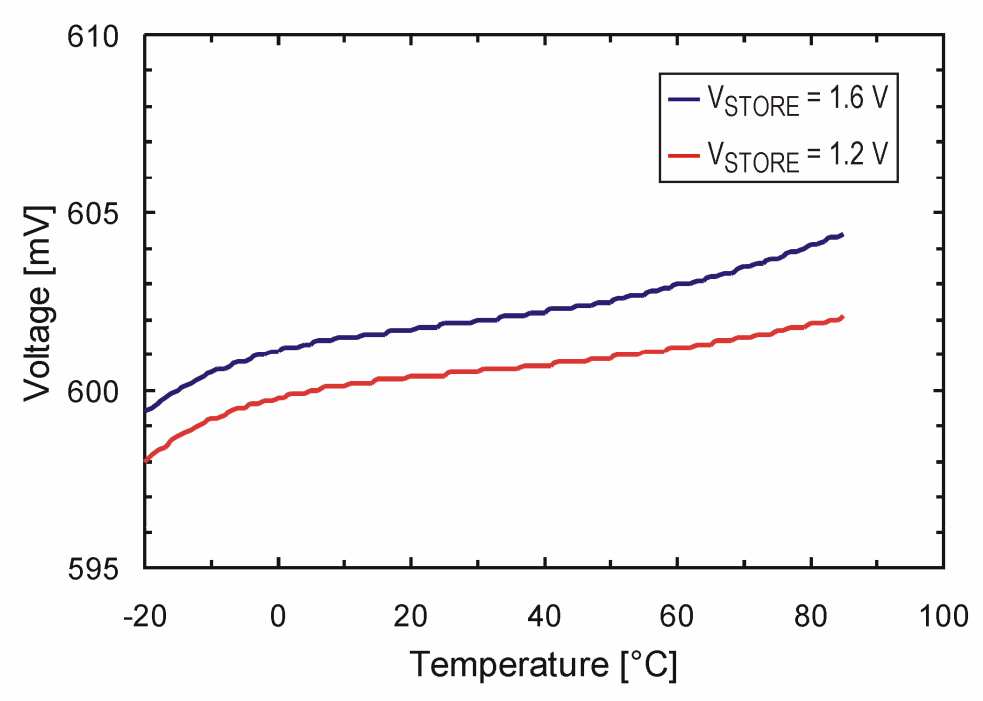


Fig. 2.25. Simulated temperature dependence of the voltage reference *REF2*.

2.2.2 Hysteresis comparator

The hysteresis comparator provides a logic level "1" at its output (*enable signal*) when the unregulated supply voltage (V_{STORE}) reaches the predefined high level $V_{STORE(high)}$. Conversely, the enable signal is set to the logic level "0" when V_{STORE} drops below the predefined low level $V_{STORE(low)}$, as shown in Fig. 2.26.

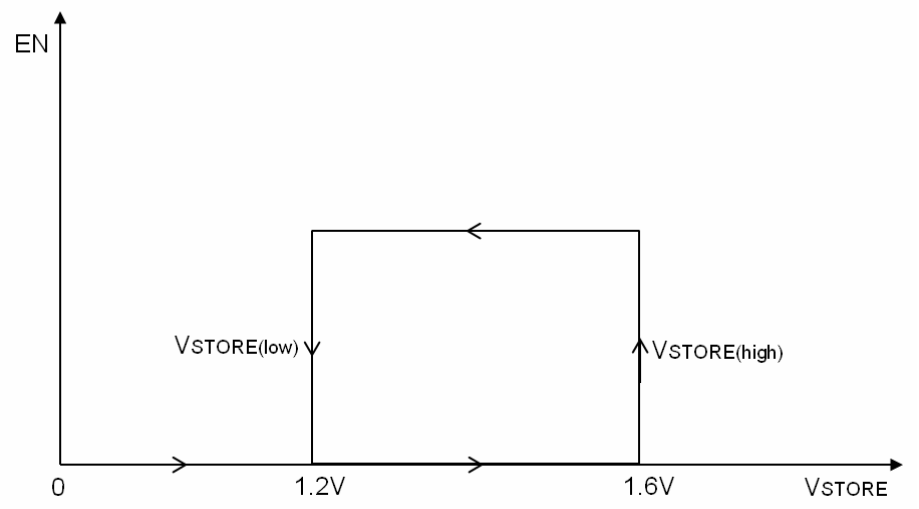


Fig. 2.26. Hysteretic characteristic of the comparator.

Fig. 2.27 displays the schematic of the designed hysteresis comparator. It is based on a two-stage amplifier with a differential input pair (M_1-M_2) and a diode-connected transistor string used to detect the unregulated voltage. Switches M_{sw1} and M_{sw2} (properly controlled by the enable signal) allow implementing the "hysteretic characteristic" with threshold voltages $V_{STORE(high)}$ and $V_{STORE(low)}$. Concerning this, it is worth noting that, as the enable signal goes high, the transistor count of the sensing string is reduced thanks to the switch M_{sw3}.

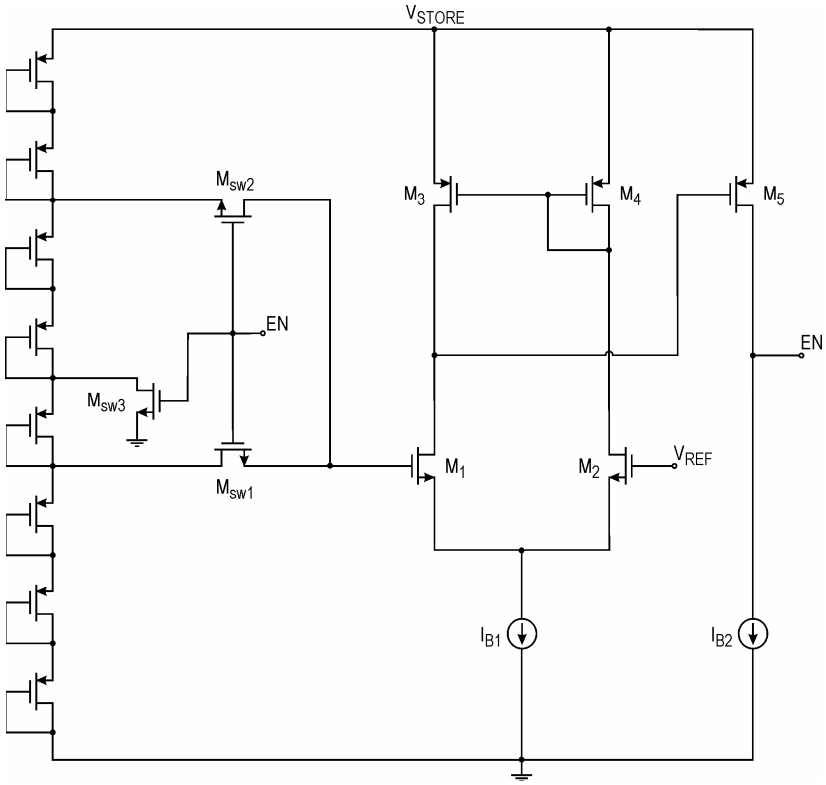


Fig. 2.27. Schematic of the hysteresis comparator.

This results in an improved circuit speed at $V_{STORE(low)}$, which allows to prevent faulty switching without increasing the comparator current consumption during the charge phase. Indeed, the overall current consumption of the comparator is set by the current drawn by the sensing string. Changing the transistor count according to the actual operating phase improves the switching speed during the discharge phase (by reducing the transistor count), keeping, at the same time, a low current consumption (17 nA) during the charge phase (by increasing the transistor count). Incidentally, minimum-size transistors were used to implement switches M_{sw1}-M_{sw3} (L = 380 nm, W = 1 um) for improved switching speed. Thick-gate-oxide transistors (3.3-V nominal supply voltage) were

extensively exploited for the hysteresis comparator design to the aim of guarantee safe operation with the unregulated supply voltage (V_{STORE}).

2.2.3 Voltage regulator

As already explained, the designed voltage regulator is able to provide a 1-V regulated supply voltage with a maximum output current of 1-mA (Fig. 2.28). The adopted topology exploits an operational amplifier in non-inverting configuration, with three gain stages and nested-Miller compensation [50].

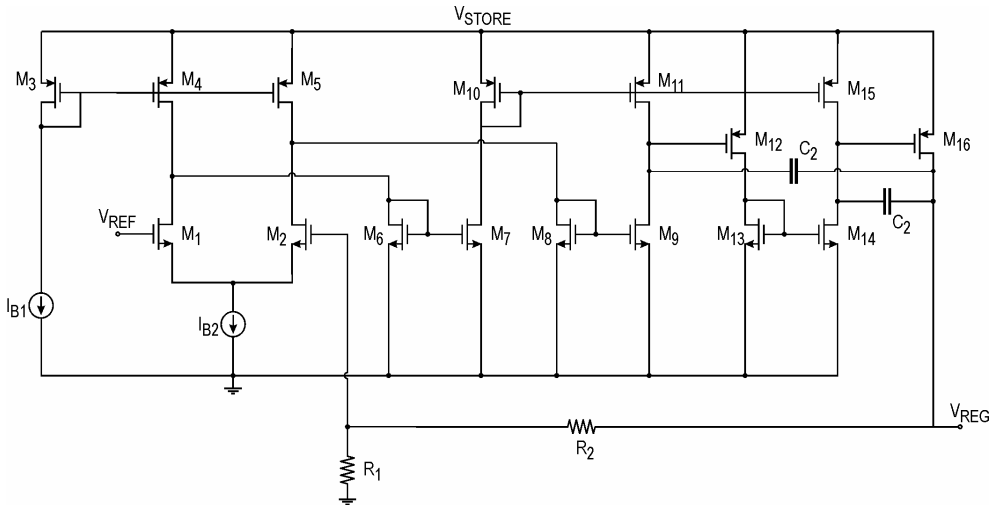


Fig. 2.28. Schematic of the voltage regulator.

Thick-gate-oxide transistors (3.3-V nominal supply voltage) were extensively used for the design of the voltage regulator. Thin-gate–oxide devices were only exploited to implement the transistors of the differential input pair (M_1-M_2), in order to allow them to operate in saturation regime with a reference voltage (V_{REF}) of 0.6 V. Diode-tied transistors (M_6 and M_8) are connected to the output terminals of the differential input pair in order to set the drain voltages of

M_1 and M_2 at around 0.7 V. This allows avoiding gate oxide breakdown of these transistors. To provide a maximum output current of 1-mA, M_{16} size was chosen to be 60µm/380nm. Finally, the simulated performance in terms of gain, gain-bandwidth and phase margin is 82 dB, 13 MHz and 60°, respectively.

2.2.4 Voltage limiter

A voltage limiter was designed in order to clamp the unregulated voltage V_{STORE} if the safe level (1.8 V) is overcome. The schematic of the voltage limiter is reported in Fig. 2.29. It is based on a two-stage differential amplifier, which drives a common source transistor M_{12} connected between V_{STORE} and ground. If the unregulated supply voltage exceeds 1.8 V, M_{12} (W/L = 1µm/380nm) is turned on and draws a 50-µA current (i.e. higher than the maximum DC current expected at the harvester output) from the storage capacitor reducing the voltage drop across its terminals. In typical operating conditions, V_{STORE} does not exceed 1.6 V and transistor M_{12} is kept off. The unregulated supply voltage is detected through a diode-tied transistor string for reduced silicon area occupation.

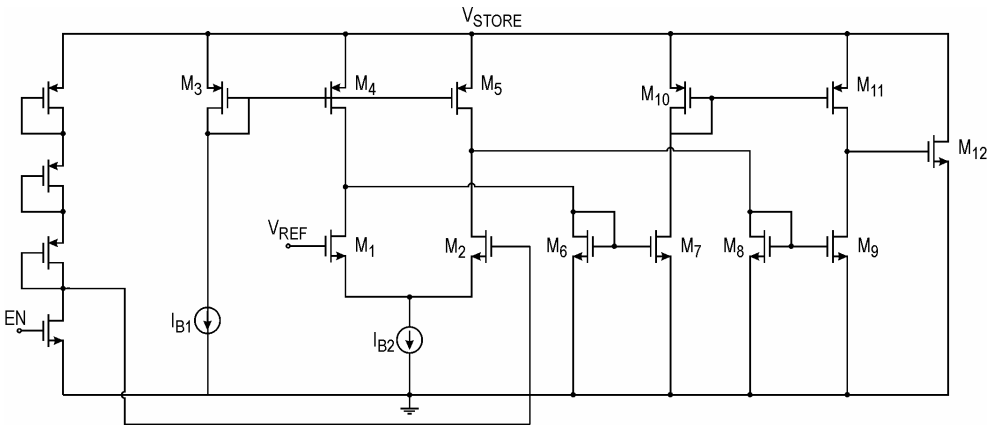


Fig. 2.29. Schematic of the voltage limiter.

2.2.5 Power management unit simulated performance

A power management unit was designed to the aim of implementing a duty-cycled operation scheme for the RF front-end (charge & burst). This enables active transmission besides improving the harvester sensitivity and charge rate. The designed circuits and related design strategies were analyzed in the previous sections, here a summary of the simulated performance related to the whole system is provided. The transient response of the most meaningful signals of the power management unit is reported in Fig. 2.30 and Fig. 2.31. The simulated settling time of the enable signal (*EN*) is of 160 ns and 115 ns for the $V_{STORE(high)}$ (Fig. 2.30) and $V_{STORE(low)}$ (Fig. 2.31) commutations, respectively.

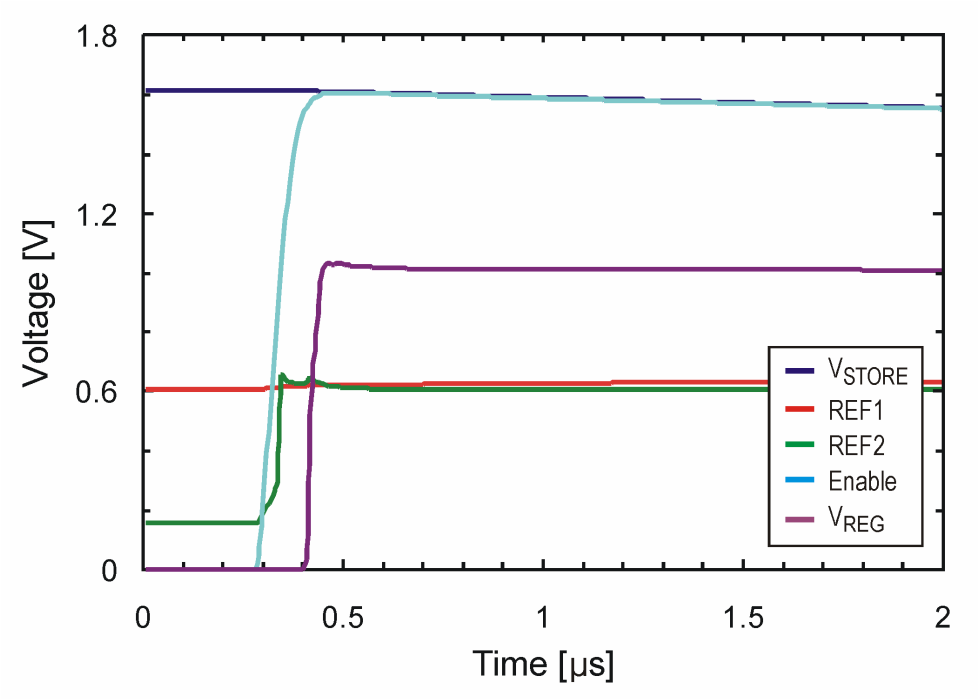


Fig. 2.30. Power management transient response ($V_{STORE(high)}$ commutation).

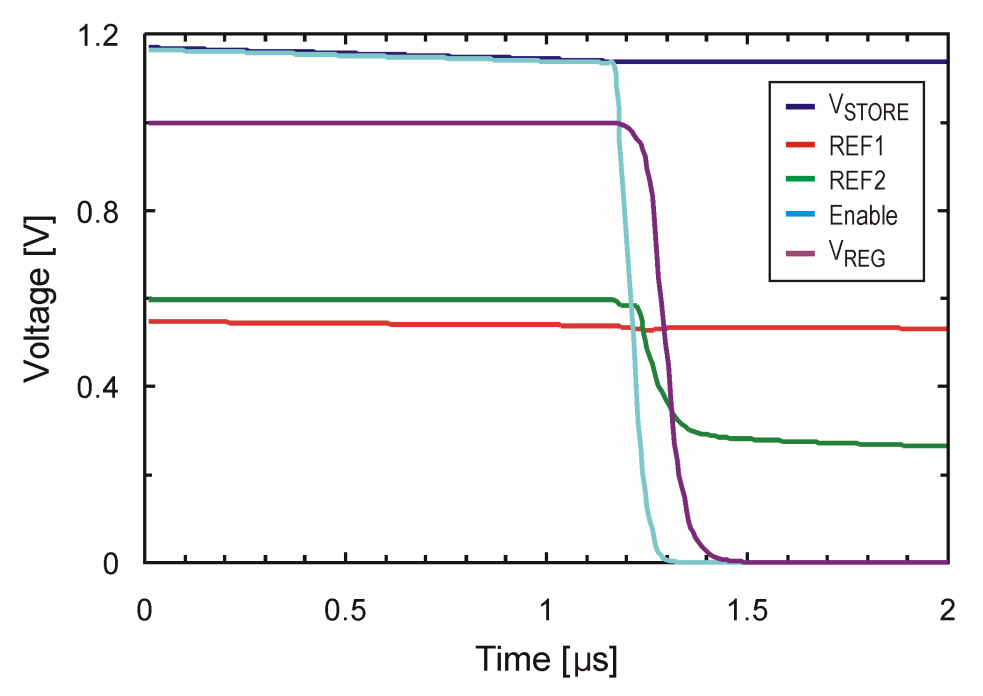


Fig. 2.31. Power management transient response ($V_{STORE(low)}$ commutation).

Finally the most meaningful performance parameters of the power management unit are summarized in Table 2.1.

Table 2.1. Simulated performance summary.

BLOCK	Hysteresis comparator	Reference Ref1	Reference Ref2	Regulator	Limiter
Current consumption	32nA	38nA	13µA	75µA	11µA
Leakage current	-	-	~pA	70pA	80pA
Transient (ton)	160ns (Pwron)	-	75ns	70ns	120ns
Transient (toff)	115ns (Pwron)	-	20ns	200ns	200ns

The power management unit exhibits an extremely low current leakage (70 nA at V_{STORE} = 1.6) during the charge phase.

2.3 RF front-end

In the adopted network architecture, the RF signal transmitted by the hub provides sensor nodes with data and reference frequency besides powering them up. Accordingly, each network node must be equipped with a RF front-end enabling both data and carrier recovery from the incoming RF signal. In the proposed batteryless transceiver this task is accomplished by exploiting a RF front-end based on a PLL with static divide ratio and a second order on-chip loop filter, as sketched in Fig. 2.32.

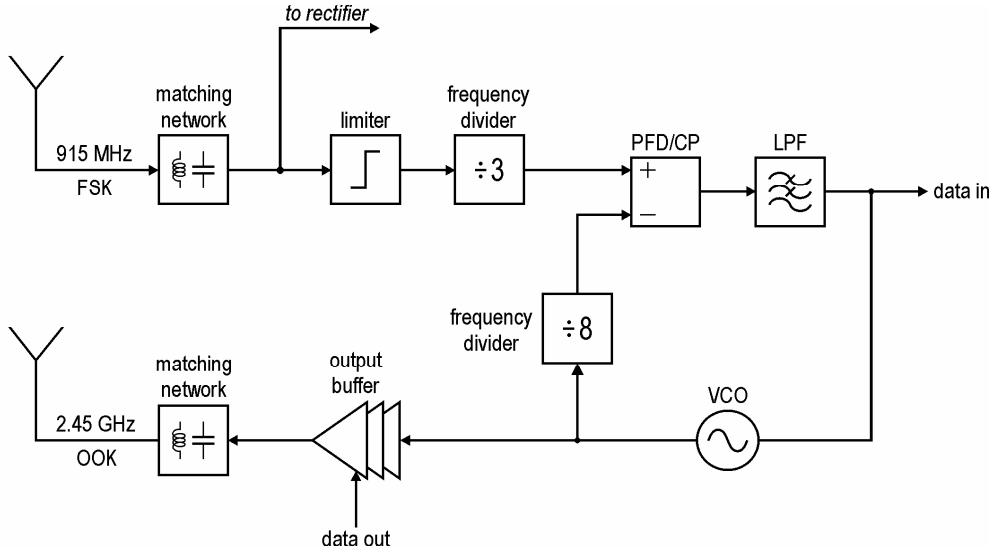


Fig. 2.32. Block diagram of the RF front-end.

Basically, the RX section of the designed RF front-end consists of a limiting circuit followed by a frequency divider, whose output signal acts as reference frequency for an integrated PLL. The latter performs both the demodulation of the FSK-modulated input signal and the synthesis of the transmission carrier. Finally,

the TX section consists of an output buffer, which is able to send data to the hub in OOK mode exploiting the carrier synthesized by the RX section. This architecture allows achieving an high integration level, since it doesn't need any external reference frequency (typically provided by a quartz oscillator) for its operation. The operating principle of the proposed system is as simple as effective. During the listen phase, a 915-MHz FSK-modulated signal is fed to the transceiver input. After being converted into a square wave through a limiting amplifier (or *limiter*), this signal is provided to the input of a frequency divider, which properly lowers its frequency. The obtained signal acts as reference frequency for the PLL. Once it is locked, the VCO control voltage tracks the frequency deviations of the reference. Therefore, if the frequency of the input signal switches between two different values, according to a BFSK modulation scheme, the VCO control voltage is changed correspondingly. Amplifying these voltage fluctuations allows data recovery to be accomplished. Moreover, a frequency ratio of 8/3 is performed for f_{OUT}/f_{REF} in order to synthesize a carrier that lies in the 2.45-GHz ISM band from the 915-MHz input. During the transmit phase, this carrier is used to send data to the hub in OOK mode.

Although a RF harvester was embedded in the manufactured prototype, the proposed transceiver may be supplied by different power sources (e.g. piezoelectric, photovoltaic, ecc) and the related energy scavenger systems may be optionally integrated on the same platform. Therefore, the RF front-end design goals weren't merely related to the RF harvester performance. As a matter of fact, the RF front-end was designed to achieve a receiver sensitivity of about –30 dBm and a maximum transmitted power of –10 dBm.

Generally speaking, a batteryless approach requires ultra-low-power circuits to be designed in order to optimize system performance. This is especially true for the RF front-end, which is the most power-hungry block of the platform. Accordingly, a current consumption of just 1 mA with a 1-V supply voltage (i.e. 1-mW power supply) were targeted for the front-end design.

As already explained, the adopted operating scheme is based on a procedure (charge & burst) in which short bursts of transmitted/received data are separated by long idle periods, during which energy is collected from a low-level power source (electromagnetic waves in our case). Assuming that energy is harvested with a rate of about 1 μW, a duty cycle of 1‰ is needed to supply the RF front-end with a 1-mW power. Incidentally, this means that the average data rate of the system is 1000 times lower than the instantaneous one. On the other hand, typical wireless sensor network applications require data rate of at least a few Kbps. Accordingly, an instantaneous data rate of a few Mbps is to be achieved by design. Concerning this, it should be noted that modulation at the TX side is performed by merely switching on and off the output buffer so as to generate an OOK-modulated signal. In such a case, the TX data rate is mainly limited by the output buffer switching speed. Therefore, Mbps data rates can be easily achieved by the TX in a sub-micrometer CMOS technology. Conversely, RX data rate performance is more critical. Indeed, it calls for a careful design of the PLL which should be able to track the fast frequency variations of its FSK-modulated reference. A high-bandwidth (6 MHz) PLL was designed to achieve a receiver data rate up to 5-Mbps. As a result, a nominal reference frequency of 305-MHz

was chosen to ensure loop stability [51] and minimal residual ripple at the data detection node.

Moreover, the PLL start-up time has to be minimized. This allows reducing the transceiver latency at the beginning of each operating cycle, hence optimizing the system energy efficiency.

Finally, the PLL noise performance has to be taken into account since it affects the minimum frequency difference, which is detectable by the FSK demodulator. Indeed, as well known, in a FSK modulation scheme, data are transmitted by exploiting two different carrier frequencies. Increasing the frequency spacing makes demodulation easier for the receiver. However, a greater frequency spacing leads to a higher transmitted signal bandwidth for a given data rate. Thus, the spectral efficiency reduces. For this design a minimum detectable frequency difference of 3 MHz was targeted.

2.3.1 Limiter

The limiter is the RF front-end input stage and sets the receiver sensitivity, i.e. the minimum input power required to perform data demodulation. As a matter of fact, it is connected to the PLL-based FSK demodulator through a frequency divider, which is a digital circuit. Therefore, proper demodulation can only be accomplished if a rail-to-rail output signal is produced by the limiter. Thus, achieving a sufficient gain to guarantee the targeted receiver sensitivity (-30 dBm) is the main design gaol. Of course, keeping the current consumption as low as possible is a design constraint as well. Moreover, the limiter must be able to operate at a relatively high frequency of 915 MHz.

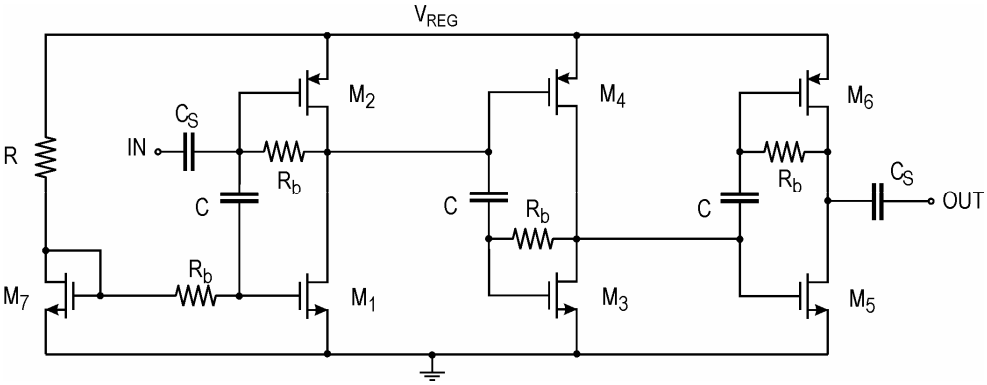


Fig. 2.33. Schematic of the limiting amplifier.

A 3-stage class AB topology was chosen to implement the limiting amplifier as shown in Fig. 2.33. Each stage is arranged in order to exploit a push-pull operating scheme for improved gain. Incidentally, the adopted topology at DC is equivalent to 3 cascaded current mirrors. This allows easy biasing through a single current reference.

The high operating frequency calls for a careful design. Small-in-size transistors (M_1-M_6) were used in order to improve RF performance. Channel length was set to the minimum value allowed by the used technology (i.e. 90-nm), whereas the channel width was set to 600 nm and 1.2 μm for NMOS and PMOS transistors, respectively. Moreover, bias resistors R_b were implemented by exploiting MOS transistors operating in triode region. This solution allows achieving high resistance values (> 100 KΩ) using a very small silicon area. This results in a reduced parasitic capacitance at the gain nodes of the amplifier for improved RF performance. Concerning this, note that capacitors C and C_S should be large enough to be shorted at the operating frequency. However, their value cannot be increased without burdening the amplifier performance. Indeed, the

higher the used capacitance values, the larger the related parasitic capacitances, which worsen the RF performance of the amplifier. Therefore, a fair trade-off is needed. Accordingly, capacitors of values 40 fF and 50 fF were used to implement C and C_S, respectively. Fig. 2.34 shows the simulated voltage gain of the limiting circuit. As can be seen, the limiter provides a voltage gain of 44 dB at 915 MHz while drawing a 70-μA current from a 1-V supply voltage. This performance translates into a sensitivity of about –30 dBm.

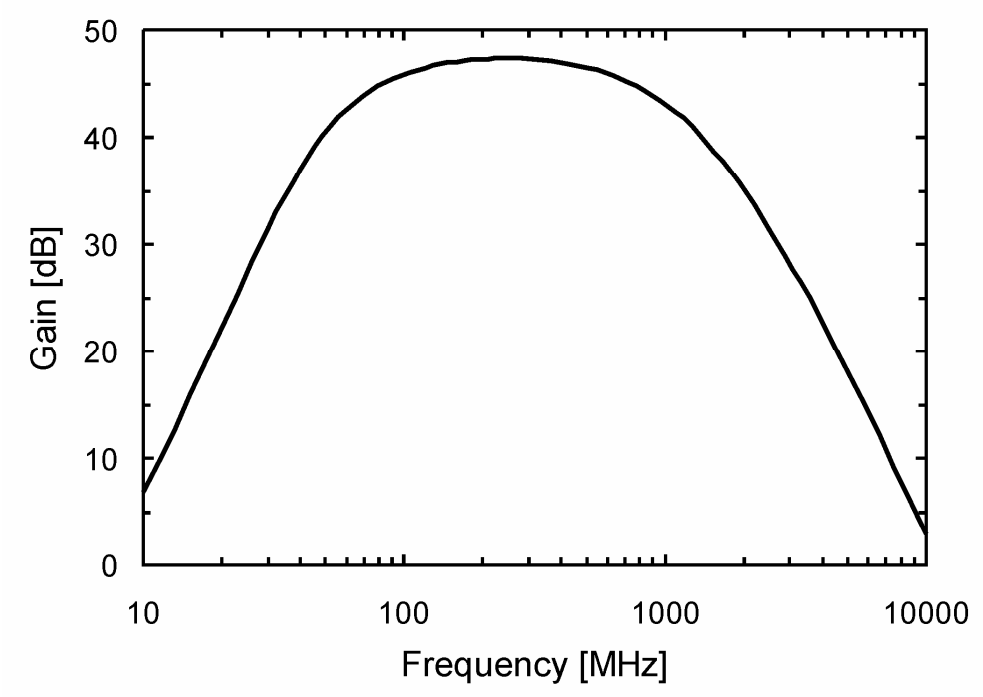


Fig. 2.34. Simulated voltage gain of the limiter.

2.3.2 Frequency dividers

The proposed RF front-end requires two frequency dividers. The first one follows the limiting amplifier, while the second one is used in the PLL feedback

path. The first divider is exploited to lower the frequency of the square wave that the limiter provides amplifying the incoming RF signal. Then, the divider output signal is fed to the input of the PLL which performs data recovery and transmission carrier synthesis.

Concerning this, it should be noted that the reference frequency of the PLL has to be high enough compared to the loop bandwidth (set according to the data rate requirements) both for stability issues [51] and to ensure minimal residual ripple at the data detection node. On the other hand, increasing the reference frequency of the PLL implies higher power consumption. Therefore, a careful choice of the division ratio of the frequency divider following the limiting circuit is needed. For this design, a divide-by-three circuit was used as first frequency divider, so that a 305-MHz reference frequency is provided to the PLL input. This divider exploits two master salve D flip-flops with an AND gate as shown in Fig. 2.35.

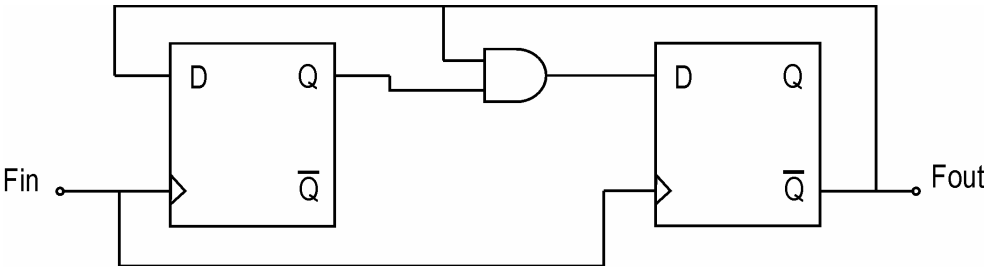


Fig. 2.35. Block diagram of the divide-by-three circuit.

Each flip flop was designed exploiting a *true single-phase clock* (TSPC) topology (Fig. 2.36) with the aim of minimizing the power consumption.

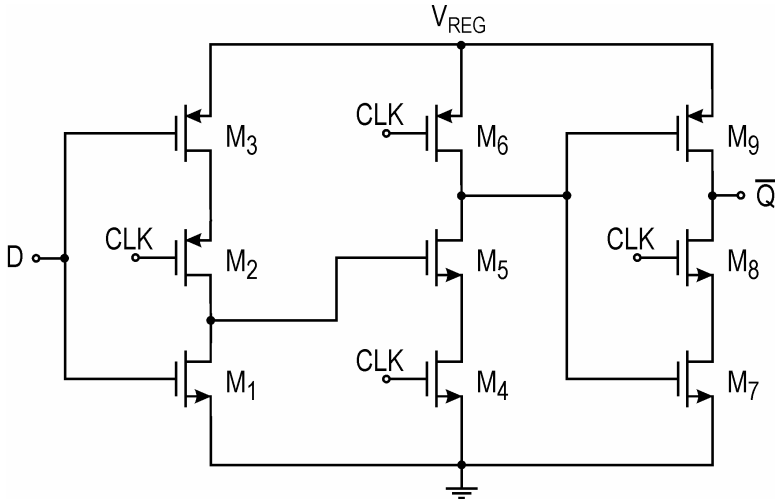


Fig. 2.36. Schematic of the TSPC D flip flop.

As regards the frequency divider used in the PLL feedback path, it was designed in order to obtain an transmission carrier which lies in the 2.45-GHz ISM band. This task was accomplished through a divide-by-eight circuit, which consists of three divide-by-two circuits each implemented using a TSPC D flip-flop as shown in Fig. 2.37.

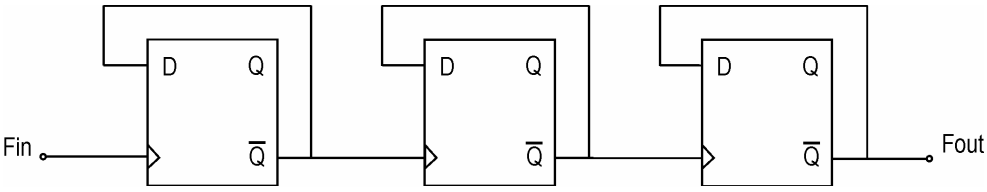


Fig. 2.37. Block diagram of the divide-by-eight circuit.

Thanks to the chosen topologies, a very low current consumption was achieved despite the high switching speed. Specifically, the simulated current consumption is of 20 μA (for a 915-input signal) and 30 μA (for a 2.45-GHz input signal) for the divide-by-three and divide-by-eight circuits, respectively.

2.3.3 Phase frequency detector and charge pump

As well known a PLL is a feedback system which operates on the excess phase of nominally periodic signals [52]. The phase frequency detector (PFD) and the charge pump (CP) are key components of such a system. The PFD detects the phase difference between the reference and feedback signals and outputs proper control signals to the charge pump. The latter turns these signals into current pulses, which allow changing the VCO control voltage and therefore its oscillation frequency. In this design, the high frequency of the reference and feedback signals (305 MHz) requires fast switching speed PFD and charge pump to be implemented. A simplified schematic of the designed phase frequency detector is shown in Fig. 2.38. A dynamic-logic approach was adopted to comply with the high frequency of its input signals with a low current consumption.

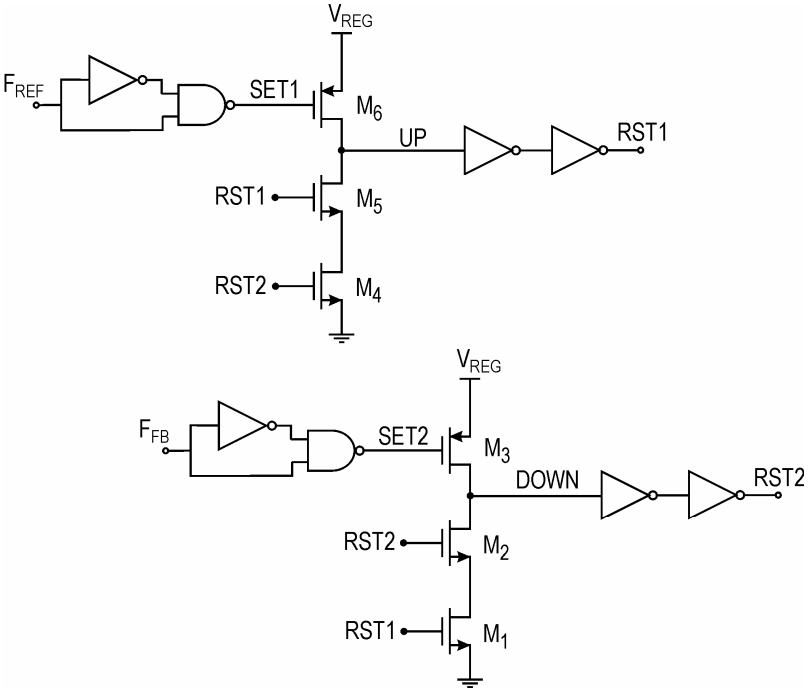


Fig. 2.38. Schematic of the phase frequency detector (PFD).

The operating principle of the proposed PFD is quite simple (Fig. 2.39). As the reference (feedback) signal goes high, *SET1* (*SET2*) exhibits a negative pulse, which is produced through a NAND gate and a delay chain. Such negative pulse enables transistor M_6 (M_3) to set *UP* (*DOWN*) to logic level "1". This level is hold until both *UP* and *DOWN* go high. Afterwards, they are reset to logic level "0" through transistors M_4-M_5 and M_1-M_2, respectively. Note that, the PFD dead zone is avoided by allowing enough delay (≈ 100 ps) between *UP* and *DOWN* signals and the related PFD reset signals (i.e. *RST1* and *RST2*). This delay was implemented through two cascaded CMOS inverters. A CMOS logic was also exploited for the design of the NAND gates.

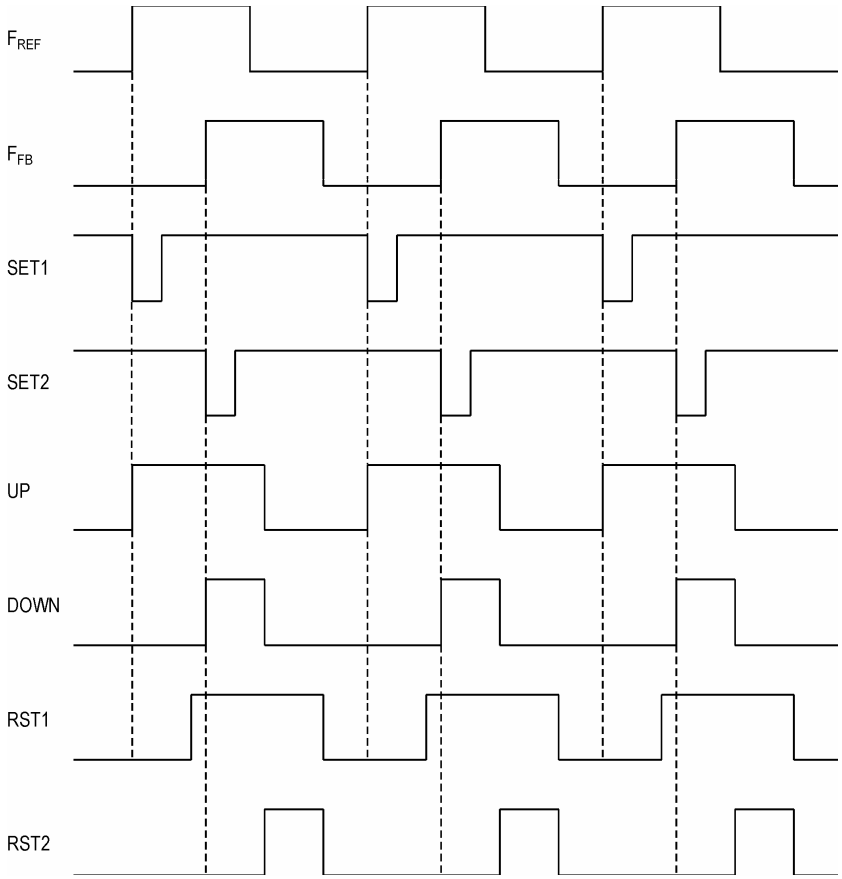


Fig. 2.39. Operating scheme of the proposed PFD.

The adopted solution allows achieving high switching speed with a low power consumption. Indeed, the simulated current consumption of the PFD is 20 μA. The PFD drives the charge-pump circuit, which basically consists of two switching current sources that pump charge into or out of the loop filter according to the *UP* and *DOWN* signals. As well known, the mismatch between the charging and discharging currents causes reference spurs at the PLL output. However, in a PLL-based FSK receiver, any undesired change of the VCO oscillation frequency turn out to be noise, which lowers the signal-to-noise ratio (SNR). Therefore, a charge pump with good current-matching performance has to be designed. Achieving a current consumption as low as possible is a design constrain as well. To best fit these requirements, a single-ended cascode topology was adopted (Fig. 2.40). Transistors M_1-M_{10} form current mirrors, which are cascaded to increase the output impedance so that the output current is less sensitive to the output voltage variations.

A drain switching solution was chosen for improved speed performance. Switches $M_{11}$and M_{12} were sized in order to minimize the current mismatch and the turn-on time. Accordingly, a 90-nm channel length was adopted for both transistors, while a channel width of 1 μm and 3 μm was chosen for M_{11} and M_{13}, respectively. Furthermore, it is worth nothing that a low-voltage topology was used for the cascode current mirrors in order to achieve a larger output voltage swing. As above mentioned, designing a fast-settling PLL is mandatory in order to optimize the transceiver energy efficiency. This constrain calls for a charge pump peak current high enough. Indeed, increasing the charge pump current allows extending the PLL bandwidth, thus lowering its settling time. This results in a

reduction of the transceiver latency at the beginning of each operating cycle besides increasing the maximum receiver data rate. For this design the charge pump peak current was set to 100 μA. Finally, the charge pump bias current (10 μA) is provided through a 44-KΩ resistance, which is split into two resistors (R_1 and R_2) in order to easily obtain the bias voltage for transistor M_6. Similarly, resistor R_3 (15 KΩ) was sized in order to provide the proper bias voltage to the gate terminal of M_7.

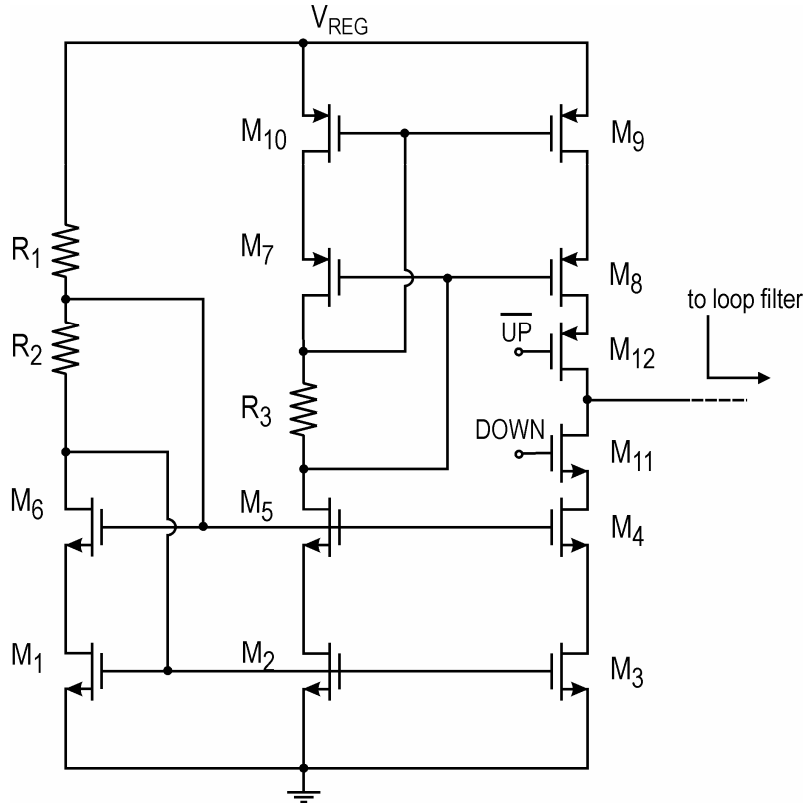


Fig. 2.40. Schematic of the charge pump (CP).

The simulated input-output characteristic of the PFD/CP block is reported in Fig.2. 41.

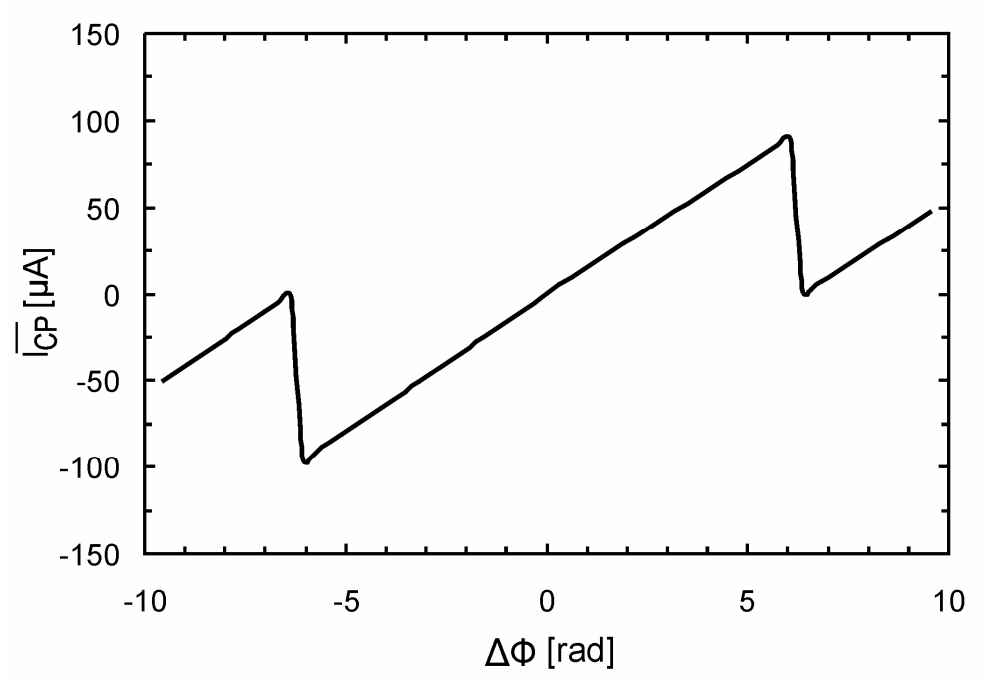


Fig. 2.41. Simulated PFD/CP input-output characteristic.

2.3.4 Voltage controlled oscillator

The voltage controlled oscillator (VCO) is one of the most critical building blocks of the PLL-based RF front-end. Indeed, it strongly affects the receiver noise performance besides being the most power-hungry component of the PLL. Hence, a LC topology was exploited for optimum trade-off between current consumption and noise performance (Fig. 2.42). Furthermore, the adopted duty-cycled operating scheme requires a VCO with a fast start-up time to be designed in order to reduce the RF front-end latency at the beginning of each operating cycle.

The VCO start-up time may be reduced either by increasing its bias current or by using an inductor with an equivalent shunt loss resistance (ωQL) as high as possible. However, this would result in a sub-optimum design concerning the

phase noise performance. Indeed, for a given current consumption an optimum inductor exists which minimizes the phase noise. On the other hand, the VCO phase noise performance cannot be neglected, since it is the main contributor to the overall noise of the receiver. Therefore, once fixed the VCO bias current, according to a well defined current budget (200 μA), a trade-off between noise performance and start-up time has to be achieved by a proper sizing of the inductor.

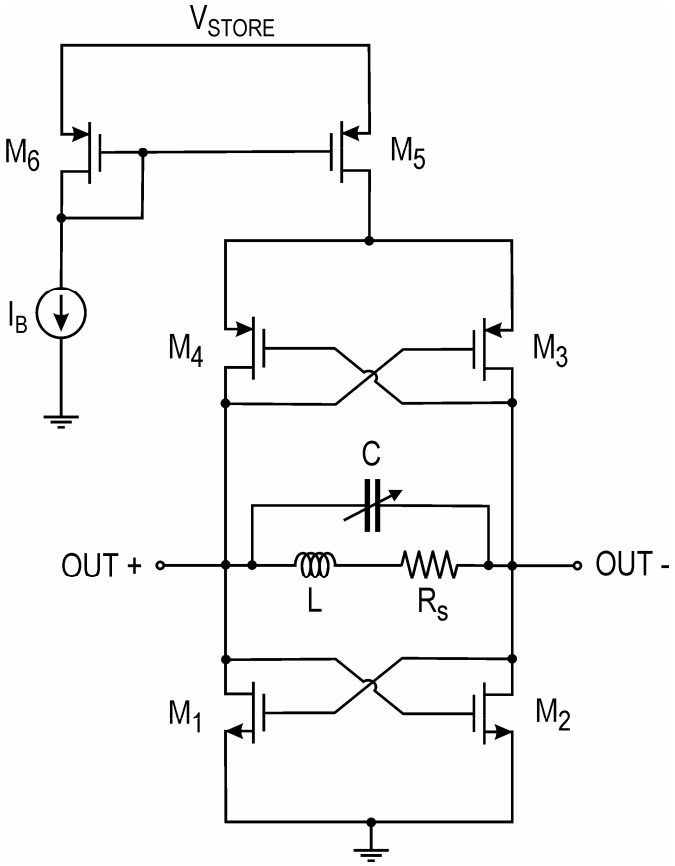


Fig. 2.42. Schematic of the voltage controlled oscillator (VCO).

Accordingly, a spiral inductor of about 9 nH was used. It is a symmetrical spiral inductor with five turns and an inner radius of 78 μm. It exhibits a relatively

high quality factor of 16 at 2.4 GHz. In addition, the VCO was designed to be directly supplied by the unregulated voltage at the storage capacitor (V_{STORE}) to the aim of lowering the noise contribution of the power management circuit. Concerning this, a 1-µm channel length was chosen for transistors M_5 and M_6, in order to make the VCO bias current less sensitive to the supply voltage variations. The sizing of the cross coupled transistor pairs plays an important role in the reduction of the current consumption. For oscillation the following condition is to be satisfied [53]:

$$g_{m1,2} + g_{m3,4} > \frac{2}{R_L} \tag{2.13}$$

Were R_L is the shunt loss resistor of the inductor (i.e. $R_L = \omega QL$). For a given bias current, increasing the transistor size results in a higher transconductance, till strong inversion operation is guaranteed. Sizes of the cross coupled pairs were chosen to be 40µm/90nm and 80µm/90nm for the NMOS and PMOS transistors, respectively.

The simulated VCO phase noise is -103 dBc at 1-MHz offset from the 2.45-GHz carrier, while the start-up time is lower than 100 ns. MOS varactors were used to implement the variable capacitance C. The VCO tuning range spans from 2.3 GHz to 2.6 GHz, as depicted in Fig. 2.43. Note that, it was designed to properly exceed the targeted ISM bandwidth (2.4-2.5 GHz) in order to take into account the process statistics.

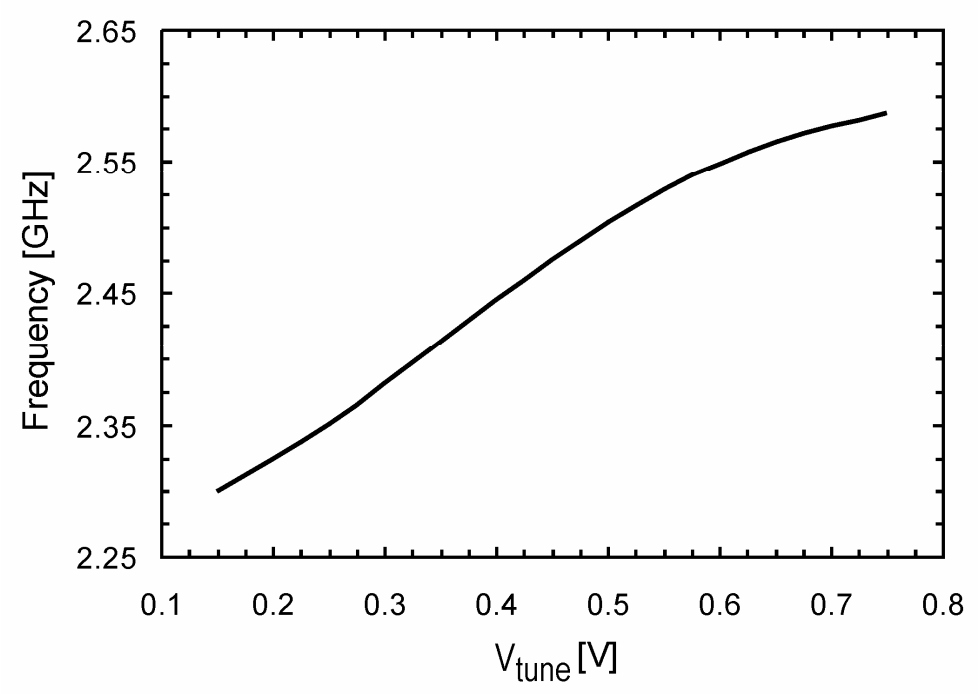


Fig. 2.43. VCO tuning range.

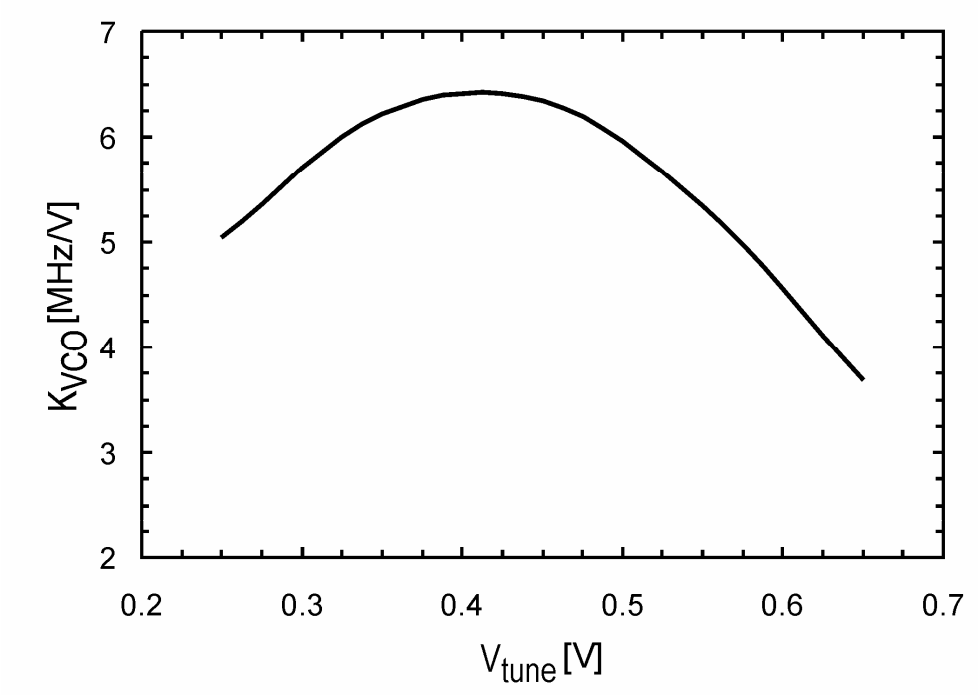


Fig. 2.44. Simulated frequency gain (K_{VCO}) of the VCO.

The simulated VCO frequency gain (K_{VCO}) is reported in Fig. 2.44. This is a very important parameter, which affects the receiver performance. Indeed, in a PLL-based FSK demodulator the amplitude of the output signal is inversely proportional to the K_{VCO} of the oscillator. Therefore, a K_{VCO} as low as possible is needed for improved SNR performance. The simulated K_{VCO} is of about 630MHz/V at 2.45 GHz.

Finally, a SCL-to-CMOS converter (Fig. 2.45) is connected to the VCO output in order to obtain a rail-to-rail signal, which is required by the following digital circuit (i.e. the divide-by-eight circuit). Devices M_1 and M_2 are connected to the NMOS transistors of the VCO core in a mirror-like configuration which allows a low current consumption (100 μA) to be achieved.

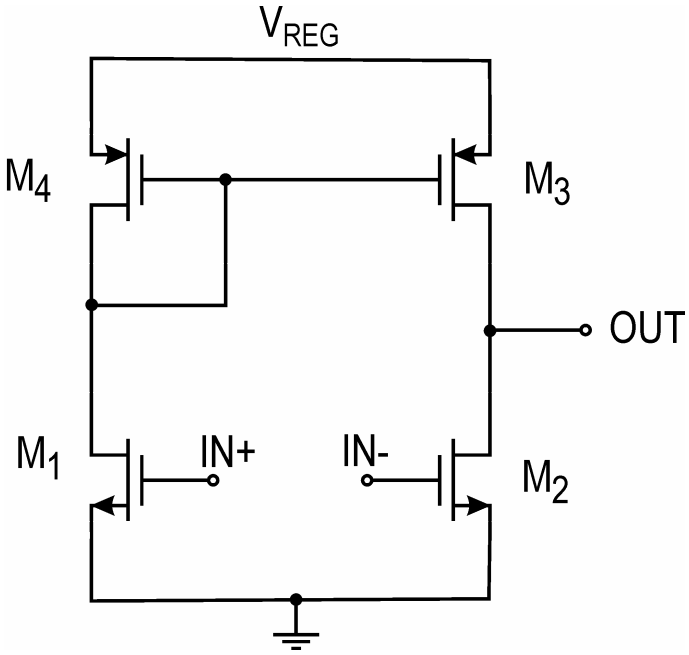
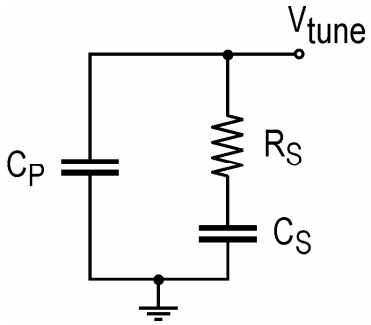


Fig. 2.45. Schematic of the SCL-to-CMOS interface.

2.3.5 Loop filter

The design of the PLL loop filter is crucial for the operation of the whole system. Indeed, the PLL filter is needed to remove the high frequency components coming from the charge pump, which would appear as spurious signals at the VCO output. Furthermore, the loop filter sets the PLL bandwidth and then the maximum achievable data rate. It also affects the PLL stability. For this work, a second order on-chip loop filter was designed. A system analysis was performed in Matlab for proper design. In particular, the loop filter was designed to achieve a 6 MHz bandwidth with a phase margin of about 50°. This results in a maximum receiver data rate of about 5 Mbps. The schematic of the designed loop filter along with the list of its component are reported in Fig. 2.46.



Component	Value
C_P	1.64 pF
C_S	11.5 pF
R_S	5.6 KΩ

Fig. 2.46. Schematic of the on-chip loop filter.

2.3.6 Output buffer

The uplink data exchange is performed by exploiting the 2.45-GHz-band carrier, which is synthesized by the PLL-based receiver from the incoming 915-MHz signal. Specifically, the 2.45-GHz carrier is fed to the output buffer,

which performs the OOK modulation of the input carrier according to the output data stream. The schematic of the designed output buffer is shown in Fig. 2.47. It consists of four cascaded inverter stages.

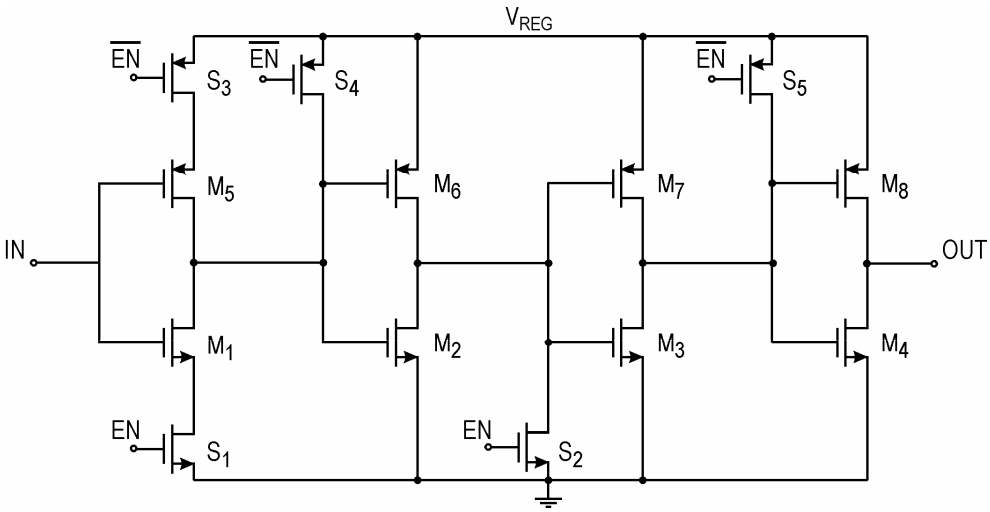


Fig. 2.47. Schematic of the output buffer.

The OOK modulation of the transmission carrier is accomplished by enabling and disabling the output buffer through switches S_1-S_5. The circuit was designed to provide an output power of –10 dBm at 2.45 GHz. The simulated current consumption is 460 μW.

2.3.7 RF front-end simulated performance

The simulated performance of the RF front-end are summarized in Table 2.2. The receiver exhibits a current consumption of 500 μA, whereas the output buffer draws 460 μA from a 1-V supply voltage as long as it provides an output power of about –10 dBm. Therefore, the overall current consumption of the RF front-end is 960 μA.

Table 2.2. Simulated performance parameters of the RF front-end.

Parameter	Performance
RX operating frequency	902-928 MHz
Downlink modulation	FSK
Minimum detectable frequency difference	3 MHz
Input sensitivity	-30 dBm
Receiver data rate	up to 5 Mps
RX current consumption	500 µA
TX operating frequency	2.405-2.475 GHz
Uplink modulation	OOK
Maximum transmitted power	-10 dBm
Transmitter data rate	up to 10 Mbps
TX buffer current consumption	460 µA

The receiver sensitivity is –30 dBm and the minimum detectable frequency difference is 3 MHz. The latter performance can be estimated by evaluating the SNR at the data detection node (i.e. the VCO control terminal). Fig. 2.48 shows the noise power spectral density of the VCO control voltage including the noise contribution of the power management unit.

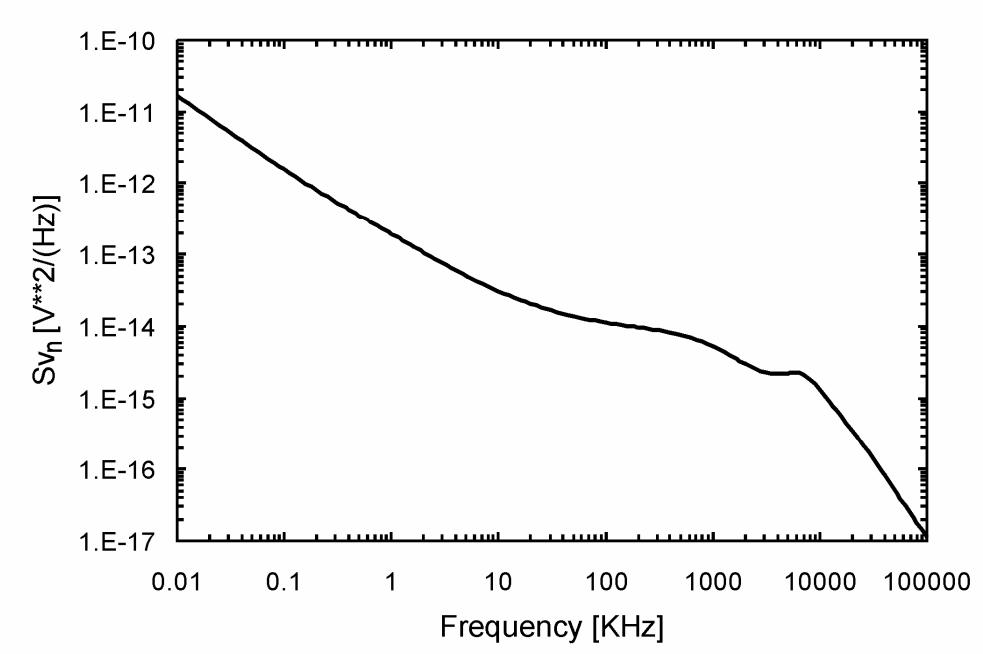


Fig. 2.48. Simulated noise power spectral density of the VCO control voltage (f_{IN} = 915 MHz, P_{IN} = –30dBm).

The SNR at the receiver output reads (see Appendix B):

$$SNR \approx \frac{1}{4} \cdot \left(\frac{8}{3}\right)^2 \cdot \left(\frac{\pi \cdot \Delta f}{K_{VCO}}\right)^2 \cdot \frac{1}{\int_B Sv_n(f) \cdot df} \tag{2.14}$$

where Δf is the frequency spacing between the two carriers of the adopted BFSK modulation scheme, K_{VCO} is the VCO frequency gain and B is the signal bandwidth. According to (2.14), at the minimum targeted frequency difference (Δf = 3 MHz), assuming a signal bandwidth of 10 MHz and a carrier frequency of 915 MHz, the simulated SNR is about 20 dB.

Fig. 2.49 illustrates the transient response of the receiver, that is the transient behaviour of the VCO control voltage while a frequency modulation is imposed to the receiver input signal. Here the input frequency is step-wise shifted

by 3 MHz, from 913.5 MHz to 916.5 MHz. The simulated settling time is of about 200 nsec. This results in a maximum receiver data rate of 5 Mbps.

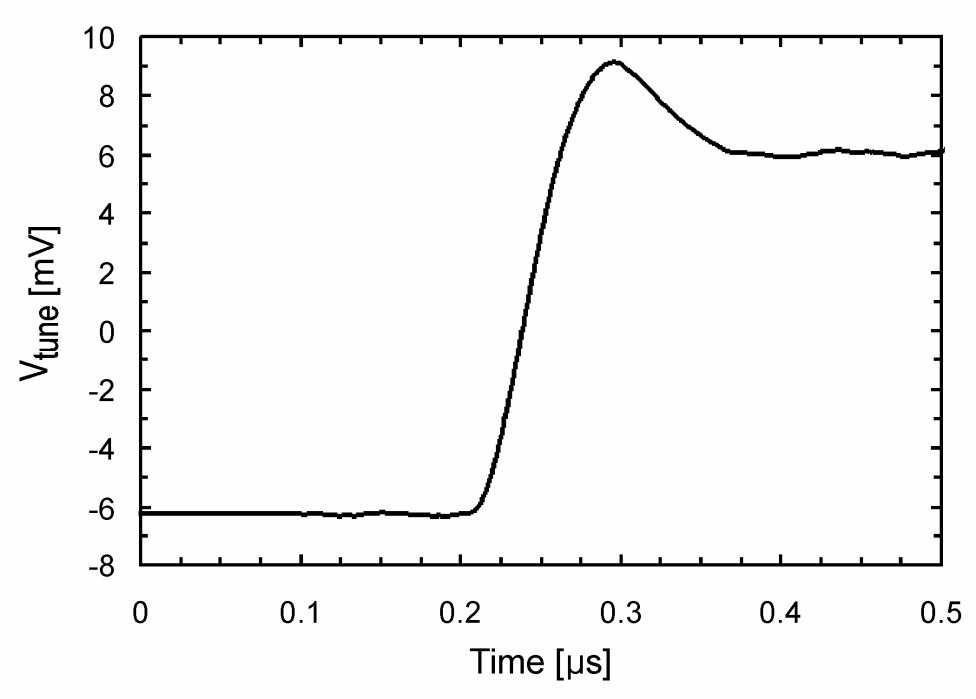


Fig. 2.49. Transient response of the PLL based receiver (ac-coupled).

As already mentioned, the OOK modulation of the 2.45-GHz-band carrier is performed by enabling and disabling the output buffer. Therefore, the maximum transmission data rate is set by the buffer switching speed. The simulated switching time is lower than 10 ns. Thus, a transmission data rate up to 10 Mbps may be supported. Fig. 2.50 displays the buffer output while its enable terminal is driven by a square wave with a period of 200 ns corresponding to a 10-Mbps data rate.

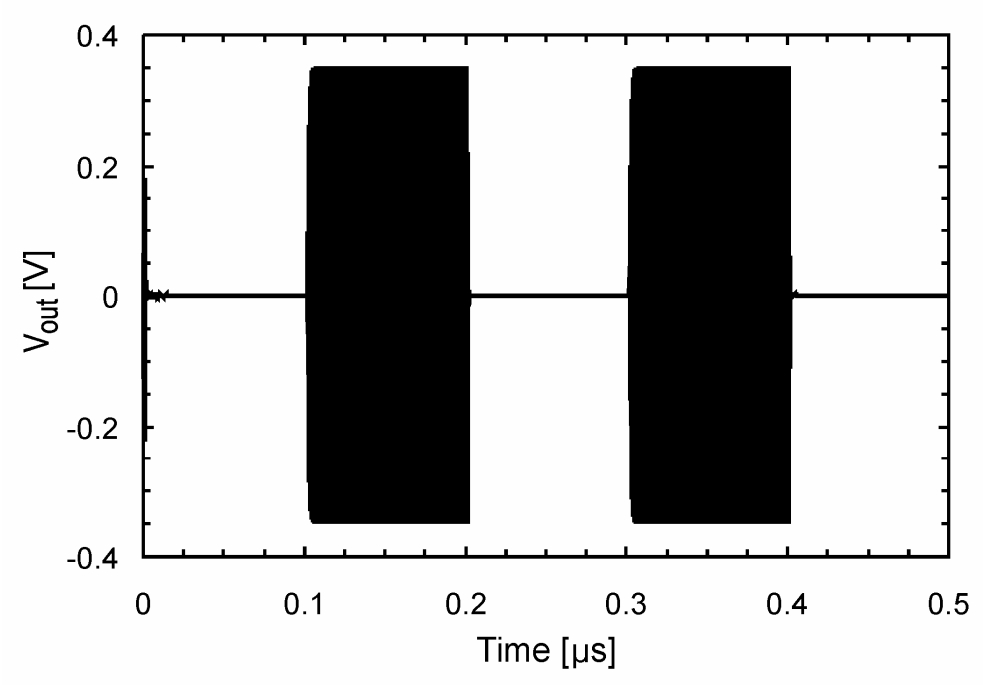


Fig. 2.50. OOK-modulated buffer output voltage at 10 Mbps (f = 2.45 GHz, P_{out} = –10 dBm).

Chapter III

Experimental results

The proposed batteryless RF transceiver was fabricated in a 90-nm CMOS technology by TSMC, which provides designer with 7 copper interconnect layers (thick-copper option for the topmost one), MIM capacitors, and high-Q inductors. First, a prototype of the RF energy harvesting system stand-alone was fabricated and tested in order to validate the proposed circuital solution and the developed design algorithm. Then, a second prototype was manufactured, which implements the whole batteryless platform. It includes the RF harvester, the power management unit and the PLL-based RF front-end. In this second *chip* the RF energy harvesting module doesn't comprise the matching network, which was implemented on board at the RF input of the integrated circuit (IC). It is worth noting that such matching network is shared by the harvester and the RF front-end. An exhaustive characterization of both the whole batteryless transceiver and its functional building blocks was performed. The obtained experimental results are here reported.

3.1 RF harvester stand-alone

A micrograph of the prototype of the stand-alone RF energy harvesting system (including the self-compensated rectifier and the matching network) is shown in Fig. 3.1. The overall chip size is 1.31 mm × 1.03 mm, while the area occupation of the self-compensated rectifier is 950 μm × 200 μm.

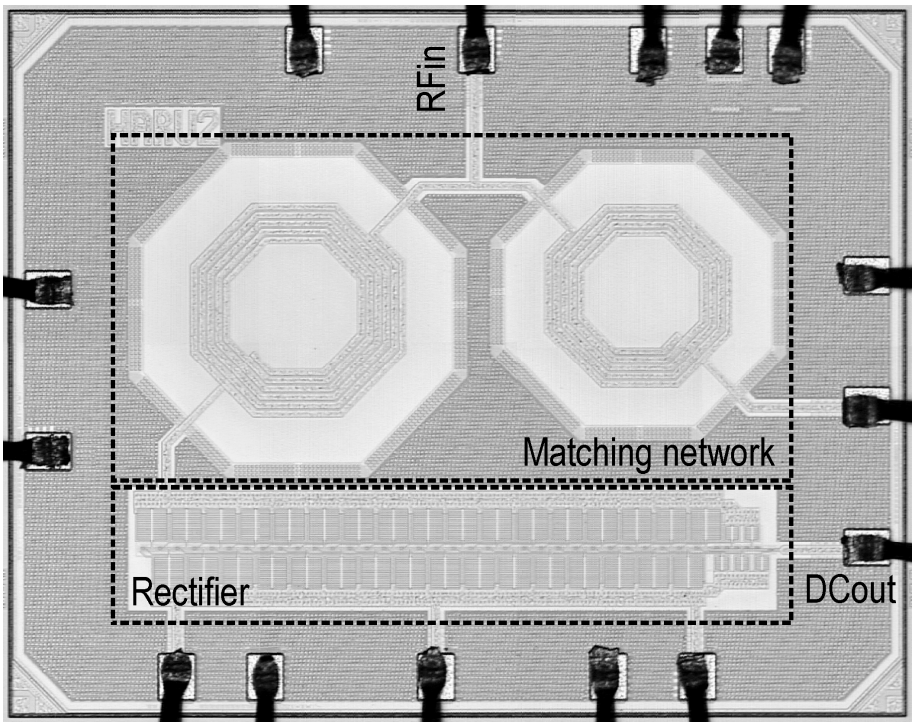


Fig. 3.1. Micrograph of the RF energy harvesting system IC.

The device was wire-bonded to a FR4 printed circuit board (PCB) and tested with a single-tone continuous-wave (CW) 50-Ω source with a nominal frequency of 915 MHz. A photograph of the test board is shown in Fig. 3.2.

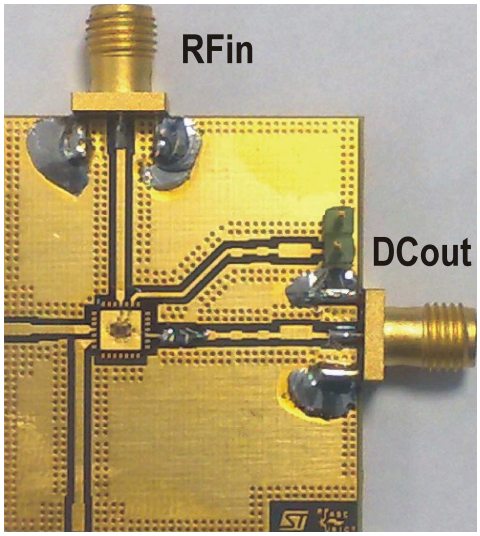


Fig. 3.2. Test board.

Fig. 3.3 shows the measured output DC voltage as a function of the available input power for different load resistances.

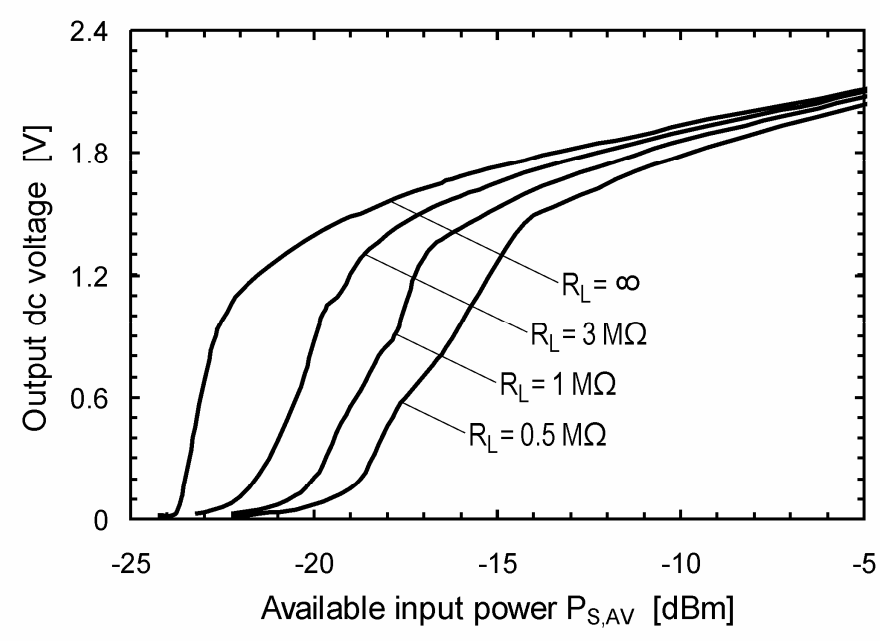


Fig. 3.3. Measured output DC voltage versus available input power for different load resistance values ($C_L = 47$ nF, $f = 915$ MHz, single-tone CW input).

The designed RF harvesting system exhibits a remarkably low input power threshold. Indeed, it is able to supply a 1-V output voltage to a purely capacitive load with an available input power as low as –22.44 dBm (5.7 μW). According to Friis equation, this power level translates into an excellent free-space distance of 31 m from the radiating source, assuming a 4 W (36 dBm) EIRP and a 3-dB receiver antenna gain. When loaded by a 1-MΩ resistance, the circuit can deliver the nominal output voltage of 1.2 V with an available input power of -17.27 dBm (18.7 μW) at the antenna connector, corresponding to a free-space distance of 17 m from a 4-W source. The harvester PCE is reported in Fig. 3.4 as a function of the available input power for different load resistances. Under nominal conditions (1.2°V output on a 1-MΩ load), the circuit attains a PCE of 7.7%, which closely agrees with the simulated one.

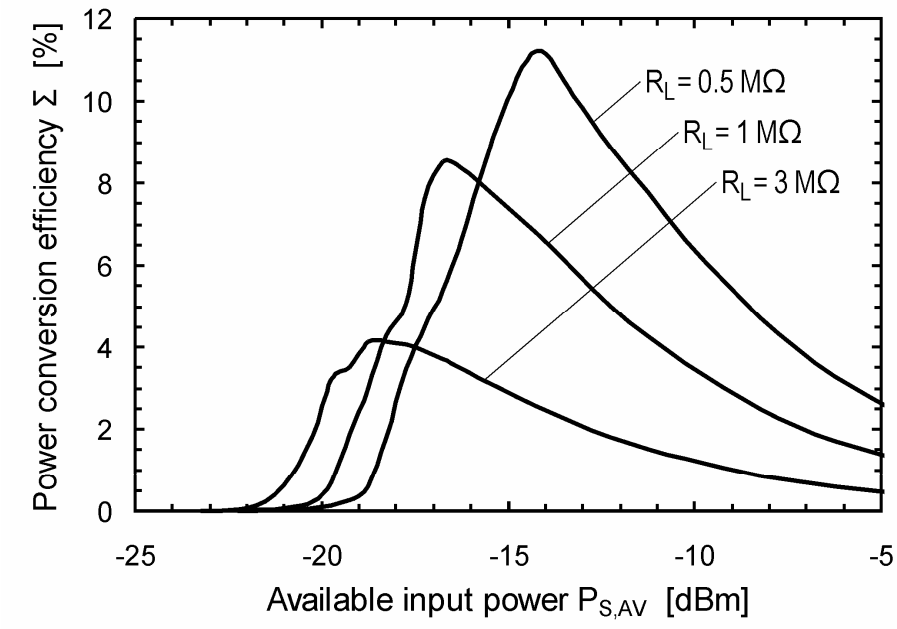


Fig. 3.4. Measured PCE versus available input power for different load resistance values (C_L = 47 nF, f = 915 MHz, single-tone CW input).

For an exhaustive characterization, the circuit was also tested by forcing its output to a given DC voltage and measuring the short-circuit output current at a given available input power. To this aim the circuit output was terminated on a semiconductor parameter analyzer. Following this procedure, the system was tested on a wide range of output voltages and input power levels as reported in Fig. 3.5.

This approach allows deriving the system steady-state performance with *any* resistive load. Indeed, by trivial post-processing of the measured data (Fig. 3.5), the output voltage can be estimated as a function of both the load resistance and the available input power, as represented by the contour plot in Fig. 3.6.

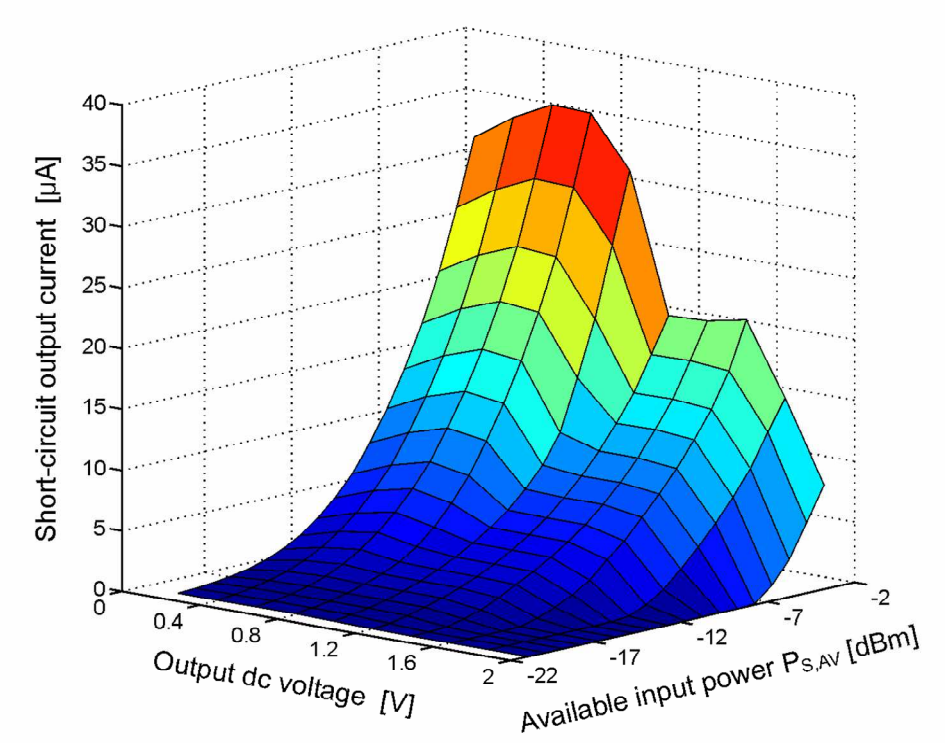


Fig. 3.5. Surface plot of the measured short-circuit output current versus available input power and output DC voltage ($f = 915$ MHz, single-tone CW input).

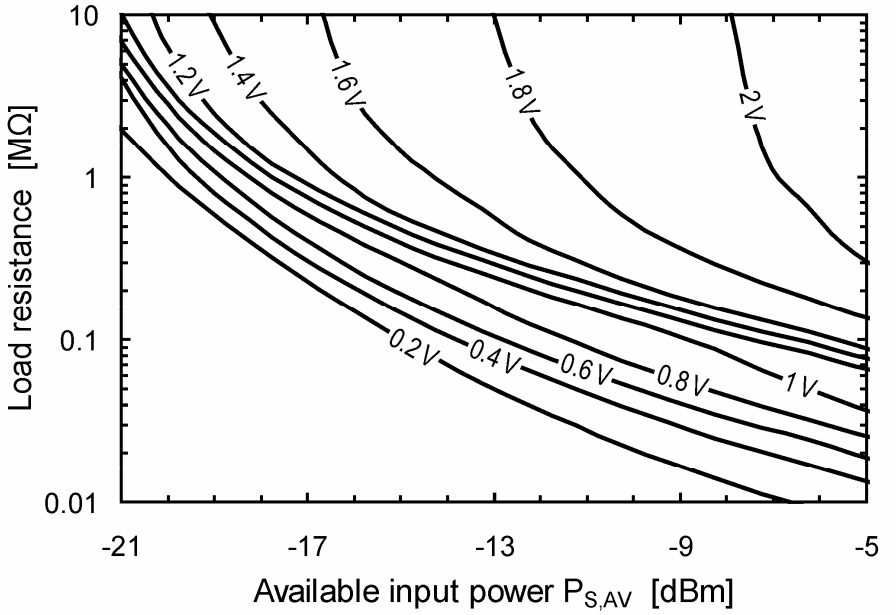


Fig. 3.6. Contour plot of the output DC voltage versus available input power and load resistance (f = 915 MHz, single-tone CW input).

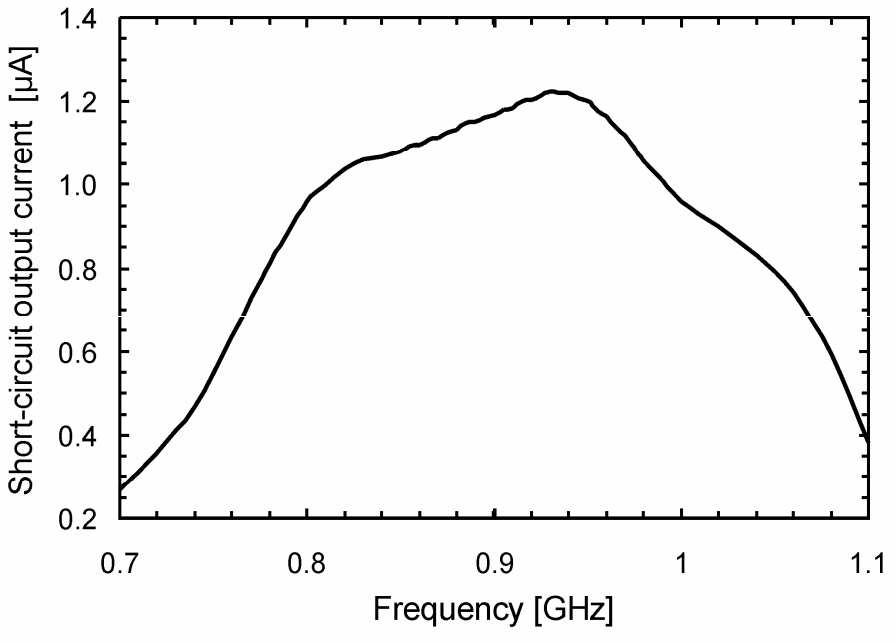


Fig. 3.7. Measured short-circuit output current versus input frequency (V_O = 1.2 V, $P_{S,AV}$ = –17.25 dBm, single-tone CW input).

The frequency response of the circuit is shown in Fig. 3.7. The device exhibits a sufficiently broad response, with a lower than 20% variation between 800 MHz and 1 GHz.

The transient response of the RF harvesting system was also investigated. To this aim, the 10% settling time of the output voltage was measured by applying a step envelope RF signal at the circuit input. The measured results are shown in Table 3.1 as a function of the available input power for different load conditions. The reported transient response is compatible with a duty-cycled power management strategy.

Table 3.1. Transient response of the RF harvesting system.

Available input power	Measured 10% settling time			
	$R_L = \infty$		$R_L = 1\ M\Omega$	
	C_L = 47 nF	C_L = 510 nF	C_L = 47 nF	C_L = 510 nF
-18.77 dBm	128 ms	1.42 s	156 ms	1.69 s
-18.27 dBm	105 ms	1.14 s	143 ms	1.56 s
-17.77 dBm	83 ms	916 ms	124 ms	1.39 s
-17.27 dBm	69 ms	762 ms	115 ms	1.22 s
-16.27 dBm	47 ms	520 ms	63 ms	684 ms

Finally, the stand-alone performance of the self-compensated rectifier was easily drawn from the overall system performance by de-embedding the available gain (G_A) of the matching network. According to this, the rectifier is able to supply a 1-V output voltage to a purely capacitive load with a very small available power of –24 dBm (4 μW or 70 mV voltage amplitude) at its input. The inherent

efficiency of the rectifier (Σ_R) is reported in Fig. 3.8 as a function of the available power at the input of the rectifier. At –18.83 dBm (13.1 μW or 130 mV voltage), the rectifier exhibits a Σ_R of 11% on a 1 MΩ load while delivering the nominal 1.2-V output voltage. This is the highest reported efficiency for a RF multi-stage rectifier in standard *analog* CMOS technology with such a low available input power. Even higher efficiency values are attained with larger input power levels and lower load resistances. For instance, a maximum Σ_R of 16.1% is achieved with a –15.83-dBm input, while delivering a 1.45-V output voltage to a 500-kΩ load resistance.

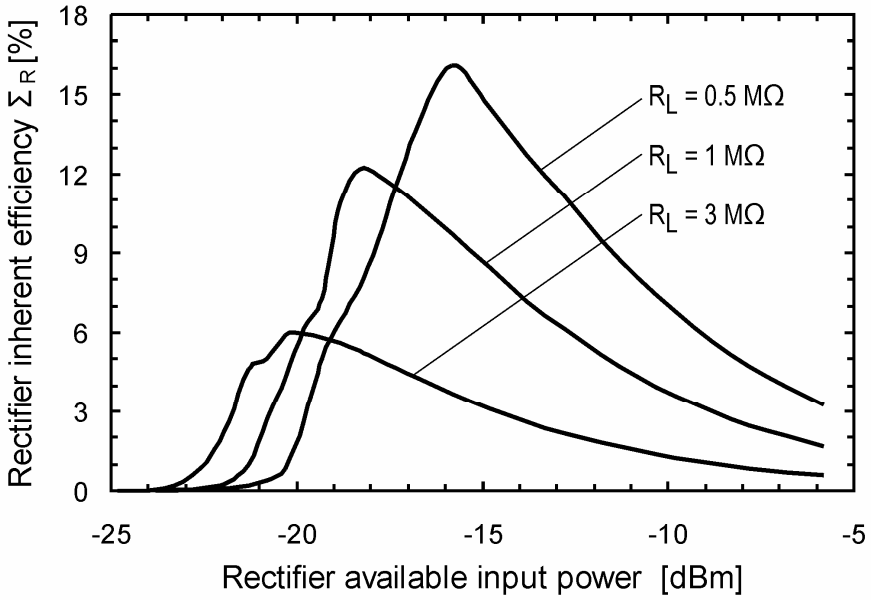


Fig. 3.8. Rectifier inherent efficiency (Σ_R) versus rectifier available input power for different load resistance values (C_L = 47 nF, f = 915 MHz, single-tone CW input).

Table 3.2 summarizes the performance of the designed self-compensated rectifier and compares it with previously published works.

Table 3.2. Rectifier's performance and comparison with the state of art.

Reference	This work	T. Le *et al.* 2008 [34]	H. Nakamoto *et al.* 2007 [32]	F. Kocer *et al.* 2006 [26]	T. Umeda *et al.* 2006 [31]	U. Karthaus *et al.* 2003 [30]
CMOS technology node	90 nm	0.25 µm	0.35 µm	0.25 µm	0.3 µm	0.5 µm
Typical threshold voltage	0.45 V	0.55 V	//	0.15 V	0.53 V	0.2 V
Operating frequency	915 MHz	906 MHz	953 MHz	450 MHz	950 MHz	869 MHz
Additional requirements	Deep *n*-well	Pre-charge phase is needed	//	Low-V_{TH} transistors are exploited	Auxiliary battery is needed	Schottky diodes are exploited
Minimum RF input power	-24 dBm V_O = 1 V R_L = ∞	-22 dBm V_O = 2 V R_L = ∞	-9 dBm V_O = 2.4 V	-18.6 dBm V_O = 1.2 V R_L = 1 MΩ	-14 dBm V_O = 1.5 V I_O = 400 nA	-20.1 dBm V_O = 1.5 V I_O = 950 nA
	-18.83 dBm V_O = 1.2 V R_L = 1 MΩ	-17.9 dBm V_O = 1.4 V R_L = 1.32 MΩ				
Rectifiers efficiency at minimum RF input power	11% [a]	9.2% [a]	15.4% [a]	10.4% [a]	1.5% [b]	14.5% [b]

(a) The rectifier available input power is considered for efficiency calculation thus including the input reflection (i.e. Σ_R is reported).
(b) The rectifier net input power is considered for efficiency calculation by deembedding the input reflection (i.e. η is reported).

3.2 Batteryless transceiver

A microphotograph of the prototype of the whole batteryless transceiver is shown in Fig. 3.9. The overall chip size is 1.4 mm × 1.1 mm.

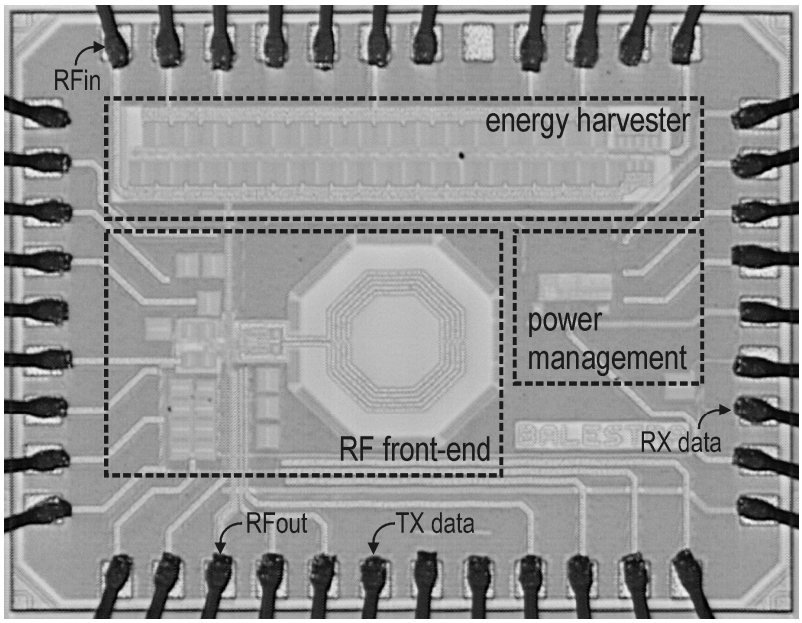


Fig. 3.9. Microphotograph of the batteryless transceiver IC.

The die was wire-bonded to a FR4 printed circuit board (PCB) and on-board semi-lumped matching networks were exploited at the input and output RF ports for 50-Ω testing. A photograph of the test board is shown in Fig. 3.10.

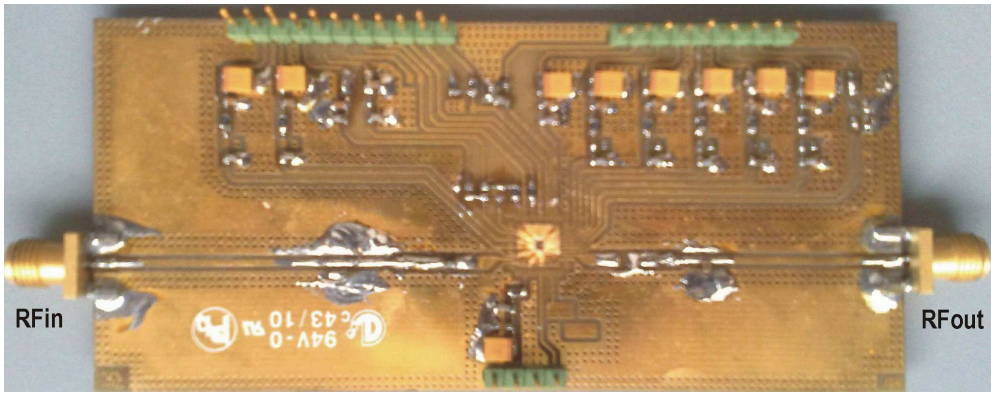


Fig. 3.10. Test board.

The input matching network (Fig. 3.11) was aimed at optimizing the energy harvester performance and basically reproduces that one integrated in the first prototype (Fig. 3.1), whereas the output matching network (Fig. 3.12) was implemented with the goal of maximizing the output power transfer to a 50-Ω load at 2.45-GHz.

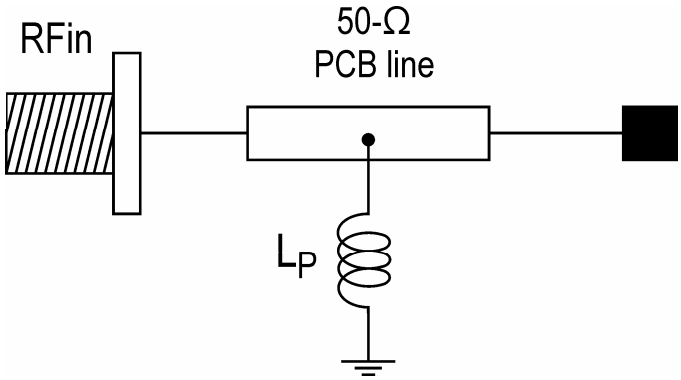


Fig. 3.11. On-board input matching network.

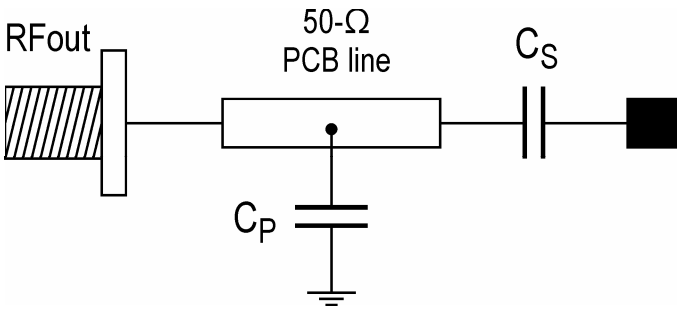


Fig. 3.12. On-board output matching network.

The test board was designed with the aim of performing an exhaustive characterization of both the whole system and its functional building blocks. The most meaningful results concerning the power management unit, the RF front-end and the whole transceiver are reported in the following sections. As regards the RF harvester, it was extensively characterized in the stand-alone configuration (Fig. 3.1) and the related measured performance are reported in the previous section. Concerning this, it is worth remembering that thanks to the adopted self-compensated topology a remarkably low input power threshold was achieved. Indeed, the RF harvester is able to deliver a 1.2-V output voltage along with a 1-μA current with an available input power as low as -17.75 dBm (16.8 μW).

3.2.1 Power management unit characterization

The power management unit characterization was performed by configuring the test board in Fig. 3.10 so as to implement the charge & burst procedure. The charge phase was emulated by charging a on-board 50-nF storage capacitor with a 1-μA current, which is roughly the DC current provided by the RF harvester in nominal operating conditions. To simulate the discharge phase a 20-pF capacitor

in parallel with a 1-KΩ resistor were connected to the voltage regulator output, so as to draw a 1-mA current from the 1-V regulated supply voltage. Plots in Figs. 3.13-3.16 demonstrate successful implementation of the charge & burst procedure. In detail, the waveforms of the enable signal (*EN*) and of the regulated (V_{REG}) and unregulated voltages (V_{STORE}) are shown in Figs. 3.13-3.14 during the charge and discharge phases, respectively. The turn-on ($V_{STORE(high)}$ = 1.68 V) and turn-off ($V_{STORE(high)}$ = 1.15 V) voltages (which are set by hysteresis comparator) are apparent. The turn-on and turn-off transient responses of the power management unit are displayed in Fig. 3.15 and Fig. 3.16, respectively. The measured turn-on and turn-off times of the voltage regulator are 300 ns and 400 ns, respectively. A so fast transient response allows maximizing the available time for the RF front-end operation.

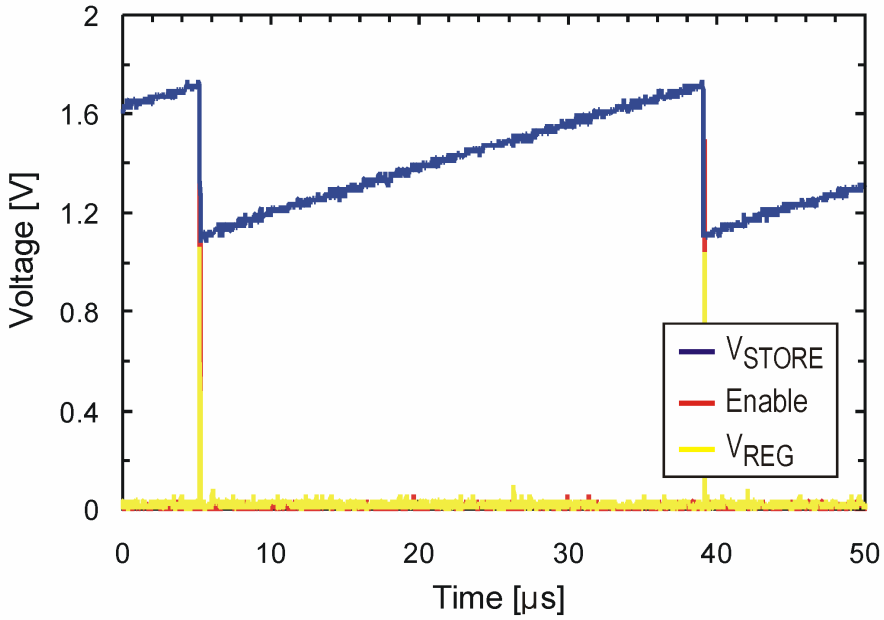


Fig. 3.13. Measured power management waveforms showing the charge phase (C_{STORE} = 50 nF, I_{CHARGE} = 1 µA, I_{LOAD} = 1 mA).

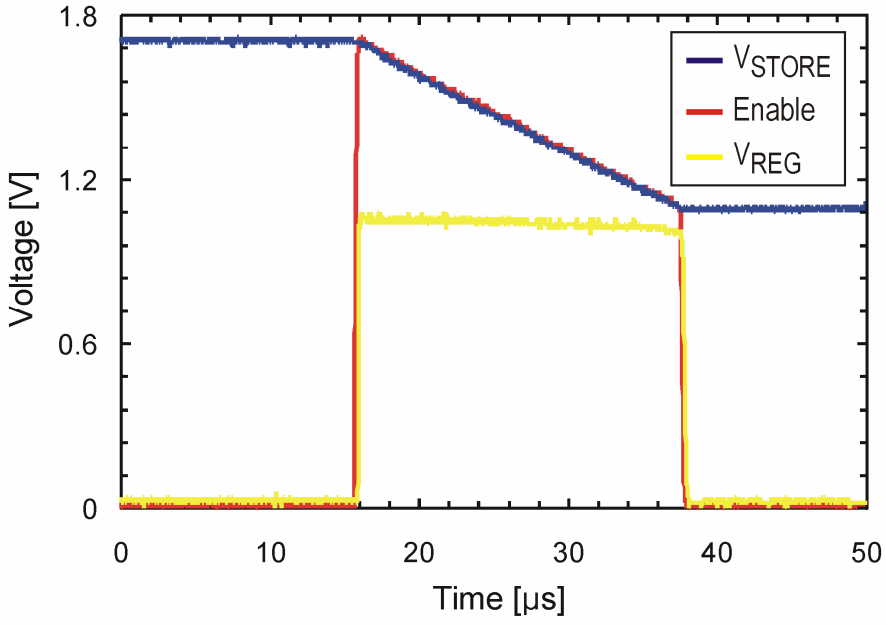


Fig. 3.14. Measured power management waveforms showing the discharge phase (C_{STORE} = 50 nF, I_{CHARGE} = 1 µA, I_{LOAD} = 1 mA).

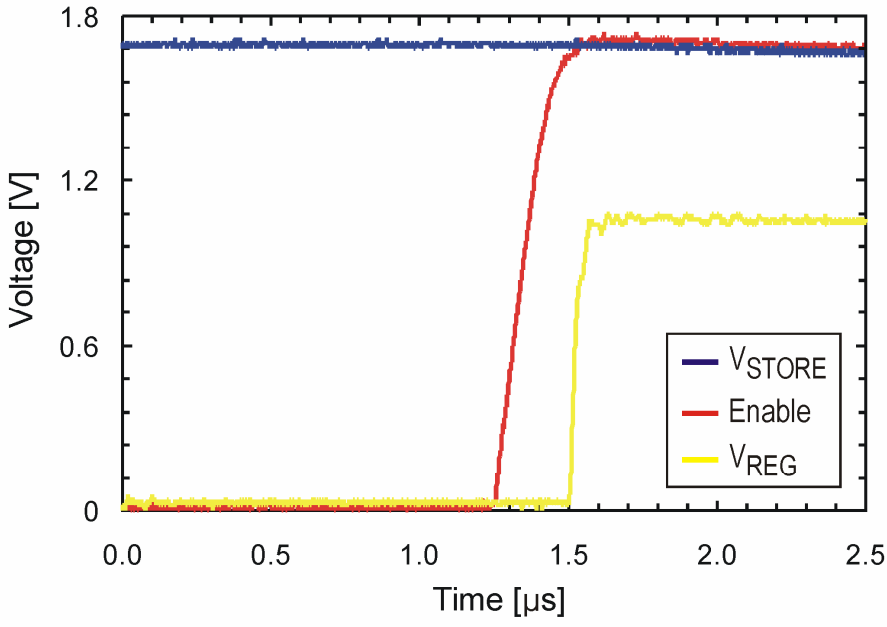


Fig. 3.15. Turn-on transient response (C_{STORE} = 50 nF, I_{CHARGE} = 1 µA, I_{LOAD} = 1 mA).

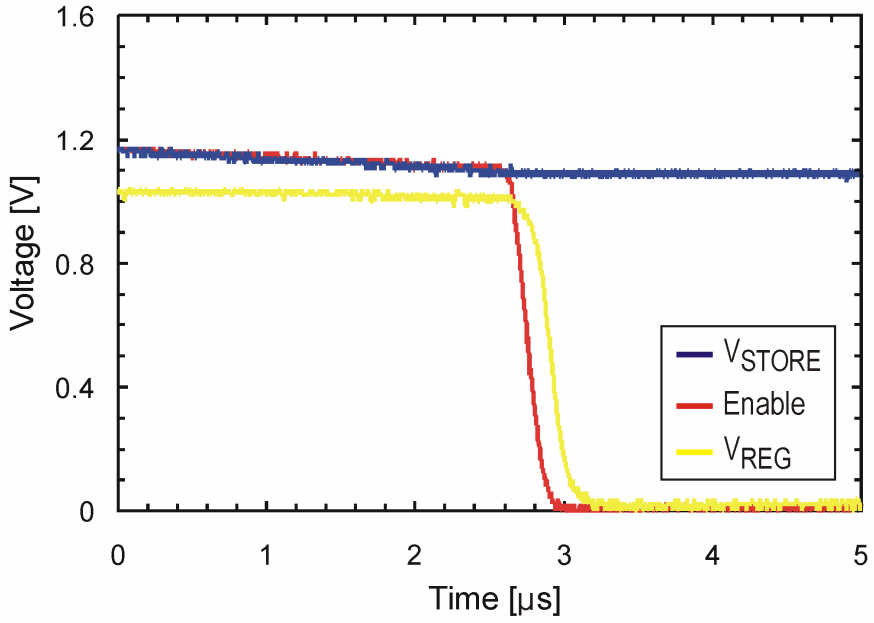


Fig. 3.16. Turn-off transient response (C_{STORE} = 50 nF, I_{CHARGE} = 1 µA, I_{LOAD} = 1 mA).

The temperature dependence of voltage reference *REF2* was also investigated. *REF2* operates during the discharge phase, with a supply voltage that varies from 1.68 V to 1.15 V. Therefore, it must be accurate over a wide range of supply voltages to ensure proper system operation. In Fig. 3.17, *REF2* voltage variations versus temperature are reported for 1.2-V and 1.6-V supply voltages. As apparent, good matching between simulations and measurements was achieved. The voltage limiter was tested as well. Injecting a 50-µA current into the 50-nF storage capacitor, the voltage drop across its terminals is clamped at 1.8 V by the limiter. Finally, the power management current leakage was measured. This is the system current consumption during the charge phase. At room temperature and 1.6-V supply voltage (V_{STORE}), the measured current leakage is 80 nA, which closely agrees with the simulated one.

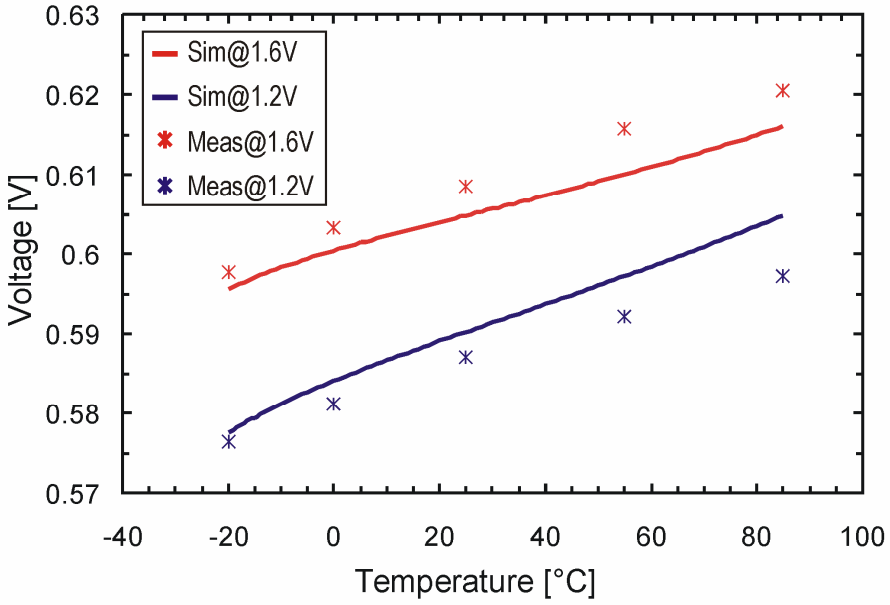


Fig. 3.17. Temperature dependence of reference voltage *REF2* for 1.2-V and 1.6-V supply voltages.

3.2.2 RF front-end characterization

Both the RX and TX sections of the RF front-end were extensively characterized and the measured performance are here reported. The measured current consumptions of the receiver building blocks are listed in Table 3.3.

Table 3.3. Current consumption of the RX building blocks.

Building block	Current consumption [µA]
Limiter + Digital circuits	140
Charge Pump	30
VCO	210
SCL-2-CMOS interface	100

As apparent, the receiver exhibits an overall current consumption of 480 μA with a 1-V supply voltage. The measured receiver sensitivity (i.e. the minimum input power level required to accomplish a correct demodulation) is –28 dBm. It is set by the limiting amplifier, which has to provide a rail-to-rail output voltage swing in order to allow proper operation of the following frequency divider.

Nevertheless, a correct demodulation can only be accomplished if a suitable signal-to-noise ratio (SNR) at the data detection node (i.e. the VCO control voltage) is guaranteed. Concerning this, it is worth remembering that, for the proposed PLL-based FSK receiver, the amplitude of the demodulated signal is proportional to the frequency spacing (Δf) between the two carriers exploited by the adopted BFSK modulation scheme. Therefore, a larger frequency spacing would result in a higher SNR at the cost of a wider transmitted signal bandwidth for a given data rate (lower system spectral efficiency).

The minimum detectable frequency difference is set by the receiver noise performance, which is mainly affected by the PLL phase noise. The measured PLL phase noise is reported in Fig. 3.18 as a function of the frequency offset from the 2.45-GHz carrier. To perform this measurement a 915-MHz single-tone continuous-wave (*CW*) signal is fed to the receiver input with a power level of -28 dBm. As shown in Fig. 3.18, a good agreement between measurements and simulations was achieved. The reported noise performance translates into a minimum detectable frequency difference of 3 MHz. Figs. 3.19-3.21 display the eye diagrams of the demodulated output showing the integrity of the decoded bits for different data rates. The maximum measured data rate is 5-Mbps.

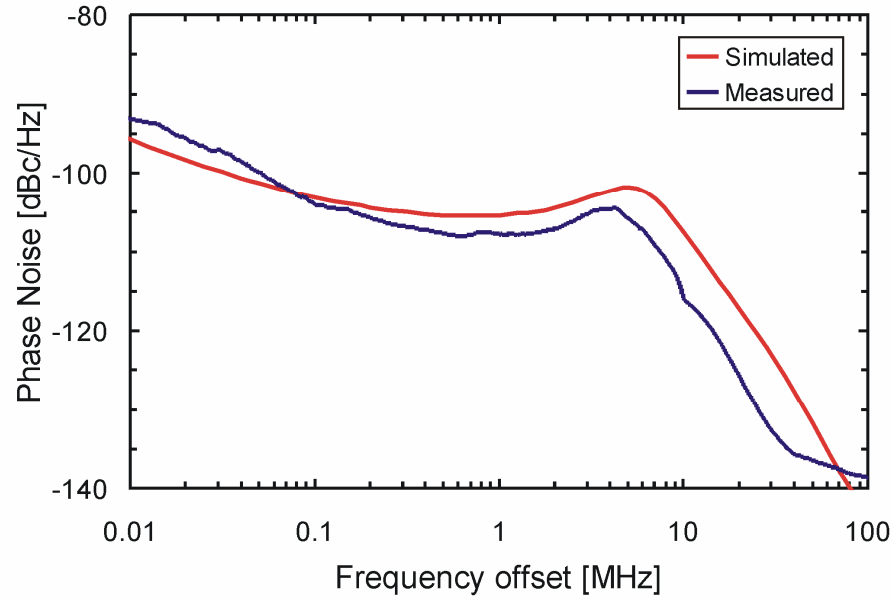


Fig. 3.18. Measured and simulated PLL phase noise as a function of the frequency offset from the 2.45-GHz carrier.

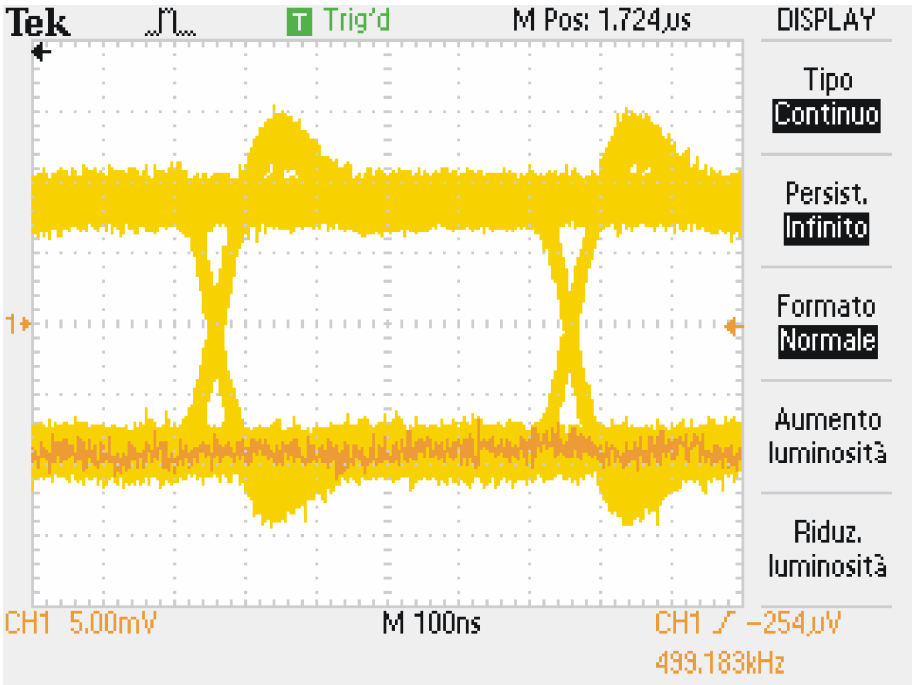


Fig. 3.19. Eye diagram of the demodulated output at 2 Mbps (Δf = 3 MHz, $P_{S,AV}$ = –28 dBm).

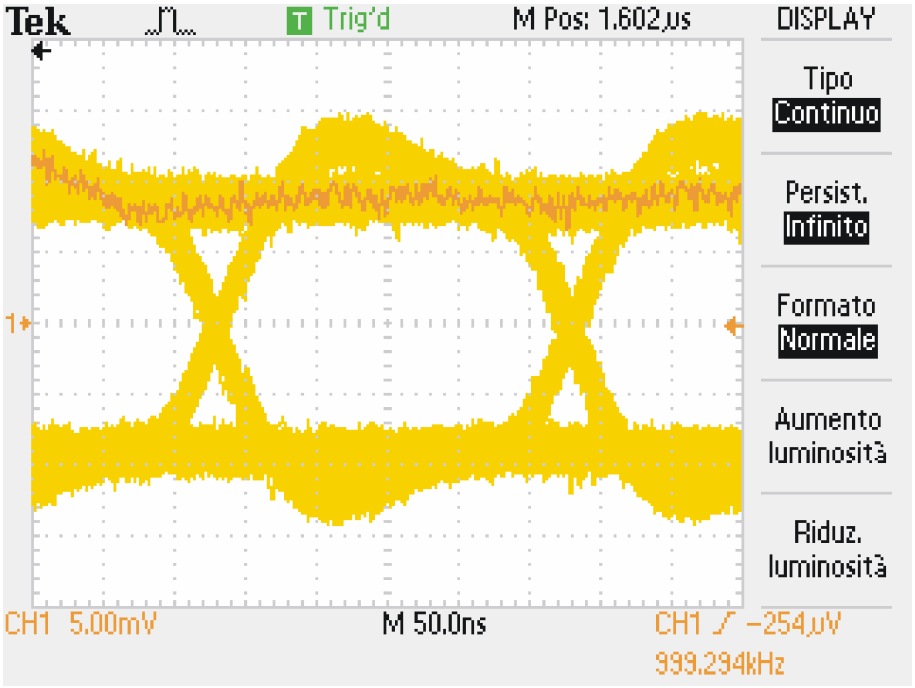


Fig. 3.20. Eye diagram of the demodulated output at 4 Mbps (Δf = 3 MHz, $P_{S,AV}$ = –28 dBm).

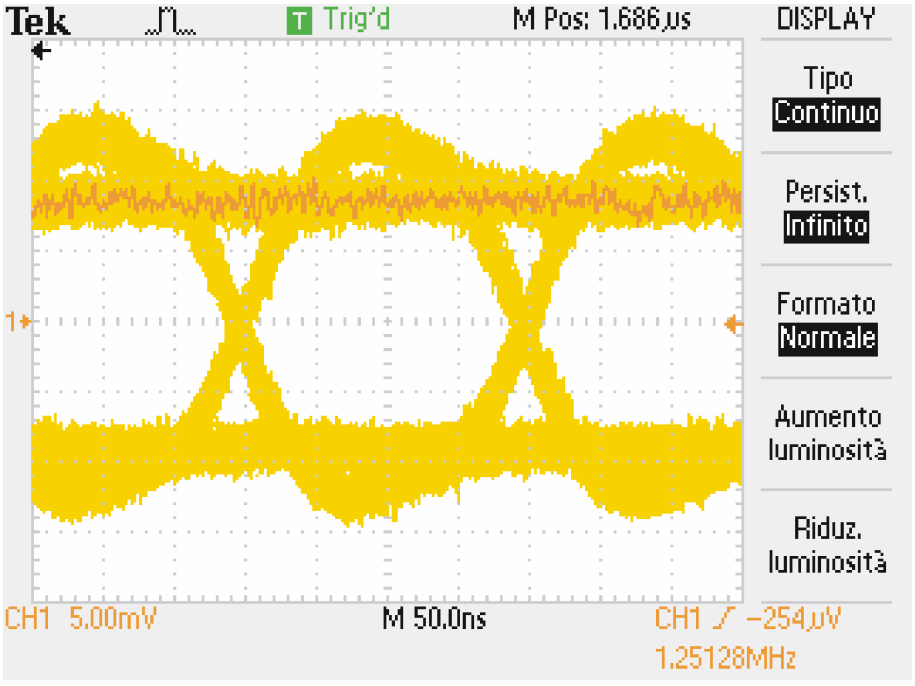


Fig. 3.21. Eye diagram of the demodulated output at 5 Mbps (Δf = 3 MHz, $P_{S,AV}$ = –28 dBm).

As regards the TX section of the RF front-end, it exploits the synthesized 2.45-GHz carrier to send data to the hub in OOK mode. Fig. 3.22 shows the VCO tuning range, which sets the covered transmission band.

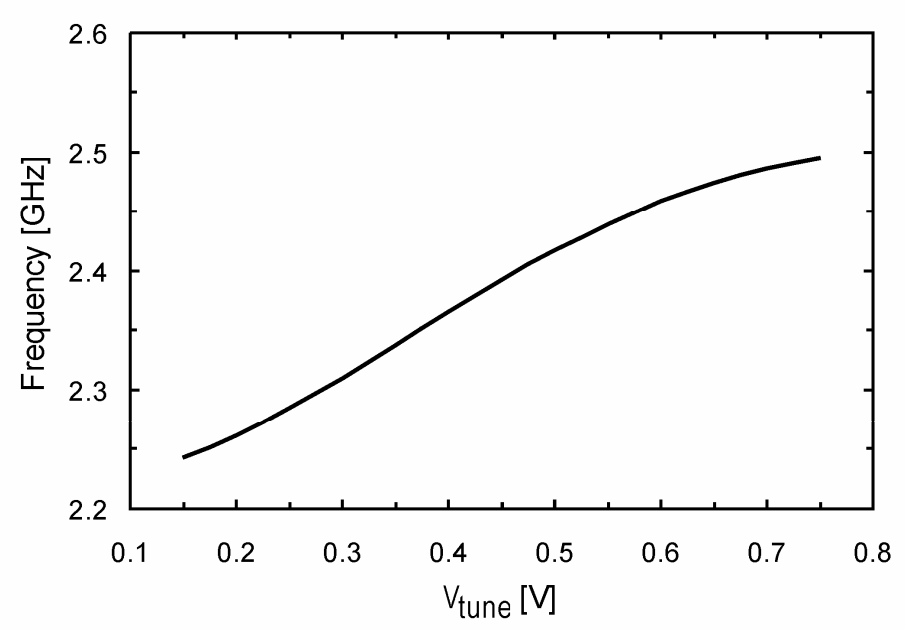


Fig. 3.22. Measured VCO tuning range.

As apparent, the transmission carrier lies in the range 2.25GHz-2.5GHz, thus covering the targeted 2.45-GHz ISM band. As already mentioned, data transmission is accomplished by merely switching on and off the output buffer according to an OOK modulation scheme. Fig. 3.23 displays the buffer's output waveform for a 10-Mbps data rate. The spectrum of the transmitted signal is displayed in Fig. 3.24. The output buffer is able to deliver a maximum power of -12.5 dBm to a 50-Ω load while drawing a 380-μA current from a 1-V supply voltage. It is worth nothing that the measured maximum output power level is

2.5 dBm lower than the simulated one. This discrepancy is due to a sub-optimal output matching.

Fig. 3.23. Time-domain waveform of the transmitted signal (pink curve) and related data stream (violet curve).

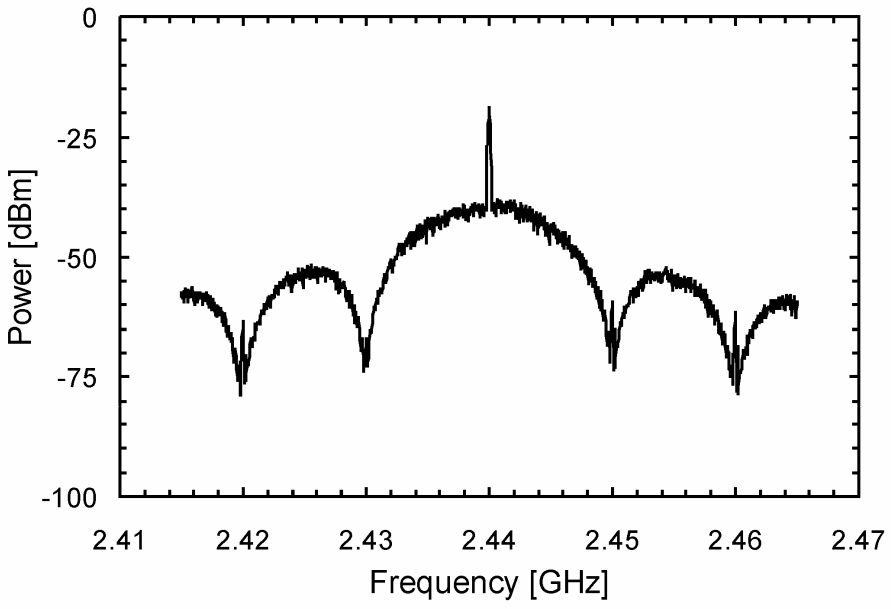


Fig. 3.24. Spectrum of the transmitted signal.

Finally, the most meaningful performance parameters concerning the RF front-end are summarized in Table 3.4.

Table 3.4. RF front-end's performance summary.

Parameter	Performance
RX operating frequency	902-928 MHz
Downlink modulation	FSK
Receiver data rate	up to 5 Mbps
Input sensitivity	-28 dBm
Minimum detectable frequency difference	3 MHz
RX current consumption	480 μA
TX operating frequency	2.405-2.475 GHz
Uplink modulation	OOK
Transmitter data rate	up to 10 Mbps
Maximum transmitted power	-12.5 dBm
TX buffer current consumption	380 μA

3.2.3 Transceiver performance

A complete characterization of the whole system was carried out by supplying the transceiver input with a 915-MHz FSK-modulated signal, which delivers power and data to the transponder.

For the transceiver characterization a 100-nF on-board capacitor was used as storage unit, in order to properly extend the RF front-end operating time. According to the adopted charge & burst procedure, the power management unit detects the charge status by sensing the voltage drop across the storage capacitor and turns the RF front-end on as soon as a fair supply voltage level is reached. The transceiver operates with a minimum input RF power of –15 dBm (30 μW), which translates into an operating free-space distance of 13 m, assuming a 4-W EIRP source and a 3-dB RX antenna gain. The most meaningful waveforms concerning the power management unit are displayed in Figs. 3.25-3.26. With a 100-nF storage capacitor a charging time of 60 ms was measured along with an operating time of 60 μs.

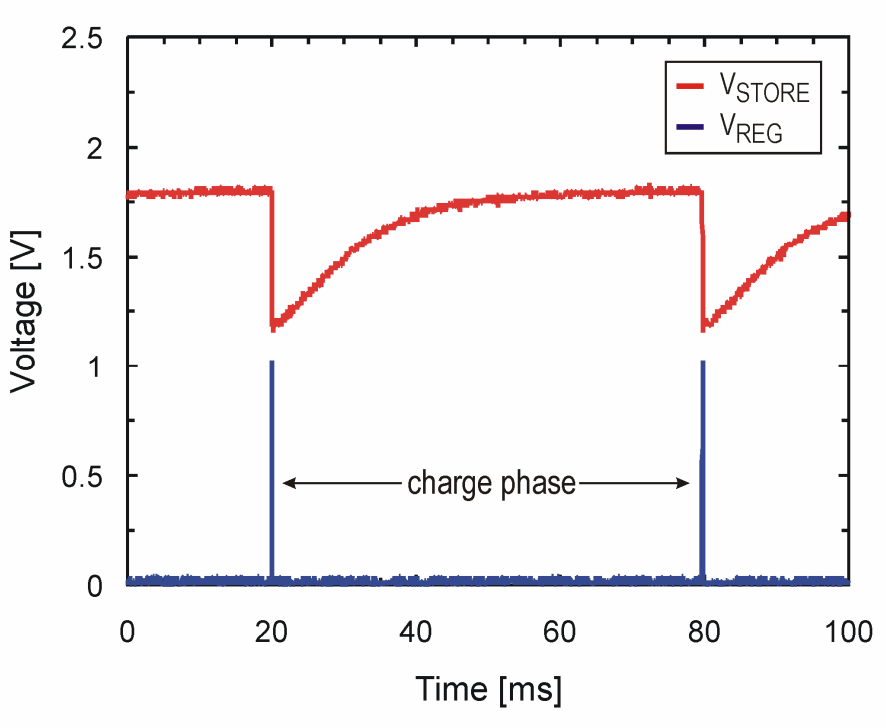


Fig. 3.25. Power management waveforms showing the charge phase ($P_{S,AV}$ = –15 dBm, f = 915 MHz, C_{STORE} = 100 nF).

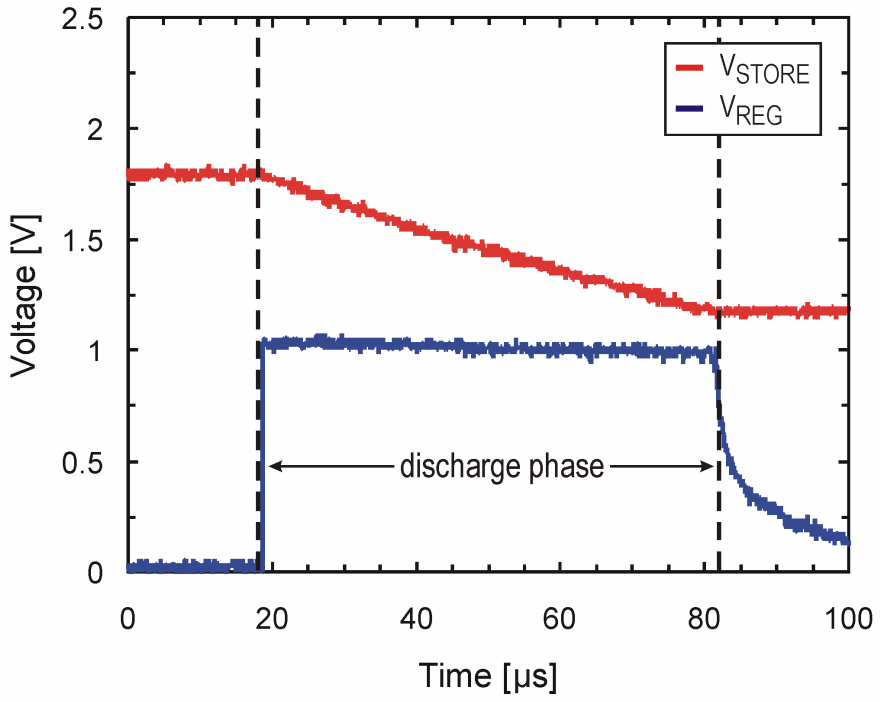


Fig. 3.26. Power management waveforms showing the discharge phase ($P_{S,AV}$ = –15 dBm, f = 915 MHz, C_{STORE} = 100 nF).

The transient response of the RF front-end was also investigated. To this aim the 10% settling time of the VCO control voltage was measured by applying a step envelope RF signal at the circuit input.

The time-domain waveforms of the VCO control voltage and the regulated supply voltage are shown in Fig. 3.27. As apparent, the receiver exhibits a start-up time of about 800 ns. A such fast transient response is needed to reduce the transceiver latency at the beginning of each operating cycle, thus optimizing the system energy efficiency.

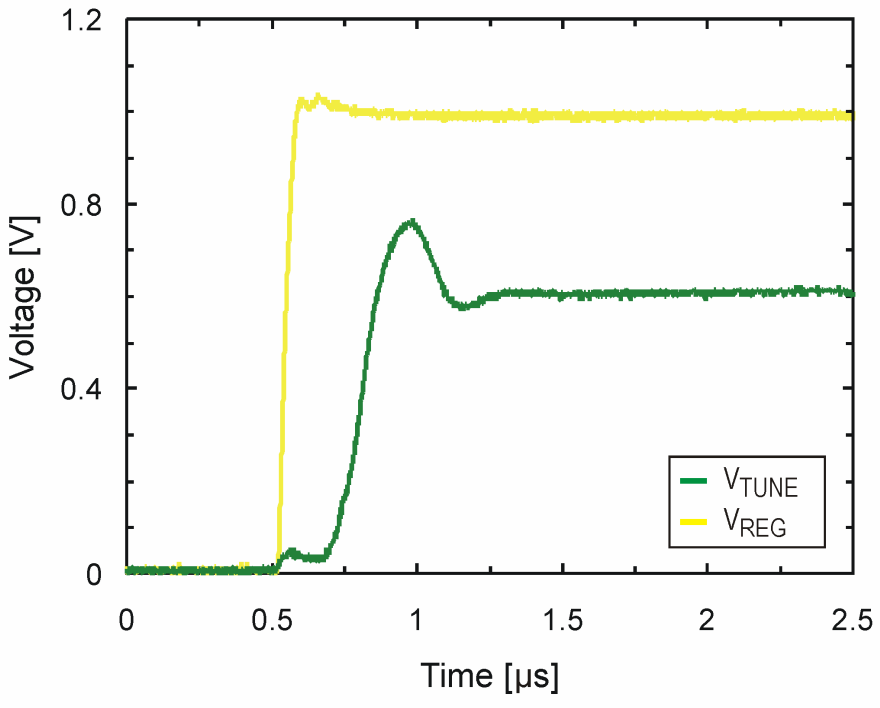


Fig. 3.27. Time-domain waveforms of the VCO control voltage and the regulated supply voltage.

The noise performance of the transceiver was characterized as well. The phase noise at the PLL output is shown in Fig. 3.28, as a function of the frequency offset from the 2.45-GHz carrier. To perform this measurement, a 1.8-V DC voltage was frozen on the storage capacitor, while a 915-MHz single-tone continuous-wave (CW) signal was fed at the RF input of the system. A slightly higher noise power level was measured with respect to the stand-alone RF front-end because of the noise contribution of the power management unit. Nevertheless, the minimum detectable frequency difference (Δf) is still 3 MHz. The eye diagrams of the demodulated output are reported in Figs. 3.29-3.31 for different data rates.

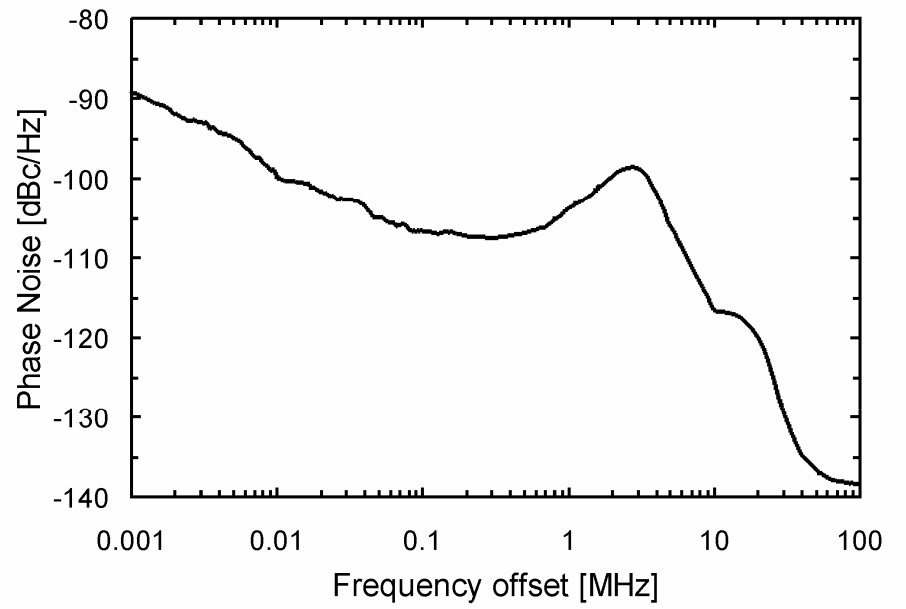


Fig. 3.28. System phase noise as a function of the frequency offset from the 2.45-GHz carrier.

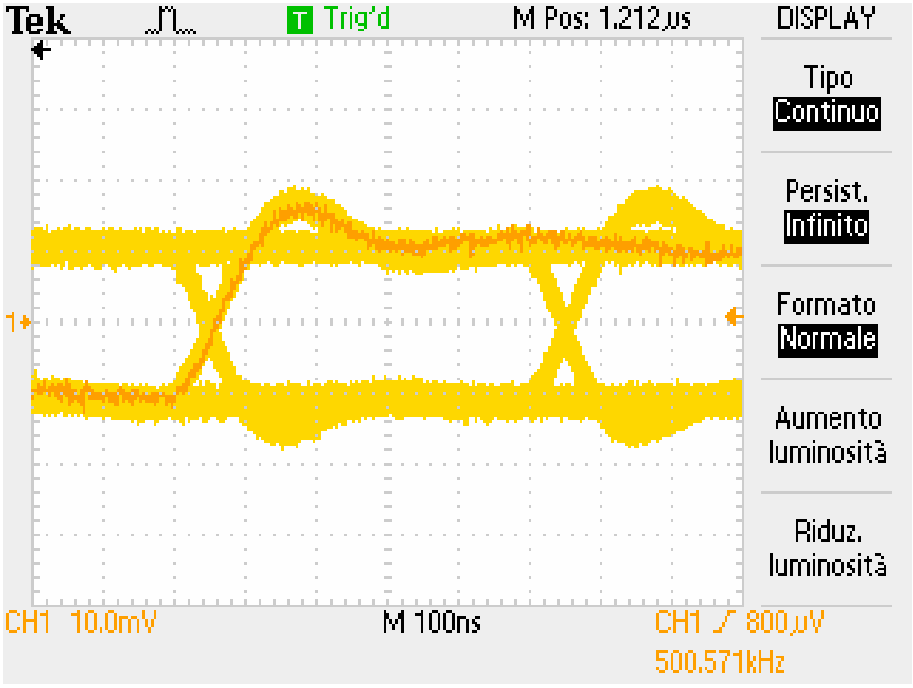


Fig. 3.29. Eye diagram of the demodulated output at 2 Mbps (Δf = 3 MHz, $P_{S,AV}$ = –15 dBm).

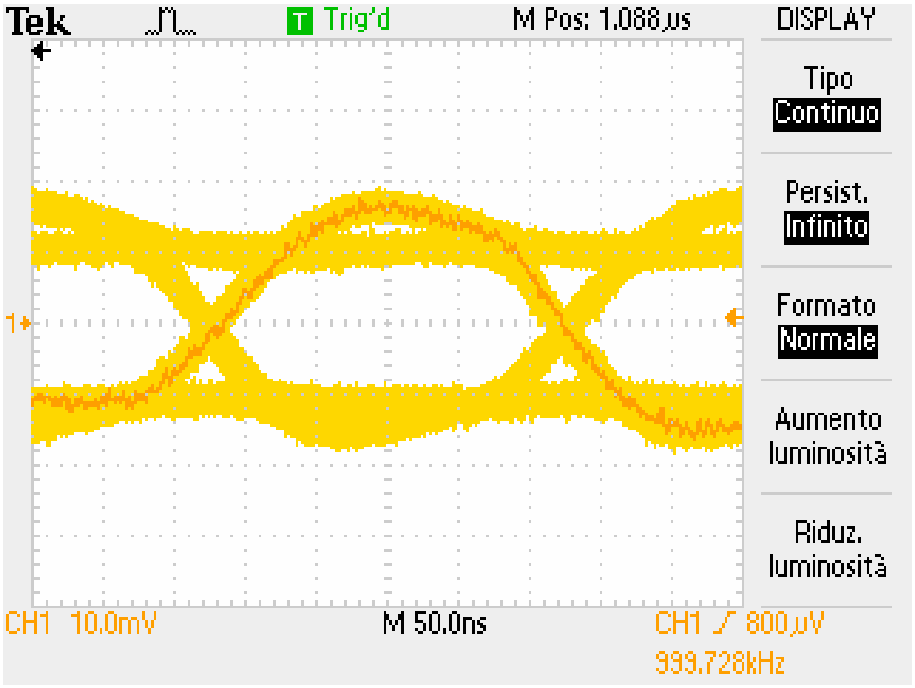


Fig. 3.30. Eye diagram of the demodulated output at 4 Mbps (Δf = 3 MHz, $P_{S,AV}$ = –15 dBm).

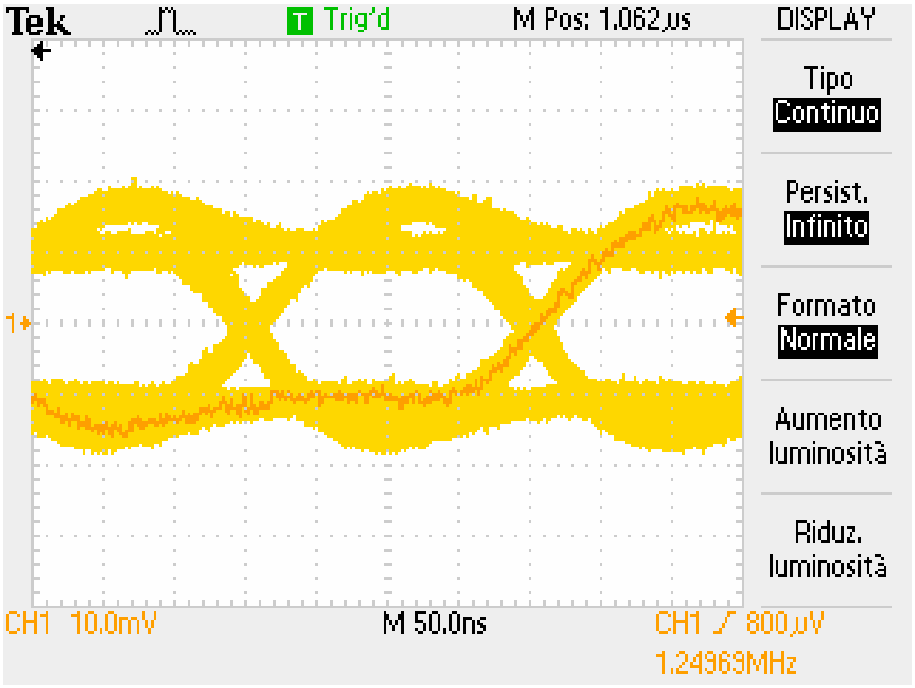


Fig. 3.31. Eye diagram of the demodulated output at 5 Mbps (Δf = 3 MHz, $P_{S,AV}$ = –15 dBm).

These measurements were performed by exploiting a 915-MHz FSK-modulated input signal with a frequency deviation ($\Delta f/2$) of 1.5 MHz and a power level of –15 dBm. As shown, the maximum measured receiver data rate is 5 Mbps. Finally, Fig. 3.32 shows the time-domain waveform of the transmitted signal for a 10-Mbps OOK modulation. The maximum measured output power is –12.5 dBm.

Fig. 3.32. Time-domain waveforms of the output data stream (violet curve) and the transmitted signal (pink curve).

The most meaningful performance parameters of the designed batteryless transceiver are listed in Table 3.5.

Table 3.5. Batteryless transceiver's performance summary.

Fabrication technology	90nm CMOS
Die size	1.4mm × 1.1mm.
RX operating frequency	902-928MHz
TX operating frequency	2.405-2.475GHz
Uplink modulation	OOK up to 10-Mbps
Downlink modulation	FSK (Δf = 1.5MHz) up to 5-Mbps
Minimum input RF power	-15dBm (30μW)
Maximum transmitted power	-12.5dBm
RX current consumption	480μA
TX buffer current consumption	380μA

Conclusions

The demand of low-cost wireless sensor networks has pushed the research toward alternative wireless platforms with respect to traditional battery-powered devices. Energy harvesting is a promising technology for the deployment of potentially maintenance-free WSNs. Several energy sources have been investigated in order to be used for the implementation of battery-free wireless sensor nodes. RF harvesting is one of the most viable technology, since RF power can be easily provided when needed, in every location, by means of intentional radiators (i.e. base stations). Designing a low-power low-complexity RF transceiver is the biggest challenge in the implementation of RF-powered sensor networks.

In this work the design and characterization of a RF-powered transceiver is presented. The system includes a RF harvesting module, implemented through an improved multi-stage rectifier, a power management unit and a RF front-end, which exploits an active narrowband transmission scheme to extend the system operating range. A prototype of the designed RF transceiver was manufactured in a 90-nm CMOS technology by TSMC. The circuit supports a 915-MHz FSK downlink and a 2.45-GHz OOK uplink, which attain a data rate up to 5 and 10 Mbps, respectively. The embedded harvesting unit enables batteryless operation with an input power threshold of –15dBm and a maximum transmit power of –12.5dBm.

Concerning the RF front-end, a PLL-based architecture allows TX carrier synthesis from the incoming RX signal, thus avoiding the use of a local quartz crystal oscillator. This results in a highly integrated wireless platform, which is suitable for the implementation of low-cost and potentially maintenance-free wireless sensor networks. Moreover, thanks to the adopted active narrowband transmission scheme, the proposed solution outperforms traditional backscattering-based transceivers (RFID-like) without burdening the hub complexity, unlike to the recently published solutions, which adopt an UWB transmission approach [23]-[25]. The need for two antennas (at 915 MHz for the RX section and at 2.45 GHz for the TX one) is the drawback of the presented system. However, a dual-band antenna might be profitably exploited for both downlink and uplink operation.

Some work remains to be done, both concerning the antenna design and the optimization of the transceiver performance. Indeed, reducing the transceiver power consumption is desirable in order to extend the operating time (discharge phase) of the transceiver and/or reducing the charge time. Moreover, the reduction of the transceiver input power threshold along with the implementation of more efficient RF energy harvesting systems would allow improving the system operating range.

Today, the most practical implementations of RF energy harvesting need for intentional sources to provide the energy. As IC power threshold decreases and the efficiency of the adopted RF energy harvesting systems increases, ambient RF energy harvesting will become feasible and available in more areas. The

development of efficient multi-band RF energy harvesters will also play an important role in the realization of ambient RF harvesting over the next years.

Appendix

Appendix A

A CAD-oriented design procedure was developed for the energy harvesting system design. The proposed algorithm splits the optimization of the system PCE into two separate optimizations aimed at maximizing parameters Σ_{M} and Σ_{R}, respectively. The equivalence of the two design strategies can be easily proven as follows. For the sake of clarity, we will consider the very simple case in which only two design parameters affect the system PCE, one concerning the matching network (namely a) and one pertaining to the rectifier (namely b). Under such assumption, equations (2.6), (2.10), and (2.11) can be rewritten as:

$$\Sigma(a,b) = G_{\mathrm{A}}(a)\, T(a,b)\, \eta(b) \tag{A.1}$$

$$\Sigma_{\mathrm{M}}(a,b) = G_{\mathrm{A}}(a)\, T(a,b) \tag{A.2}$$

$$\Sigma_{\mathrm{R}}(a,b) = T(a,b)\, \eta(b) \tag{A.3}$$

Let (a_1, b_1) be the optimum-PCE design and (a_2, b_2) be the solution of the proposed iterative procedure. Maximization of Σ implies that:

$$\frac{\partial \Sigma}{\partial a}(a_1, b_1) = 0 \tag{A.4}$$

$$\frac{\partial \Sigma}{\partial b}(a_1, b_1) = 0 \tag{A.5}$$

According to (A.1), equations (A.4) and (A.5) lead to:

$$\frac{\partial G_{\mathrm{A}}}{\partial a}(a_1)\, T(a_1, b_1)\, \eta(b_1) + G_{\mathrm{A}}(a_1) \frac{\partial T}{\partial a}(a_1, b_1)\, \eta(b_1) = 0 \tag{A.6}$$

$$G_{\mathrm{A}}(a_1) \frac{\partial T}{\partial b}(a_1, b_1)\, \eta(b_1) + G_{\mathrm{A}}(a_1)\, T(a_1, b_1) \frac{\partial \eta}{\partial b}(b_1) = 0 \tag{A.7}$$

The goal of the proposed iterative design procedure can be formally expressed as:

$$\frac{\partial \Sigma_{\mathrm{M}}}{\partial a}(a_2, b_2) = 0 \tag{A.8}$$

$$\frac{\partial \Sigma_{\mathrm{R}}}{\partial b}(a_2, b_2) = 0 \tag{A.9}$$

According to (A.2) and (A.3), equations (A.8) and (A.9) read:

$$\frac{\partial G_{\mathrm{A}}}{\partial a}(a_2)\, T(a_2, b_2) + G_{\mathrm{A}}(a_2) \frac{\partial T}{\partial a}(a_2, b_2) = 0 \tag{A.10}$$

$$\frac{\partial T}{\partial b}(a_2, b_2)\,\eta(b_2) + T(a_2, b_2)\,\frac{\partial \eta}{\partial b}(b_2) = 0 \tag{A.11}$$

It is now apparent that systems (A.6)-(A.7) and (A.10)-(A.11) are exactly the same. Therefore, they have the same solution, i.e. a_1=a_2 and b_1=b_2. This proves the equivalence of the two design strategies.

Appendix B

Frequency-shift keying (FSK) is a frequency modulation scheme in which data are transmitted through discrete frequency changes of a carrier wave. The simplest FSK modulation scheme is binary FSK (BFSK), in which the frequency of the carrier is switched between a high ($f_C+\Delta f/2$) and low ($f_C-\Delta f/2$) level according to the binary ("0" or "1") information to be transmitted.

The frequency spacing Δf between the high and low levels of the carrier frequency is a key parameter for the adopted PLL-based FSK demodulator. Indeed, the amplitude of the demodulated signal is proportional to Δf, as we will show. A simplified block diagram of the designed receiver is sketched in Fig. B.1.

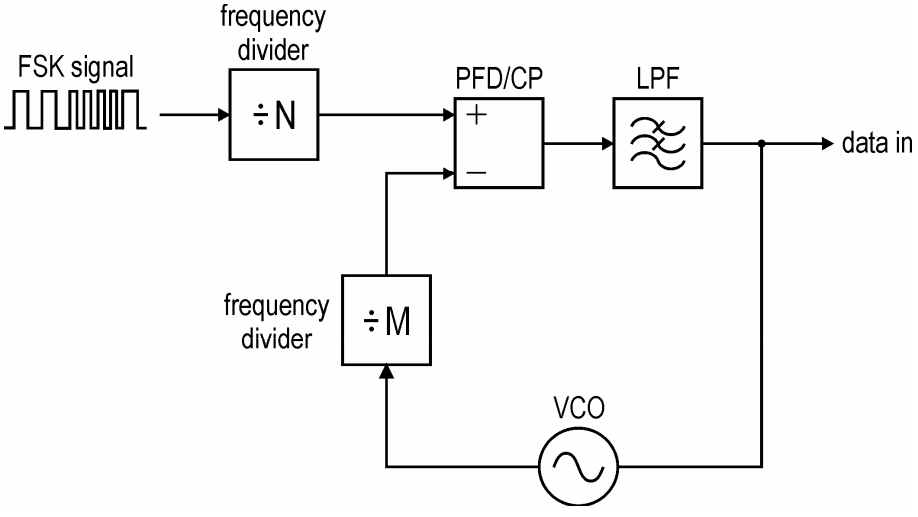


Fig. B.1. Block diagram of the PLL-based receiver.

The data detection node is the VCO control voltage. Once the PLL is locked to the incoming BFSK-modulated signal, the VCO control voltage is changed in order to track the frequency variations of the input signal. Let us consider the linear model of the PLL-based receiver (Fig B.2).

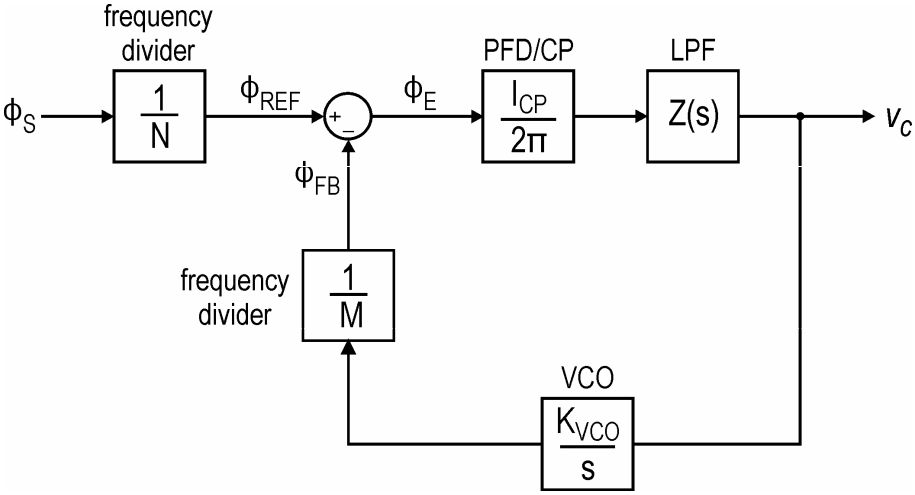


Fig. B.2. Linear model of the PLL-based FSK receiver.

Where Z(s) is the transfer function of the loop filter. As apparent from Fig. B.2:

$$\phi_E = \phi_{REF} - \phi_{FB} \tag{B.1}$$

$$\phi_{REF} = \frac{\phi_S}{N} \tag{B.2}$$

$$\phi_{FB} = \frac{v_C}{M}\frac{K_{VCO}}{s} \tag{B.3}$$

Where Φ_S is the phase variation of the input signal. If Φ_S varies slowly:

$$\phi_E = 0 \tag{B.4}$$

According to equations (B.1)-(B.3), equation (B.4) leads to:

$$v_C = \frac{M}{NK_{VCO}} s\phi_S \tag{B.5}$$

Let f_S be the frequency variation of the input signal ($2\pi f_S = s\Phi_S$). Then, equation (B.5) can be rewritten as:

$$v_C = 2\pi \frac{M}{NK_{VCO}} f_S \tag{B.6}$$

Equation (B.6) shows the relationship between the variation of the input signal frequency (f_S) and the corresponding variation of the VCO control voltage (v_C). For the sake of simplicity, let us assume that the frequency f of the input signal varies according to the following relation:

$$f = f_C + \Delta f \cdot \cos\left(\frac{\pi \cdot t}{T_b}\right) \tag{B.7}$$

Where f_C is the carrier frequency and $1/T_b$ is the data rate. Thus, the *RMS* value of the AC signal at the VCO control node reads:

$$v_{C,RMS} = \pi \frac{M}{NK_{VCO}} \frac{\Delta f}{\sqrt{2}} \tag{B.8}$$

As apparent from (B.8), the amplitude of the demodulated signal is proportional to the frequency spacing between the high and low levels of the frequency of the input signal.

From equation (B.8) an approximate expression of the signal-to-noise ratio (SNR) at the receiver output can be drawn:

$$SNR \approx \frac{1}{4} \cdot \left(\frac{M}{N} \right)^2 \cdot \left(\frac{\pi \cdot \Delta f}{K_{\mathrm{VCO}}} \right)^2 \cdot \frac{1}{\int_B Sv_{\mathrm{n}}(f) \cdot df} \tag{B.9}$$

Where Sv_{n} is the power spectral density of the noise at the receiver output and B is the signal bandwidth.

References

[1] J. Wilson, “Sensor technology handbook”, Burlington, MA, USA: Elvesier/Newnes, 2005.

[2] E. S. Leland, E. M. Lai, P. K. Wright, “A self-powered wireless sensor for indoor environmental monitoring,” in *Proc. of the Wireless Networking Symposium (WNCG)*, Austin, TX, USA, Oct. 2004.

[3] V. Leonov, *et al.*, “Wearable self-powered wireless devices with thermoelectric energy scavengers,” in *Proc. 2nd Eur. Conf. Exhib. Integr. Issues Miniaturized Syst.*, pp. 217–224, 2008.

[4] G. Chen, *et al.*, "Millimeter-scale nearly perpetual sensor system with stacked battery and solar cells," in *ISSCC Dig. Tech. Papers*, pp. 288-289, 2010.

[5] J. Colomer-Farrarons, P. L. Miribel-Catala, "A CMOS self-powered front-end architecture for subcutaneous event-detector devices", Springer 2011.

[6] R. J. M. Vullers, R. Van Schaijk, I. Doms, C. Van Hoof, R. Mertens, “Micropower energy harvesting”, *Solid-State Electronics*, Elvesier, pp. 684-693, April 2009.

[7] L. Mateu, F. Moll, “ Review of energy harvesting techniques and applications for microelectronics,” *SPIE Microtechnologies for the New Millenium*, pp. 359-373, 2005.

[8] S. Kamarudin, W. Daud, S. Ho,U. Hasran, “Overview on the challenges and developments of micro-direct methanol fuel cells,” in *J Power Sources* (DMFC), pp. 743–54, 2007.

[9] G.-Z. Yang, “Body Sensor Networks,” London, UK: Springer, 2006.

[10] “Freescale single-package tire pressure monitoring system”, *White paper,* [Online]. Available: http://www.freescale.com.

[11] M. Kuorilehto, *et al.,* “Ultra-low energy wireless sensor networks in practice,” England: John Wiley & Sons, 2007.

[12] S. Priya, D.J. Inman, “Energy harvesting technologies,” New York: Springer, 2009.

[13] M. Renaud, *et al*., “Piezoelectric harvesters and MEMS technology: fabrication, modeling and measurements,” *IEEE* S*olid–State Sensors, Actuators and Microsystems Conference*, pp. 891–894, June 2007.

[14] M. Marzencki, S. Basrour, B. Charlot, S. Spirkovich, M. Colin, “A MEMS piezoelectric vibration energy harvesting device,” *Power MEMS Conference*, pp. 45-48, Nov. 2005.

[15] W. Wang, V. Leonov, P. Fiorini, C. Van Hoof, “Micromachined thermopiles for energy scavenging on human body,” *IEEE* S*olid–State Sensors, Actuators and Microsystems Conference*, pp. 911-914, June 2007.

[16] H. Ostaffe, “RF energy harvesting enables wireless sensor networks”, [Online]. Available: http://www.sensorsmag.com.

[17] *ITU-R Radio Regulations*, Volume 1, [Online]. Available: http://www.itu.int.

[18] B. Otis, J. M. Rabaey, “Ultra-low power wireless technologies for sensor networks,” New York: Springer, 2007.

[19] R. Chakraborty, S. Roy, and V. Jandhyala, “Revisiting RFID link budgets for technology scaling: range maximization of RFID tags,” *IEEE Microwave Theory Tech.*, vol. 59, pp. 496-503, Feb. 2011.

[20] K. Finkenzeller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification*, 2nd ed., Chicester, Sussex, UK: John Wiley & Sons, 2003.

[21] D. Yeager, F. Zhang, A. Zarrasvand, B. Otis "A 9.2µA Gen 2 compatible UHF RFID Sensing tag with -12dBm sensitivity and 1.25µVrms input-referred noise floor," in *ISSCC Dig. Tech. Papers*, pp. 52-53, 2010.

[22] H. Reinisch, *et al.*, "A 7.9μW remotely powered addressed sensor node using EPC HF and UHF RFID technology with -10.3dBm sensitivity," in *ISSCC Dig. Tech. Papers*, pp. 454-455, 2011.

[23] M. Beghaei-Nejad, *et al.*, "A remote-powered RFID tag with 10Mb/s UWB uplink and –18.5dBm sensitivity UHF downlink in 0.18μm CMOS," in *ISSCC Dig. Tech. Papers*, pp. 198-200, Feb. 2009.

[24] S. Radiom, M. Beghaei-Nejad, K. Mohammadpour-Aghdam, G. A. E. Vandenbosch, L.-R. Zheng, and G. G. E. Gielen, "Far-field on-chip antennas monolithically integrated in a wireless-powered 5.8-GHz downlink/UWB uplink RFID tag in 0.18-μm standard CMOS," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1746-1758, Sept. 2010.

[25] M. Pelissier, *et al.*, "A 112 Mb/s full duplex remotely-powered impulse-UWB RFID transceiver for wireless NV-memory applications," *IEEE J. Solid-State Circuits*, vol. 46, pp. 916-927, Apr. 2011.

[26] F. Kocer and M. P. Flynn, "A new transponder architecture with on-chip ADC for long-range telemetry applications," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1142-1148, May 2006.

[27] S. Pellerano, J. Alvarado Jr., and Y. Palaskas, "A mm-wave power-harvesting RFID tag in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1627-1637, Aug. 2010.

[28] *Federal Communications Commission (FCC) Rules & Regulations* in US Code of Federal Regulations, Title 47, Chapter 1 [Online]. Available: http://wireless.fcc.gov/index.htm.

[29] *ITU Recommendation P.1238-6*, "Propagation data and prediction methods for the planning of indoor radiocommunication systems and radio local area networks in the frequency range 900 MHz to 100 GHz," Oct. 2009.

[30] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602-1608, Oct. 2003.

[31] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35-41, Jan. 2006.

[32] H. Nakamoto, *et al.*, "A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-μm technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 101-110, Jan. 2007.

[33] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I*, *Reg. Papers*, vol. 54, no. 1, pp. 153-166, Jan. 2007.

[34] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1287-1302, May 2008.

[35] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011-3018, Nov. 2009.

[36] J. F. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374-378, Jun. 1976.

[37] H. Lin, K.-H. Chang, and S.-C. Wong, "Novel high positive and negative pumping circuits for low supply voltage," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 1999, vol. 1, pp. 238-241.

[38] J. F. Dickson, "Voltage multiplier employing clock gated transistor chain," U.S. Patent 4,214,174, Jul. 22, 1980.

[39] F. Carrara, G. Papotto, G. Palmisano, "Methodology and circuits for threshold compensation in voltage multipliers," IT patent appl. no. MI09A001646 filed Sep. 9, 2009.

[40] G. Papotto, F. Carrara, G. Palmisano, "A 90-nm CMOS threshold-compensated RF energy harvester," in . *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985-1987, Sept. 2011.

[41] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed., Upper Saddle River, NJ, USA: Prentice-Hall, 1996.

[42] G. De Vita and G. Iannaccone, "Design criteria for the RF section of UHF and microwave passive RFID transponders," *IEEE Trans. Microwave Theory Tech.*, vol. 53, no. 9, pp. 2978-2990, Sep. 2005.

[43] J.-P. Curty, N. Joehl, F. Krummenacher, C. Dehollain, and M. J. Declercq, "A model for μ-power rectifier analysis and design,"*IEEE Trans. Circuits Syst. I*, *Reg. Papers*, vol. 52, no. 12, pp. 2771-2779, Dec. 2005.

[44] R. E. Barnett, J. Liu, and S. Lazar, "A RF to DC voltage conversion model for multi-stage rectifiers in UHF RFID transponders," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 354-370, Feb. 2009.

[45] C. De Roover and M. S. J. Steyaert, "Energy supply and ULP detection circuits for an RFID localization system in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1273-1285, Jul. 2010.

[46] J. Shin, I.-Y. Chung, Y. J. Park, and H. S. Min, "A new charge pump without degradation in threshold voltage due to body effect," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1227-1230, Aug. 2000.

[47] G. A. Rincón-Mora, "Voltage references: From Diodes to Precision High-Order Bandgap Circuits," New York: John Wiley & Sons, 2001.

[48] H. J. Oguey, D. Aebischer "CMOS Current Reference Without Resistance" *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1132-1135, Jul. 1997.

[49] G. De Vita, G. Iannaccone, "A sub-1-V, 10ppm/°C, Nanopower Voltage Reference Generator," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, July 2007.

[50] R. G. H. Eschauzier, L. P. T. Kerklaan, and Johan H. Huijsing, "A 100-MHz 100-dB Operational Amplifier with Multipath Nested Miller Compensation Structure" *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1709-1717, Dec. 1992.

[51] J. Rogers, C. Plett, and F. Dai, "Integrated Circuit Design for High-Speed Frequency Synthesis," Boston, MA: Artech House, 2006.

[52] B. Razavi, “RF Microelectronics,” Upper Saddle River, NJ, USA: Prentice Hall, 1998.

[53] B. Razavi, “Design of analog CMOS integrated circuits,” New York: MacGraw-Hill, 2001.