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AlGaN/GaN heterostructures for enhancement mode transistors

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To the memory of Dr. Vito Raineri,
who introduced me to this
wonderful adventure

Contents

Introduction

In the last 30 years, *microelectronics* research activities have registered a growth with a nearly exponential rate. These continuous progresses led to the miniaturizing of devices and integrated circuits and, consequently, to an increased circuit density and complexity of the systems at lower costs. However, the critical device size for commercial products is already approaching the nanoscale dimensions. Hence, several new issues, related to the fabrication processes of new multifunctional materials and to the final device performances and reliability, are encountered. The significant development of microelectronics devices for computing technology was closely followed by that of wireless and optical communications systems.

However, the rapid expansion of computing capability related to the device miniaturization is not the unique key issue in modern electronics. In fact, today the continuous increase of electric power demand in our society has become a global concern, whose solution cannot be simply found in the device miniaturization or in the simple increase of the electric power supply. Rather, the reduction of the energy consumption through its efficient use is the main task of modern *power electronics*.

For several years Silicon (Si) has been the dominant material for semiconductor devices technology. However, the physical limits and the ultimate performances of Si, in terms of power handling, maximum operating temperature and breakdown voltage, have been already reached. In particular, due to the band gap and intrinsic carrier concentration of the material, Si devices are limited to work at a junction temperature lower than 200 °C. Hence, the material is less suitable for modern power electronics applications [1,2].

On the other hand, *wide band semiconductors* (WBG), such as silicon carbide (SiC), gallium nitride (GaN) and related alloys, exhibit superior physical properties that can better satisfy the demand of increased power, frequency and operating temperature of the devices.

SiC technology is surely the most mature among the WBG materials. First, and foremost, the size of commercial SiC wafer has been continuously

increasing in the last decade and was accompanied by a reduction of the defect density (especially micropipes) [3]. Recently, 150 mm SiC wafers have been made available, thus making the processing of this material much easier even using in part the conventional Si equipments. Furthermore, the device processing technology has reached a high level of maturity and some SiC devices like Schottky diodes or MOSFETs operating in the range of 600-1200 V have already reached the market [4,5,6,7].

While SiC is undoubtedly the most mature WBG semiconductor, GaN and related alloys (like $Al_xGa_{1-x}N$) still suffer from the several physical issues related to both surface and interfaces [8,9]. Furthermore, the lack of good quality (and cheap) "free standing" GaN templates make also the material growth a serious concern, since heteroepitaxy on different substrates (like Al_2O_3, SiC, or Si) is required. Although for long time GaN has been mainly attractive because of the optoelectronics applications, the recent improvement of the material quality of GaN-based heteroepitaxial layers provided the scientific community with considerable incentive to investigate the potentialities of this material also for applications in power electronics. As a matter of fact, some works demonstrated in the last years the possibility to fabricate Schottky diodes with a high breakdown voltage on good quality GaN material [10,11,12,13] and, lately, quasi-vertical Schottky diodes in GaN on Al_2O_3, with breakdown voltage of 600 V and forward current of 6 A at 1.7 V, were announced [14].

Furthermore, the continuous development of the quality of epitaxial GaN over large diameter Si-substrates (recently up to 200 mm) is resulting into significant advances also in GaN-based transistors for power switching and millimeter wave communications [15,16].

Although the low-field mobility of bulk GaN is much lower than that of other III-V materials like GaAs, GaN has a larger saturation velocity and a wide band gap, very suitable for using it as a channel material in high frequency power devices.

In this context, further contributing to the outstanding properties of GaN is the possibility to form *AlGaN/GaN heterostructures* with a large band discontinuity. In this system, a *two-dimensional electron gas (2DEG)* is formed due to the presence of both a spontaneous and piezoelectric polarization of the material. The high polarizations and resulting electric

fields in AlGaN/GaN heterostructures produce high interface charge densities even for unintentionally doped materials. In particular, the 2DEG formed is AlGaN/GaN heterostructures can have sheet carrier densities in the order of $1\text{-}3\times10^{13}$ cm^{-2}, i.e., well in excess of those achievable in other III–V systems like GaAs. Moreover, the possibility to use undoped material results in a significant improvement of the electron mobility in the 2DEG, due to the reduction of Coulomb scattering with ionized impurities.

AlGaN/GaN heterostructures are particularly interesting for the fabrication of *high electron mobility transistors* (HEMTs), based on the presence of the 2DEG. This kind of devices were first demonstrated in GaN by Khan et al. in the 1993 [17]. In a HEMT, the sheet carrier density in the 2DEG channel is modulated by the application of a bias to a Schottky metal gate. These devices are depletion mode (*normally-on*), i.e., a negative bias must be applied to the gate in order to deplete the electron channel and turn the device off. Clearly, since the 2DEG is confined in the potential well arising from the band discontinuity of the two materials (AlGaN and GaN) and the conductive channel is located very close to the surface (i.e., typical thickness of the AlGaN barrier in a HEMT structure is around 20-30 nm), the physical problems affecting the operation of these devices must be investigated at a nanoscale level. Indeed, several fundamental issues related to both surfaces and interfaces in AlGaN/GaN heterostructures are today object of deep scientific investigation in order to understand the physical phenomena related to the carrier transport in these nanometric systems and, ultimately, improve the performance of HEMT devices.

As an example, one of the big problems related to GaN HEMTs is the presence of trapping centres near the surface or in the bulk of the material, that limit the maximum drain current, particularly under high frequency operation [18]. Another issue in AlGaN/GaN HEMTs is related to the high gate leakage currents at the Schottky gate, also related to the presence of electrically active near-surface defects in the thin AlGaN barrier layer. In order to overcome this problem, the use of a dielectric under the metal gate can be used to reduce the leakage current. However, the choice of the dielectric can be critical, due to the effects on the threshold voltage (the bias required to deplete the 2DEG) and, ultimately, on the device transconductance.

Surely, the most challenging aspect in the present research activity on GaN devices is the development of a reliable way to achieve an enhancement mode (*normally-off*) HEMT. In fact, enhancement mode AlGaN/GaN HEMTs would offer a simplified circuitry (eliminating the negative power supply), in combination with favourable operating conditions for device safety.

Several solutions to achieve a positive threshold voltage have been proposed, mostly involved modification of the first nanometers of the AlGaN barrier layer, like the use of a recessed gate approach, the introduction of fluorine atoms by plasma treatments, or the use of oxidation process of the near-surface. An interesting approach is the use of a p-GaN gate onto a conventional AlGaN/GaN heterostructures, rising the conduction band of the heterostructure in order to deplete the 2DEG. As a matter of fact, one company has already started to commercialize devices fabricated with such kind of approach [19].

Some of the above mentioned critical issues related to the development of enhancement mode AlGaN/GaN HEMTs with a p-GaN gate have been addressed in this thesis. In particular, the aim of this work was to clarify the mechanisms ruling the electronic transport at relevant interfaces in AlGaN/GaN devices after surface modification processes used in normally-off technologies, e.g, plasma treatments or oxidation, deposition of metal contacts or dielectrics, etc. For this purpose, in some cases the use of nanoscale electro-structural characterization techniques allowed to better explain the macroscopic electrical behaviour of these systems.

The thesis is divided in 6 chapters.

In *chapter 1*, after an historical introduction to GaN research, the main physical properties of the material are discussed, considering both the crystal structure and the electronic properties of the material (like its band gap, its spontaneous polarization, etc.) and emphasizing the reason why GaN is a suitable material for high power and high frequency device. An brief mention to the substrates used for the growth (Al_2O_3, SiC and Si) and the growth techniques is also given (HVPE, MOCVD, MBE).

Chapter 2 is focused on the properties of the AlGaN/GaN heterostructures. In the first part, after a brief introduction on the $Al_xGa_{1-x}N$ alloys, the formation of the 2DEG in semiconductor heterostructures is

explained, with special attention to the case of an AlGaN/GaN systems. In the second part, the working principle of the HEMT is discussed, defining some important parameters like the threshold voltage (that will be often used in the rest of the thesis) and describing how it is possible to characterize the 2DEG properties (carrier concentration and mobility) from the HEMT characteristics. Finally the most critical scientific open issues for AlGaN/GaN-based devices are described.

In *chapter 3*, a nanoscale characterization of modified AlGaN surfaces is presented in order to study possible approaches to deplete the 2DEG and obtain normally-off AlGaN/GaN HEMTs. In particular two specific different approaches have been investigated, i.e., the possibility to use a fluorine plasma treatment and the use of a local oxidation process. Both processes have the aim to modified locally the proprieties of the AlGaN barrier layer in the region below the gate electrode. To evaluate the modifications of the AlGaN properties several characterization techniques as Atomic Force Microscopy (AFM), Conductive Atomic Force Microscopy (C-AFM), Transmission Electron Microscopy (TEM) were employed in combination with macroscopic electrical measurements as Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements on fabricated test patterns. Even though a depletion of the 2DEG is possible by using these approaches, it has been concluded that several reliability concerns need to be investigated (especially in the case of the oxidation) before a practical application to devices can be envisaged.

In this context, it has been pointed out that among the possible approaches for the fabrication of enhancement mode transistors using AlGaN/GaN heterostructures, the use a p-GaN gate contact seems to be the most interesting one. Hence, c*hapter 4* reports a detailed investigation on the formation of Ohmic contact to p-GaN, which in turn can be extremely important when using a p-GaN gate electrode. In particular, the evolution of a Au/Ni bilayer, annealed at different temperatures and in two different atmospheres (Ar or N_2/O_2) was considered. The experimental approach included macroscopic electrical measurements of the fabricated test patterns as Transmission Line Method (TLM) or Van der Pauw (VdP). The electrical measurements of the contacts annealed under different conditions demonstrated a reduction of the specific contact resistance in oxidizing atmosphere. Structural characterizations of the metal layer carried out by

TEM and X-Ray Diffraction (XRD), associated with nanoscale electrical measurements by C-AFM, allowed to give a possible scenario on the Ohmic contact formation mechanisms. Finally, the temperature dependence of the specific contact resistance was studied in the two cases, thus allowing the extraction of the metal/p-GaN barrier.

In *chapter 5*, the fabrication and characterization of AlGaN/GaN transistors with the use of a p-GaN cap layer under the gate contact is presented. Firstly, by electrical I-V measurements on simple test structures, the impact of the p-GaN layer on the 2DEG channel was demonstrated. Then, more complex p-GaN/AlGaN/GaN transistors were fabricated and characterized. The C-V measurements showed a significant positive shift of the threshold voltage (V_{th}) with respect to devices without p-GaN gate, thus confirming the validity of our approach. Hence, basing on a simulation of the band structure, an optimized heterostructure was prepared, which led to a normally-off behaviour of the devices (V_{th} =1.4V). However, a further improvement in the material quality and processes is still needed in order to reduce the high leakage that affected the device characteristics .

Finally, c*hapter 6* reports on a preliminary study on the use of nickel oxide (NiO) as a dielectric below the Schottky gate contact in AlGaN/GaN heterostructures. First, a structural and morphological investigation of the NiO layers grown by MOCVD showed continuous epitaxial film. The electrical measurements on devices allowed to extract a value of the dielectric constant for the grown NiO very close to the theoretical one, and a strong reduction of the leakge current in HEMT structures integrating such a dielectric.

The research activity presented in this work of thesis was carried out using the clean room and others characterization facilities of CNR-IMM in Catania. The activity was supported by ST Microelectronics of Catania, that provided the AlGaN/GaN heterostructures grown on Si and gave access to some processing and characterization tools. The p-GaN material and p-GaN/AlGaN/GaN heterostructures grown on Al_2O_3 were provided by the Institute of High Pressure Physics (UNIPRESS) in Warsaw, Poland. Most of the work has been carried in the framework of the ENIAC JU Last Power project under grant agreement n° 120218.

Chapter 1: Properties of Gallium Nitride

The research activity on GaN dates back to the first 1930s. However, only in the '90s the material started to attract interest for power and RF electronics, because of its superior properties such a high band gap, a high breakdown field and a high saturated electron velocity. In this chapter, after an historical introduction to GaN research, the properties of GaN will be described, introducing the figures of merit that make the material promising for power electronics applications.

1.1 Historical introduction to GaN research

Electronics is the basic field for information and communication technology (ICT) and for the electric power control technology required to support modern human society.

Today, the need of electric power is continuously increasing and represents a global concern. In the next years, power electronics will play an important role for the reduction of the energy consumption all over the world. In this context, it is now commonly agreed that the most suitable approach to the problem is to improve the energy efficiency of the devices that could lead to a reduction of 20% of the global energy demand [20,21].

Many discrete power electronic devices are used in the power modules for the transmission and the conversion of electric power. For these devices, a reduction of the static and dynamic losses can directly result in the overall lowering of power consumption of the system. Also the next generation of

high-speed communication devices are becoming key technologies for network communication, requiring increasing operating frequency associated with portability and convenience.

Since the production of the first silicon transistor by Gordon Teal at the *Texas Instruments* [22], silicon (Si) has assumed a central role in the development of semiconductor devices. Recently however, Si technology is approaching the theoretical limits imposed by the material properties, in terms of maximum operation power, frequency and temperature.

In this general context, the research activities in modern electronics clearly hint towards new materials able to satisfy the specific need of higher operation frequency, higher output power and higher operation voltages.

The use of *wide bandgap* (WBG) materials can be considered as the best solution to meet the requirements of modern power electronics. In fact, WBG semiconductors such as silicon carbide (SiC) and gallium nitride (GaN), have been known to exhibit superior electrical characteristics compared to Si because of their inherent advantages such as high electron mobility, higher breakdown field strength and larger energy bandgap. Indeed, significant advances have been accomplished in the recent past in the growth, doping and devices processing technologies of wide bandgap materials, opening new avenues in semiconductor electronics in general, and high power electronics in particular [23].

While SiC has shown in the last two decades the most progress with respect to improved material quality and device processing, GaN is still affected by several challenging aspects, related both to specific material issues and to a non-conventional technology if compared to Si.

GaN cannot be considered as a “new” material since its history began already in the first decades of the last century. In fact, the first synthesis of GaN was achieved in 1932 by passing ammonia (NH_3) over liquid gallium (Ga) at elevated temperatures. Anyway it was only in 1968 that the first large area GaN epitaxially grown on sapphire substrates by Hydride Vapor Phase Epitaxy (HVPE) was demonstrated. After that discover a rapid progress in the GaN technology was recorded, culminated in 1994 in the demonstration of the first high electron mobility transistor (HEMT) by M. Khan. From 1994 to our days, several progress has been achieved in the development of GaN technology. In 2000, Kaiser et al. were able to transfer

HEMT technology on Silicon substrates, growing AlGaN/GaN heterostructures by Metal Organic Chemical Vapor Deposition (MOCVD). The research of HEMTs working in normally-off operation started in 2006. Cai et al investigated the possibility to obtain normally-off AlGaN/GaN HEMTs by the introduction of fluorine ions in the AlGaN barrier layer. Over the years, several possibility has been investigated in order to reach normally-off AlGaN/GaN HEMTs. Another milestone achieved over the years in GaN technology was the use of dielectric films to insulate the gate electrode. In fact Sugiyama showed as the use of an insulating layer, not only brings benefit in order to leakage current, but also can bring several benefits in terms of threshold voltage, in the goal to achieve a normally-off devices. In addiction, in 2012, an important step in GaN technology was achieved, consisting in the growth of AlGaN/GaN heterostructures on 200 mm diameter Si(111).

Table 1.1 summarizes chronologically the most important achievements of the scientific research on GaN.

Year	Discovery	REF
1932	First synthesis of GaN	Johnson and Parsons, Crew [24]
1938	Production of a powder composed by needles and platelets in order to study the crystal structure and the lattice parameters of GaN	Juza and Hahn [25]
1959	First photoluminescence measurement on small GaN crystals	Grimmeiss *et al* [26]
1968	First large area GaN epitaxially grown on sapphire substrates by Hydride Vapor Phase Epitaxy (HVPE)	Maruska and Tietjen [27]

1971	Fabrication of the first GaN light emitting diode (LED)	Pankove *et al* [28,29]
1972	Using magnesium (Mg) as p-type dopant was fabricated the first HVPE GaN LED, emitting at a wavelength of 430 nm (violet)	Maruska *et al* [30]
1986	Fabrication of improved GaN films grown by Metal Organic Chemical Vapor Deposition (MOCVD) on sapphire substrates	Amano *et al* [31]
1989	The first p-type conducting GaN films was achieved	Amano *et al* [32]
1991	Possible introduction at low temperature (450-600 °C) GaN nucleation layer to prevent defect generation	Nakamura [33]
1992	Mg activation by thermal annealing First individuation of a two-dimensional electron gas (2DEG) formation at an AlGaN/GaN heterojunction grown by MOCVD	Nakamura et al. [34] Khan et al. [35]
1993	First HEMT on GaN grown by MOCVD on sapphire substrates Theoretical prediction of piezoelectric effect in AlGaN/GaN	Khan et al [17] Bykhovski et al. [36]
1994	Fabrication of the first AlGaN/GaN HEMT	Khan et al [37]
1995	First AlGaN/GaN heterostructure achieved by MBE on sapphire	Ozgur et al. [38]

1996	Doped channel AlGaN/GaN HEMT	Khan et al. [39]
1997	Quantification of piezoelectric effect AlGaN/GaN HEMT on SiC	Asbeck et al. [40] Binari et al. [41]
1998	First GaN MOSFET	Ren et al. [42]
1999	First GaN BJT (Bipolar Junction Transistor)	Yoshida et al. [43]
2000	First GaN HBT (Heterostructure Bipolar Transistor) AlGaN/GaN 2DEG by MOCVD on Si	Zhang et al. [44] Kaiser et al. [45]
2001	AlGaN/GaN HEMT by MBE on Si	Semond et al. [46]
2003	Design of GaN-based heterostructures with Back Barrier	Maeda et al. [47]
2004	Reliable Ohmic contact on n-GaN technology	Mohammad et al. [48]
2006	Normally-off AlGaN/GaN HEMT with use of fluorine plasma process First recessed-gate structure for normally-off AlGaN/GaN HEMT	Cai et al. [49] Saito et al. [50]
2007	Normally-off AlGaN/GaN HEMT with Thin InGaN cap layer	Mizutani et al. [51]
2009	First normally-off AlGaN/GaN HFET with p-type GaN Gate	Uemoto et al. [52]
2010	Threshold voltage control using SiN_x in normally off AlGaN/GaN HFET	Sugiyama et al. [53]
2011	AlN/GaN MOS-HEMTs with thermally	Taking et al. [54]

	grown Al_2O_3 passivation	
2012	AlGaN/GaN two-dimensional-electron gas heterostructures on 200 mm diameter Si(111)	Tripathy et al. [55]

Table 1.1: *Chronology of the most important achievements on GaN research .*

1.2 GaN crystal structure

Any III-nitride material can be found in three different crystal structures as rock salt, zinc-blend or wurtzite (see *Fig. 1.1*). For GaN, at room temperature and atmospheric pressure, the wurtzite structure is the thermodynamically stable phase and exhibits an hexagonal unit cell with a basis of four atoms, two Nitrogen and two Gallium atoms. The unit cell of wurtzite structure is depicted in *Fig. 1.2*. It contains six atoms and it is characterized by two lattice constants, a_0 (3.18 A) and c_0 (5.18 A). The Ga and N atoms are arranged in two interpenetrating hexagonal close packed lattices (HCP), each one with one type of atoms, shifted 3/8 c_0 each other [56]. The covalent bonds allow that each atoms is tetrahedrally bonded to four atoms of the other type. There is also a ionic contribution of the bound due to the large difference in electronegativity of Ga and N atoms. On a wurtzite structure there is no inversion symmetry on the [0001] direction (*c axis*). This latter means that it is possible to distinguish two different orientation of GaN crystals, i.e., Ga-face and N-face, depending if the material is grown with Ga or N on top and corresponding to the (0001) and $(000\bar{1})$ crystalline faces as is shown in *Fig. 1.3a*.

The presence of the nitrogen, because of its strong electronegativity, leads to a strong interaction between the covalent bonds. The ionicity induced by the Coulomb potential of the N atomic nucleus is responsible for the formation of a polarization effect in all the material along the [0001]

direction (see *Fig. 1.3b*). This effects is called *spontaneous polarization* P_{SP}, because it exists also without any introduced stress or strain. In the [111] direction of zinc-blend crystals (i.e. GaAs, GaN, AlN) there exists a similar phenomenon but with a less pronounced behaviour because the smaller ionicity of the covalent bond.

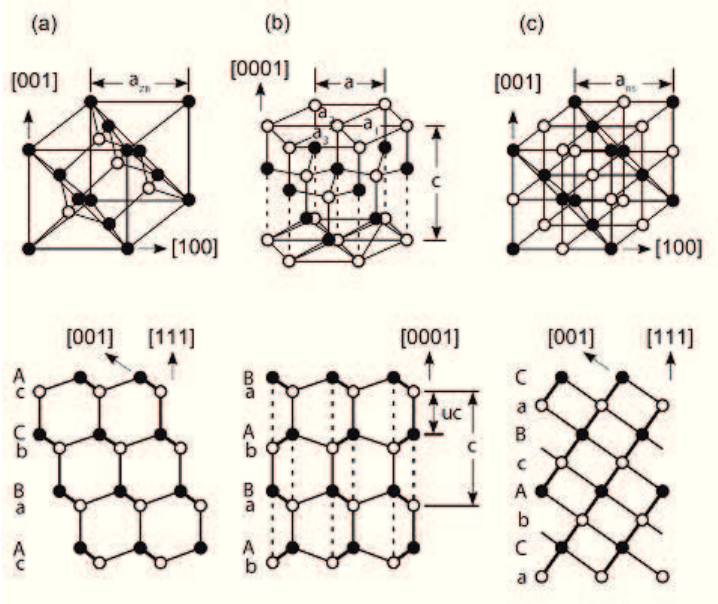

Fig. 1.1: *Crystal example of (a) zinc blende, (b) wurtzite, and (c) rock salt structures.*

The strength of the spontaneous polarization depends on the non-ideal (asymmetric) structure of the crystal. Not only the covalent bond in the direction parallel to c_0 plays an important role, but also the other three covalent bonds of the tetrahedral structure. Their resultant polarization is aligned with c_0 but in a opposite direction, compensating the polarization in the [0001] direction. For this reason in a wurtzite structure, the ratio c_0/a_0 play a fundamental role for the spontaneous polarization, where the resultant P_{SP} increases with reducing the asymmetry of the crystal, i.e. decreasing the c_0/a_0 ratio. For example an GaN crystal with a c_0/a_0 ratio of 1.6259 will present a reduced P_{SP} (-0.029 C/m^2) with respect to an AlN crystal (-0.081 C/m^2) with a c_0/a_0 ratio of 1.6010.

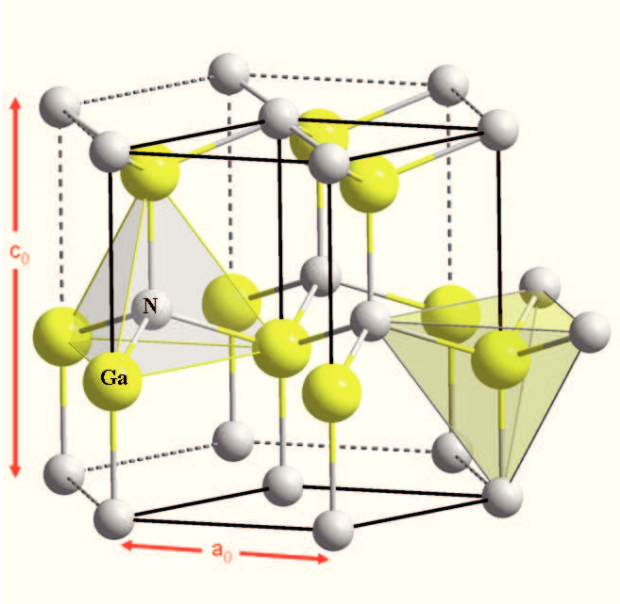

Fig. 1.2: *The wurtzite unit cell of GaN with lattice constants a_0 and c_0.*

In this context, in the presence of factors that may change the ideality of the structure and the c_0/a_0 ratio, as stress or strain, the total polarization will be modified.

The additional contribution to the polarization, due to the presence of strain and stress in the crystal, is the so called *piezoelectric polarization* P_{PE} . This contribution is particularly important in AlGaN/GaN heterostructures for the generation of the two dimensional electron gas and will be discussed in the next chapter.

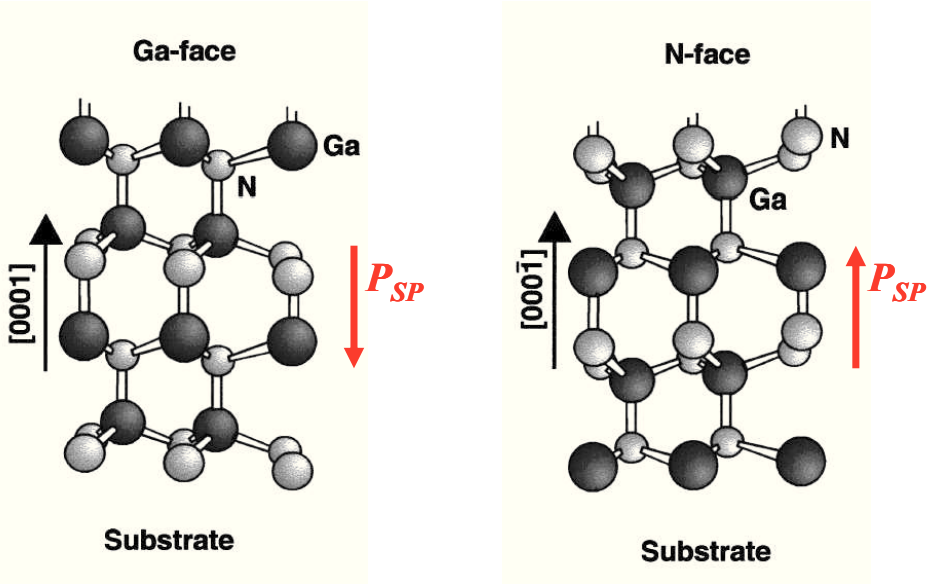

Fig. 1.3: *Schematic drawing of the crystal structure of wurtzite Ga-face and N-face GaN. The spontaneous polarization vector is also reported.*

1.3 Propierties of GaN

Thanks to its superior physical properties, GaN is considered an outstanding materials for opto-electronics, high power and high frequency devices. Properties like the wide band-gap, the high value of critical electric field and the saturation velocity can represent a big advantage in terms of electronic devices applications. In *Table 1.2*, some of these properties, which are relevant for electronic devices performances, are reported and compared to other semiconductors counterparts [57].

The wide band-gap of GaN (3.39 eV) is responsible for the high critical electric field (3.3 MV/cm), which is one order of magnitude higher than that of Si. The high critical electric field gives the possibility to sustain the application of high bias values, thus making the material suitable for high-voltage devices fabrication. A further implication of its wide band-gap is the

low intrinsic electron concentration n_i . The value of n_i in GaN at room temperature is in fact several orders of magnitude lower with respect to that of Si or GaAs, and comparable with that of SiC. This characteristic enables to increase the maximum operation temperature of the devices made of this material and have reduced leakage currents.

Materials / ***Properties***	*Si*	*SiC (4-H)*	***GaN***	*GaAs*	*Diamond*
Bandgap Energy (E_g), eV	1.12	3.26	**3.39**	1.42	5.45
Electric breakdown field (Ec), MV/cm	0.3	3.0	**3.3**	0.4	5.6
Intrinsic electron concentration (n_i), cm^{-3}	1.5×10^{10}	8.2×10^{-9}	$\mathbf{1.9\times10^{-10}}$	1.5×10^{6}	1.6×10^{-27}
Electrons saturation velocity (v_{sat}), $\times10^7$ cm/s	1.0	2.0	**2.5**	1.0	2.7
Electron mobility (μ), $cm^2/V\cdot s$	1350	700	**1200**	8500	1900
Thermal conductivity (k), W/cm·K	1.5	3.3 - 4.5	**1.3**	0.5	20
Relative permittivity (ε_r)	11.8	10.1	**9.0**	13.1	5.5

Table 1.2: *Properties of GaN compared with other conventional and wide band-gap semiconductors at room temperature [58].*

Other parameters that describe the quality of the material are the relative permittivity (ε_r) and the thermal conductivity (k). The relatively high permittivity value (ε_r) is a good indicator of the capacitive loading of a transistor and passive components. On the other hand, the thermal conductivity (k) describes the ease of heat conduction and, hence, the possibility to efficiently extract the dissipated power from the device. Materials with a lower thermal conductivity typically lead to a device degradation at elevated temperatures. Although III-V semiconductors typically have a moderate value of k, GaN has a thermal conductivity which is comparable to that of Si (but lower than SiC).

The amazing properties of GaN include also a high electrons saturation velocity (v_{sat}), which in turn is important for high current and high frequency operation of devices. Compared to other wide band gap materials that show high v_{sat}, GaN can also reach an high electron mobility (μ) comparable with Si.

Undoubtedly, among wide band gap semiconductors, the unique feature of GaN is the possibility to make *band gap engineering* considering the related $Al_xGa_{1-x}N$ alloys. In particular, by varying the Al content it is possible to tailor the band gap of the material. In this way, AlGaN/GaN heterostructures can be fabricated, allowing to reach carrier mobility up to 2000 $cm^2/V \cdot s$ in the *two dimensional electron gas (2DEG)* formed at the interface. The formation of 2DEG and the huge potentialities of AlGaN/GaN heterostructures will be described in the next chapter.

In the last decade, the most significant efforts in GaN research for electronics devices applications have been focused on the study and on the development of Schottky diodes and HEMTs. In fact, rectifyiers and switches are basic component of many electronics systems and power modules. As an example of applications, electric power converters are integrated practically in all the electronic systems to convert either DC or AC current. Their efficiency is also related to the possibility to have fast switching elements with increased power density. Typical applications of efficient power converters are the energy conversion in solar systems, wind power stations and modern electric vehicles as well as for power supplies in mobile base stations and computer systems. In all the aforementioned sectors, GaN represents today an attractive material. In fact, GaN based switches have theoretically a better figure of merit with respect to Si and

SiC. *Fig. 1.4* shows the comparison between the trade-off curves of the *specific on resistance* R_{ON} *vs breakdown voltage* for Si, SiC and GaN [59].

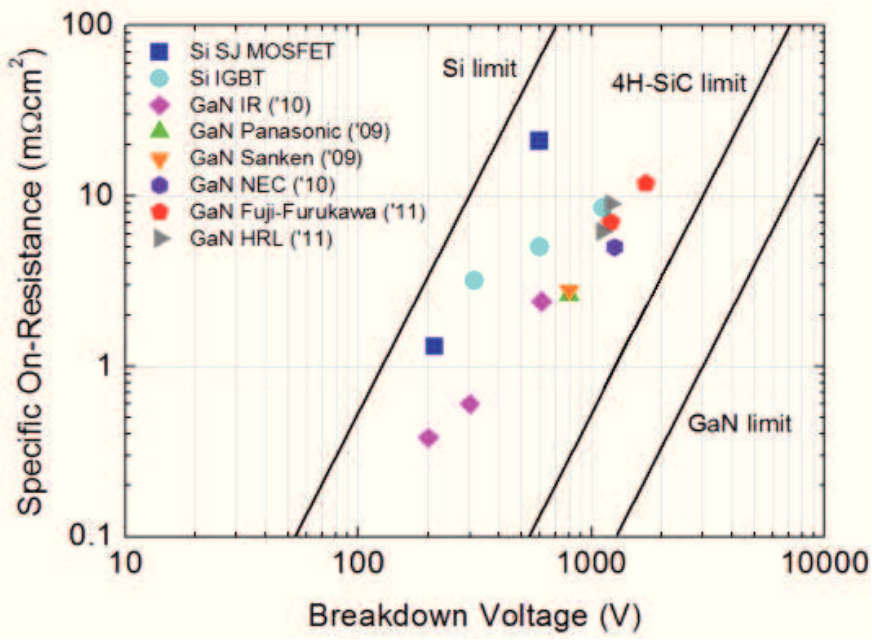

Fig. 1.4: *The Specific On-Resistance* (R_{ON}) *versus Breakdown Voltage* (V_{BR}) *for Si, SiC and GaN.*

Some experimental data related to GaN devices taken from the literature are also reported. As can be seen, at a given operation voltage, the on-state resistance of GaN devices can, in principle, outperform the competing Si or SiC devices. Since the specific on resistance is strictly related to the power losses of the device, the use of GaN can significantly lead to a reduction of the losses and to an improvement of the efficiency of the electronic systems. However, at can be seen, the experimental data point are still far from the theoretical limits of the material.

To better compare the potential power electronic performance for different semiconductors materials, *figures of merit* (FOM) are commonly adopted. In particular, for high power and high frequency devices three important FOM are considered, Johnson (JFOM), Baliga (BFOM) and

Baliga high frequency (BHFOM). $JFOM=(v_{sat}\cdot E_C)^2$ is an indication of the maximum capability to energize carriers by electric field, $BFOM=\mu\cdot\varepsilon_S\cdot E_C^3$ measures the minimum conduction losses during DC operation and $BHFOM=\mu\cdot E_C^2$ give information about the minimum conduction losses during high frequency operation. All these figures of merit for GaN are reported in *Table 1.3* and compared to Si and SiC, clearly showing that GaN is potentially a superior material for the high power and high frequency applications.

Materials / ***Figure of merit***	*Si*	*SiC*	***GaN***
$JFOM = (v_{sat}\cdot E_C)^2$	6×10^{10}	3.6×10^{13}	$\mathbf{14.6\times10^{13}}$
$BFOM = \mu\cdot\varepsilon_S\cdot E_C^3$	248	20.9×10^{4}	$\mathbf{79\times10^{4}}$
$BHFOM = \mu\cdot E_C^2$	84	7200	**20800**

Table 1.3: *Figures of merit JFOM, BFOM and BHFOM for Si, SiC and GaN.*

A comparison of the typical operating frequency and output power range for different semiconductor materials is shown in *Fig. 1.5*. In this case, it must be noted that with respect to SiC, GaN is more suitable for higher frequencies but in a lower output power range.

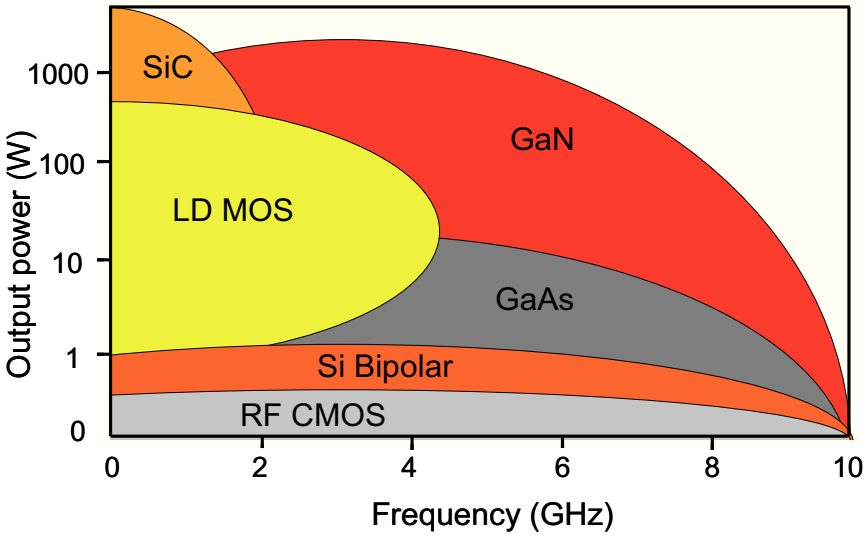

Fig. 1.5: *Typical operating frequencies and output power ranges of electron devices made using a different semiconductor materials. Figure adapted from [60]*

1.4 Substrates and growth techniques

In spite of its outstanding material properties, the technological development of GaN has come later than in other semiconductors. The reasons of this delay were mainly related to the difficulty to have high quality free-standing GaN substrates and, consequently, the difficulty to fabricate vertical structures for power devices. In fact, for the growth of GaN other materials must be used as substrate. Since the perfect substrate does not exist, an ideal candidate must have physical and crystallographic properties, such as lattice parameters and thermal expansion coefficients, close to those of GaN, in order to avoid the formation of cracking of the film, or defects formation during the growth of the material. The lattice mismatch and the difference in *thermal expansion coefficients* (TEC) of the common substrates used for GaN growth are reported in *Table 1.4*.

Different substrates have been used for GaN growth. Sapphire (Al_2O_3) has been the most common substrate used for GaN heteroepitaxy for optoelectronics applications (like LEDs). Sapphire is an interesting choice because it is insulating, it can withstand the required high growth temperatures, and it is relatively cheap. Anyway the large lattice mismatch (+16%), and large thermal expansion coefficient mismatch (-25.3%) with the GaN epilayers do not make it the most convenient choice. A better substrate, in terms of lattice and thermal expansion coefficient mismatch, is the hexagonal silicon carbide (6H-SiC). The lattice mismatch for (0001)-oriented GaN films is smaller and the thermal conductivity is higher compared to the values of sapphire. In this case, however, the substrate cost represents a limiting aspect. Additionally, in spite of the minimal lattice mismatch, a high defect density (10^7-10^9 cm^{-2}) is still observed in GaN layers grown on SiC [61].

Silicon can be also a possible substrate for the growth of GaN layers. In the recent years, GaN materials grown on Si is attracting a huge attention thanks to the low substrate cost, the possibility of large substrate diameters and the potential integration with the well developed Si electronics technology. Despite a large lattice (+17%) and a thermal expansion coefficient (+55.5%) mismatch, GaN devices fabricated on Si substrates can have performance at the same level than those obtained on Sapphire or SiC substrates. Anyway this large mismatch is typically responsible for the formation of defects and cracks on the material. The main problem to the growth of GaN on Si substrate comes from the compressive stress generated during the growth. For this reason, to achieve a good material quality, the stress has to be minimized. Fu et al [62] showed that the residual stress is depending on the growth condition and cool-down procedure. Moreover there exists a dependence of the stress on the impurity concentrations, that lead to an increase of the tensile stress with increasing the doping concentration [63]. To relieve the tensile stress and achieve crack-free GaN heterostructures, several kind of transition layers can be used, such as low temperature AlN [64], graded AlGaN buffers [65] or AlGaN/GaN superlattices [66]. It has been seen that the dislocation density in the material strongly depends on the choice of the transition layer, and can be partially mitigated by using a high temperature AlGaN intermediate layer that acts as a dislocation filter [67]. Moreover transition layers increase also the series

resistance in the GaN layer, reducing the crack density and providing a good electrical insulation from the substrates. Recently, crack-free AlGaN/GaN heterostructures grown on 200 mm diameter (111)-oriented silicon substrates has been demonstrated [16]. This results represent an important step for the full integration of GaN technology with silicon process foundries based on CMOS (Complementary Metal Oxide Semiconductor) technology. In order to obtain high quality AlGaN/GaN heterostructures on 200 mm Si substrate, thick GaN buffer layers (in the order of 2.4-2.5 μm) were grown.

Substrate	***Lattice mismatch***	***Difference in thermal expansion coefficient (TEC)***
Al_2O_3 (0001)	+ 16 %	- 25.3 %
6H-SiC (0001)	+ 3.5 %	+ 33.3 %
3C-SiC (111)	+ 3 %	+ 24.4 %
Si (111)	- 17 %	+ 55.5 %
AlN (0001)	+ 2.5 %	+ 33.3 %

Table 1.4: *Lattice mismatch and difference in thermal expansion coefficient of GaN with respect to the most common substrates*

If the choice of a suitable substrate is an important issue for the development of GaN technology, not less important are the growth techniques employed to obtain a high quality material, with a low concentration of defects. The first technique used to grow epitaxial GaN layers was the Hydride Vapor Phase Epitaxy (HVPE). This technique remained the most commonly used method until the early 1980s. In this technique the gallium monochloride (GaCl) precursor is synthesized inside a reactor by the reaction of hydrochloric acid (HCl) with liquid Ga at temperatures between 750 °C and 900 °C. Then the GaCl, transported in

some proper substrates, will react with the ammonia (NH_3) at 900-1100 °C forming the GaN film. Finally the exceeding substrate can be removed by system such as laser ablation. HVPE have a really high growth rate (100 μm/hr), useful more for large area quasi substrate that have to be later completed by other epitaxial techniques as MOCVD and MBE.

Nowadays, the Metal Organic Chemical Vapor Deposition (MOCVD) has become the most used method to grow GaN, owing its superior quality as high degree of composition control and uniformity, reasonable growth rates (1-2 μm/hr), the possibility to use high purity chemical sources and to grow abrupt junctions. MOCVD uses the reaction of trimethylgallium (TEGa) and NH_3 that occurs close the substrate. To obtain high quality GaN film, during the deposition the substrate must be kept at a temperature of about 1000 °C - 1100 °C, to allow a sufficient dissociation of the NH_3 molecule, at a pressure between 50 and 200 Torr. Moreover, another critical aspect is the control of the N/Ga molar ratio, that must be kept high in order to compensate N losses due to the high partial nitrogen pressure at the elevated growth temperatures [68].

In fact the poor nucleation of GaN on Si at high temperatures results in a reaction of nitrogen with Si and in a Ga-Si alloy formation which initiates a strong and fast etching reaction (melt back etching) destroying the substrate and the epitaxial layer [69]. The most established method to prevent the nitridation is starting the growth process with an AlN nucleation larger grown in the same reactor with a few monolayers pre-deposition of Al. [70]

The material doping can be tailored by the induction of extra precursor on the reactor, as silane (SiH4) for Si doping (n-type) or bis-cyclopentadienylmagnesium (Cp_2Mg) for Mg doping (p-type). Anyway the control of a low doping concentration ($N_D < 1\times10^{16}$ cm^{-2}) is still a complex factor because the formation of nitrogen vacancies, which act as donors leading to n-type doping of the material. Also the oxygen impurities present during the growth process can act as donors, leading to a n-type material [71].The p-type GaN epitaxial layer that were used in this work of thesis has been obtained by the use of Mg as dopant specie.

To improve the crystalline quality of the grown GaN, pre-treatments can be required. For example the deposition of a thin low temperature buffer layer can be an advantage. The use of this layer, generally AlN or Si, can

reduce the lattice mismatch, providing a benefit in terms of defects density (dislocations, oxygen impurity, nitrogen and gallium vacancies, etc).

To reduce the defects density in the grown material, a different process called lateral epitaxial overgrowth (LEO) has been also developed [72]. It consists in the deposition of GaN on a patterned dielectric substrates (like SiO_2) followed by the lateral expansion and coalescence of the grown material. Although this technique can lead to a significant reduction of the dislocation density (up to 6×10^7 cm^{-2}), the extremely high cost of the process (which require the employment of lithographic steps for the substrate preparation) has limited its practical application for GaN growth.

The Molecular Beam Epitaxy (MBE) is a slow (1 μm/hr) but efficient technique for GaN growth, that show comparable material quality to those grown by MOCVD. A problem is that the NH_3 is very stable at the low temperature (700-800 °C) used in MBE. To solve this issues reactive species of nitrogen, generated by electron cyclotron resonance (ECR) or radio frequency (RF) plasmas with low energy, are generally used [73].

In this work of thesis, mostly GaN layers grown on 150 mm Si (111) substrates, supplied by ST Microelectronic, were used. GaN has been growth by MOCVD using precursor as trimethylgallium (TEGa) and NH_3. Also GaN material grown on 2 inch Al_2O_3 wafers, supplied by the Institute of High Pressure Physics of Warsaw, has been used for the some experiments.

Chapter 2: AlGaN/GaN heterostructures: physics and devices

One of the most interesting aspects related to GaN materials is the possibility to grow AlGaN/GaN heterostructures, in which a two dimensional electron gas (2DEG) is formed at the heterojunction. In this chapter, the physics of AlGaN/GaN heterostructures is discussed, considering the band structure and the piezoelectric polarization of the materials to explain the formation of the 2DEG. Moreover, the operation principle of HEMTs devices is described. In the last paragraph, the possible approaches to obtain normally-off HEMTs in GaN will be briefly discussed.

2.1 $Al_xGa_{1-x}N$ alloys

As pointed out in the previous chapter, GaN is characterized by the possibility to grow heterostructures based on $Al_xGa_{1-x}N$ alloys.

The peculiarity of $Al_xGa_{1-x}N$ alloys is the possibility to tailor the lattice constant and the energy gap by varying the Al concentration x.

In particular, the in-plane lattice constant a of $Al_xGa_{1-x}N$ alloys depends on the Al concentration x, and is also related to the lattice constant of GaN and AlN by the relation [74]

$$a^{AlGaN}(x) = x a^{AlN} + (1-x) a^{GaN} \qquad \text{(Eq. 2.1)}$$

On the other hand, also the band gap of a $Al_xGa_{1-x}N$ alloy can be expressed as a function of the Al mole fraction [75] according to

$$E_g^{AlGaN}(x) = xE_g^{AlN} + (1-x)E_g^{GaN} - x(1-x) = [x \cdot 6.13 + (1-x) \cdot 3.42 - x(1-x)] \ eV \quad \text{(Eq. 2.2)}$$

The dependence of the lattice constant and of the band gap energy on the Al mole fraction in a $Al_xGa_{1-x}N$ are reported on *Fig. 2.1a* and *Fig. 2.1b* respectively. A schematic of the crystal structure for AlGaN/GaN heterostructure is represented in *Fig. 2.2*.

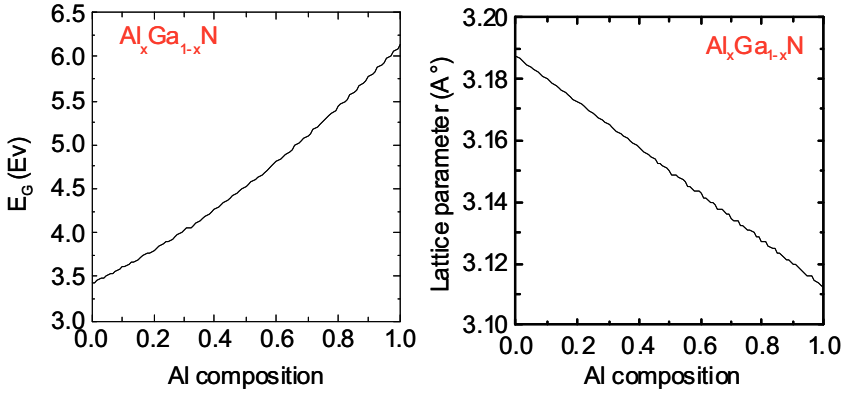

Fig. 2.1: *Dependence of the band gap energy (a) and of the lattice parameter a (b) on the Al mole fraction for the $Al_xGa_{1-x}N$.*

The big advantage of AlGaN/GaN heterostructures consists in the formation of a *two dimensional electron gas* (2DEG) at the interface, generated by the strain induced by the lattice mismatch between GaN and AlGaN. The presence of the 2DEG allows the fabrication of an innovative device called *High Electron Mobility Transistor (HEMT)* that will be discussed in the following paragraphs.

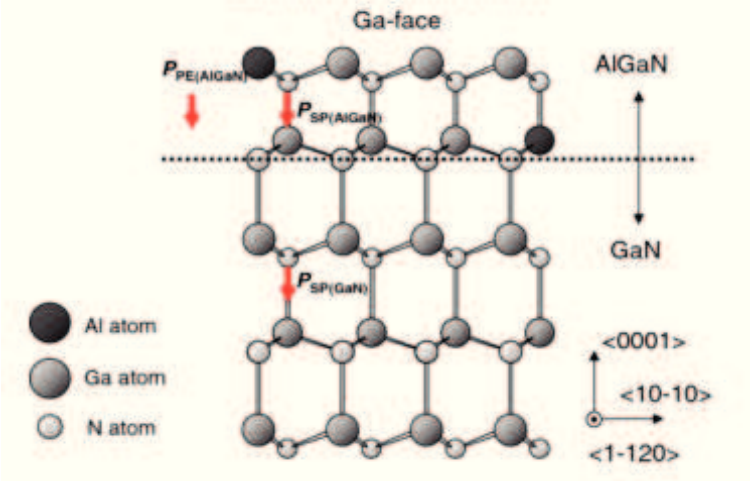

Fig. 2.2: *Schematic of the structure for AlGaN/GaN heterostructure.*

2.2 Formation of two dimensional electron gas (2DEG) in semiconductor heterostructures

In general, when a n-type doped wide band gap semiconductor layer is brought into contact with a narrow band gap semiconductor layer, an electrons transfer will occur, accompanied by a band bending in the upper part of the narrow band gap semiconductor. In this way, a triangular well is formed, in which the transferred electrons are confined and form a two dimensional conductive channel (see *Fig. 2.3*). The electrons of the n-type doped barrier layer collected in the quantum well are commonly referred as two dimensional electron gas (2DEG), since they behave as free particles in two directions (in the plane of the interface) while their motion is quantized only in orthogonal direction. The separation of electrons from their donor atoms N_D reduces the Coulomb scattering and leads to a high mobility of the electrons in the 2DEG. The possibility to have a significant increase of the

free carrier concentration within a semiconductor layer without the intentional introduction of dopant impurities is often referred as *modulation doping*.

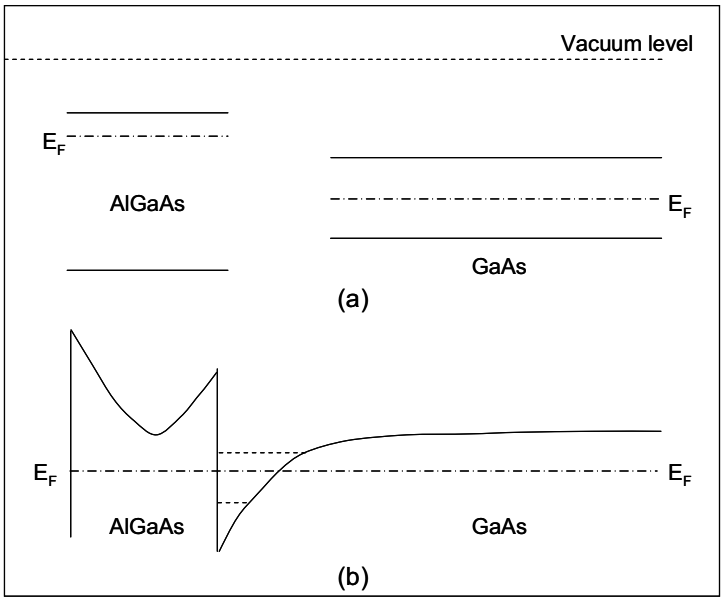

Fig. 2.3: *The energy band diagrams of the AlGaAs and GaAs layers when apart and in equilibrium (a) and the energy band diagrams after the formation of the AlGaAs/GaAs heterostructures (b).*

An example of this situation can be found in the AlGaAs/GaAs heterostructures. When the two semiconductors are separated (*Fig. 2.3a*) the Fermi level in AlGaAs will be closer to the conduction band edge with respect to its position in the GaAs, since the AlGaAs is intentionally n-type doped. When the two semiconductors are put in contact (*Fig. 2.3b*), the Fermi levels will align and a transfer of electrons from the AlGaAs to the GaAs layer occurs. This effect significantly increases the electron concentration at the interface with the GaAs layer, without any introduction of ionized donor impurities. To maintain the charge neutrality of the system, the electrons flowing towards the GaAs layer leave positive ionized donor atoms behind. The spatial separation between the ionized donors atoms (located inside the AlGaAs) and the free electrons (confined inside the

triangular well at the heterointerface) significantly reduces the Coulomb scattering of the transferred electrons by the ionized impurities effects, thus leading to an increase of the electron mobility in the 2DEG.

Hence, because of the electron transfer, the conduction band edge in the GaAs layer is strongly bent near the heterostructure. Moreover a net positive charge will be present at interface, because of the positive ionized donors. Therefore, the electrons placed in the GaAs near the interface, will be attracted to the interface by the action of the positive charge. The sharp bending of the conduction band edge and the presence of the conduction band edge discontinuity forms a potential triangular quantum well within the GaAs layer. The electrons will drop in this triangular quantum well, positioning in discrete levels of energy, called *subbands*. For this reason the electrons will be free to move in all the direction parallel to the interface, because no quantization of the space occurs, while along the direction perpendicular to the interface (direction z showed in *Fig. 2.4*), they are confined by band bending in the quantum well close to the interface.

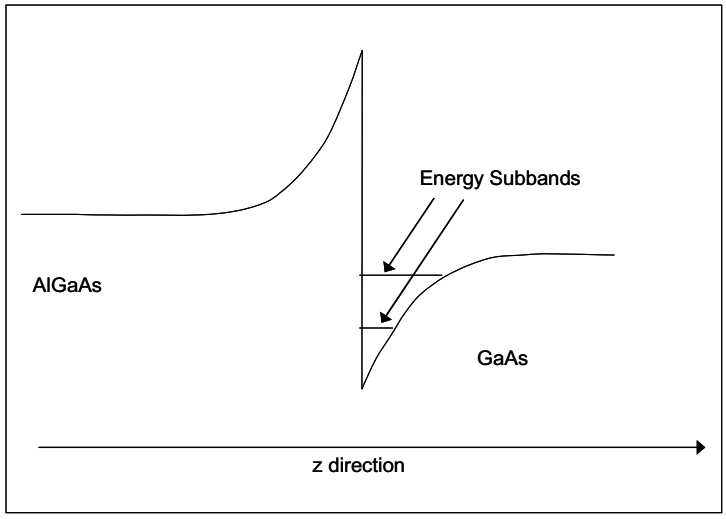

Fig. 2.4: *The conduction band edge discontinuity in the n-AlGaAs and i-GaAs heterojunction, showing two energy subbands*

2.3 2DEG formation in AlGaN/GaN heterostructures

As explained in the Chapter 1, a spontaneous polarization is present in GaN. However, due to the piezoelectric nature of the material, when an AlGaN/GaN heterostructure is formed, the strain induced by the lattice mismatch generates an additional contribution to the polarization, namely, the *piezoelectric polarization* P_{PE}.

For this reason, in contrast to the conventional III-V semiconductors (like the example of AlGaAs/GaAs heterojunction described in paragraph 2.2) where a n-type doped barrier layer is necessary to provide the charges for the 2DEG formation, a different situation occurs in AlGaN/GaN systems. In this case, due to the presence of the piezoelectric polarization the formation of a high sheet charge density in the 2DEG is possible even using undoped layers. The possibility to use undoped layers in AlGaN/GaN systems (with respect to other system like n-type doped AlGaAs/GaAs heterojunction) further reduces the Coulomb scattering, leading to an enhanced electron mobility in the 2DEG.

As schematically drawn in *Fig. 2.5*, when an AlGaN/GaN heterojunction is formed the piezoelectric and the spontaneous polarization act in the same direction, thus leading to an overall increase of the total polarization. This is the case when a tensile strain is applied to the crystal. The strength of the piezoelectric polarization P_{PE} is related to the piezoelectric coefficients e_{33} and e_{31} through the relation:

$$P_{PE} = e_{33} \cdot \varepsilon_z + e_{31} \cdot (\varepsilon_x + \varepsilon_y) \qquad \text{(Eq. 2.3)}$$

where $\varepsilon_z=(c-c_0)/c$ is the strain along the c-axis, $\varepsilon_x=\varepsilon_y=(a-a_0)/a$ are the in-plane strains assumed to be isotropic, and a_0 and c_0 are the equilibrium lattice constants. The relations between the lattice constants *a* and *c* of the hexagonal GaN is given by

$$\frac{c-c_0}{c_0} = -2\frac{C_{13}}{C_{33}} \cdot \frac{a-a_0}{a_0} \qquad \text{(Eq. 2.4)}$$

where C_{13} and C_{33} are the elastic constants. In order to take into account the piezoelectric polarization in the direction of the c-axis, the following relation is considered:

$$P_{PE} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) \qquad \text{(Eq. 2.5)}$$

Table 2.1 report the lattice parameters, piezoelectric constants, elasticity constants, and spontaneous polarization for GaN and AlN [76][77].

Parameter	***AlN***	***GaN***
a_0 *(nm)*	0.3112	0.3189
e31 (C/m^2)	-0.60	-0.49
e33 (C/m^2)	1.46	0.73
C_{13} *(GPa)*	108	103
C_{33} *(GPa)*	373	405
$P_{SP}(C/m^2)$	-0.081	-0.029

Table 2.1: *Values for lattice parameters, piezoelectric constants, elasticity constants, and spontaneous polarization for GaN and AlN*

Since the term $\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)$ is always negative independent of the composition of the AlGaN barrier layer, the piezoelectric polarization will be

negative for tensile strain ($a > a_0$) and positive for compressive strain ($a < a_0$). In the case of Ga-face heterostructures, the spontaneous polarization vector of GaN will be pointing towards the substrate (negative). For this reason the alignment between spontaneous and piezoelectric polarization will be parallel in case of tensile strain and antiparallel in case of compressive strain. On the other hand, considering the N-face, the spontaneous and piezoelectric polarization will have the opposite signs, with the vector of the spontaneous polarization pointing in the reverse direction, away from the substrate. The directions of the *spontaneous (P_{SP})* and *piezoelectric polarization (P_{PE})* are shown in *Fig. 2.5*, where also the polarization induced sheet charge density (σ) is indicated.

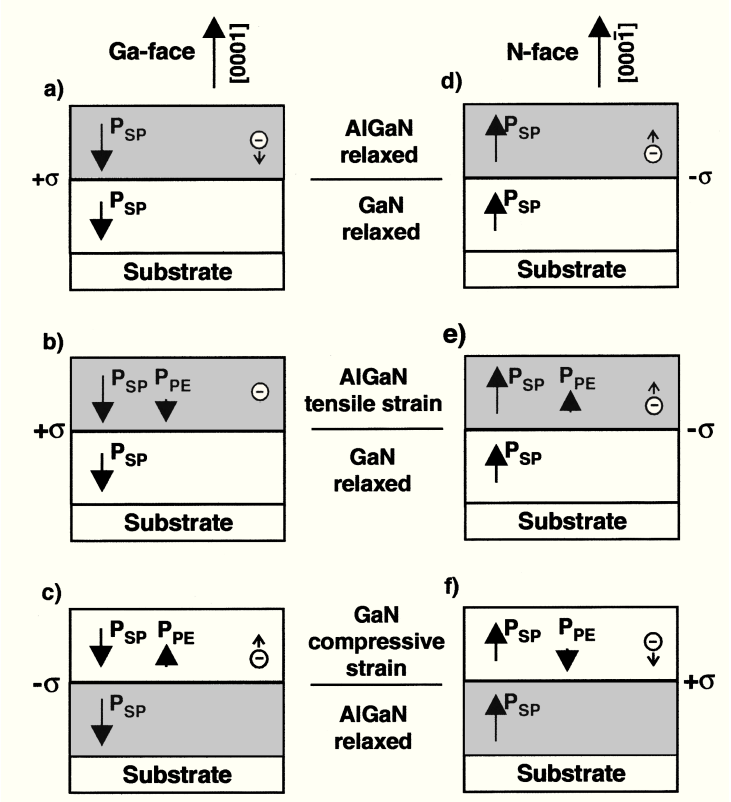

Fig. 2.5: *Spontaneous and piezoelectric polarization in Ga- and N-face strained and relaxed AlGaN/GaN heterostructures. Figure taken from Ref. [74].*

Considering a gradient of polarization in space **P**, there exists a polarization-induced charge density $\rho_P = \nabla P$ associated to this gradient. In the presence of an abrupt interface AlGaN/GaN or GaN/AlGaN (top/bottom layer) the total polarization will create *a polarization sheet charge density σ* defined by:

$$\sigma = [P(top) - P(bottom)] = [P_{SP}(top) + P_{PE}(top)] - [P_{SP}(bottom) + P_{PE}(bottom)] \quad \text{(Eq. 2.6)}$$

Hence in an AlGaN/GaN interface, with a relaxed GaN bottom layer, it is possible to estimate the amount of sheet charge density:

$$\sigma = [P_{SP} + P_{PE}]^{AlGaN} - [P_{SP} + P_{PE}]^{GaN} = \left[P_{SP}(x) + 2\frac{a(0) - a(x)}{a(x)} \left(e_{31}(x) - e_{33}(x) \cdot \frac{C_{13}(x)}{C_{33}(x)} \right) \right] - [P_{SP}(0)] \quad \text{(Eq. 2.7)}$$

where *x* is the Al mole fraction in the AlGaN layer. Of course, considering a GaN/AlGaN heterostructures the polarization has the opposite sign and the sheet charge density will be negative.

The polarization charge is due to the piezoelectric effect in strained AlGaN and to the difference in spontaneous polarization between AlGaN and GaN. Piezoelectric constants and spontaneous polarization increase moving from GaN to AlN, so the total polarization of AlGaN layer is larger than of GaN buffer layer and therefore a positive polarization charge is present at lower AlGaN/GaN interface, for Ga-face structure. Then the electrons will tend to compensate this positive charge resulting in the formation of the 2DEG in the triangular quantum well at the AlGaN/GaN interface, whose ground subband level lies below the Fermi level E_F. In *Fig. 2.6* the band structure for a Ga-face undoped AlGaN/GaN heterostructure is shown. In the case of N-faced structures a negative polarization charge will be compensated by holes and these will be accumulated at the interface.

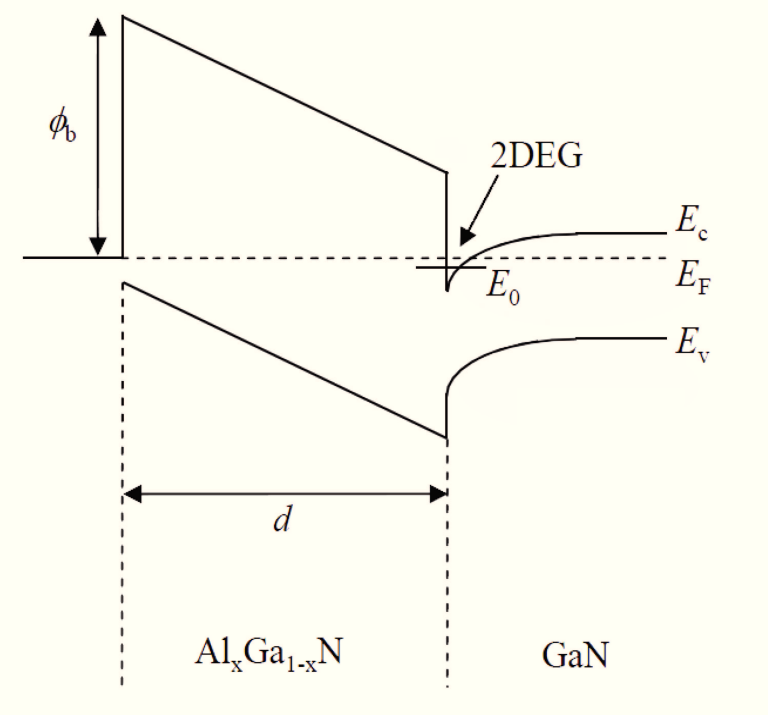

Fig. 2.6: *Energy band diagram of a Ga-face undoped AlGaN/GaN heterostructure.*

To determine the effective sheet charge density of the 2DEG, different parameters must be considered like the polarization induced bound sheet charge density at the AlGaN/GaN heterojunction σ_{int}, the Schottky barrier height ϕ_B formed at the metal/AlGaN contact, the Fermi level at the heterojunction with respect to the GaN conduction band edge E_{F0}, the conduction band offset at the AlGaN/GaN interface ΔEc and the relative dielectric constant ε_{AlGaN}, the thickness d_{AlGaN}, and the Al mole fraction x of the AlGaN barrier layer. From these parameters is possible to give an expression of the sheet charge density n_S located at the AlGaN/GaN interface by the Eq. 2.6 [78]

$$n_S(x) = \frac{\sigma_{\text{int}}}{q} - \left[\frac{\varepsilon_0 \varepsilon_{AlGaN}(x)}{d_{AlGaN} q^2}\right] \cdot \left[q\phi_B(x) + E_{F_0}(x) - \Delta E_C(x)\right] \qquad \text{(Eq. 2.8)}$$

where q is the elementary charge and ε_0 is the vacuum permittivity.

As can be seen, the sheet carrier concentration induced by the polarization sheet charge density is a function of the Al concentration *x* present in the AlGaN barrier layer. For an AlGaN/GaN heterojunction we can consider $\varepsilon_{AlGaN}(x)$ and $\phi_B(x)$given by [79]

$$\varepsilon_{AlGaN}(x) = -0.5x + 9.5 \qquad \text{(Eq. 2.9)}$$

and

$$q\phi_B(x) = 1.3x + 0.84 \ \ eV \qquad \text{(Eq. 2.10)}$$

The Fermi energy is given by [80]

$$E_F(x) = E_0(x) + \frac{\pi\hbar^2}{m^*(x)} n_S(x) \qquad \text{(Eq. 2.11)}$$

where $m^*_{AlGaN}(x) \approx 0.22 m_e$ is the effective electron mass and $E_0(x)$ represent the ground subband level of the 2DEG [81] [82]

$$E_0(x) = \left[\frac{9\pi\hbar q^2}{8\varepsilon_0 \sqrt{8m^*_{AlGaN}(x)}} \frac{n_S(x)}{\varepsilon_{AlGaN}(x)} \right]^{2/3} \qquad \text{(Eq. 2.12)}$$

According to the previous equations, the maximum sheet carrier concentration $n_s\ (x)$ appearing at the AlGaN/GaN interface can be determined. Clearly, by decreasing the Al concentration of the AlGaN barrier layer, the 2DEG density n_s decreases. The same behaviour occurs by decreasing the AlGaN thickness barrier layer. From Eq. 2.12 it can be estimated that the formation of the 2DEG is hindered for a critical thickness of the AlGaN barrier layer below 3.5 nm. At same time, it is also important to avoid too thick layer of AlGaN that can lead to relaxation of the structure and, hence, to the suppression of the piezoelectric polarization contribution. In *Fig. 2.7* the dependence of the 2DEG sheet carrier concentration n_s on the Al alloy composition *x* is shown for different values of the thickness of the AlGaN barrier layer.

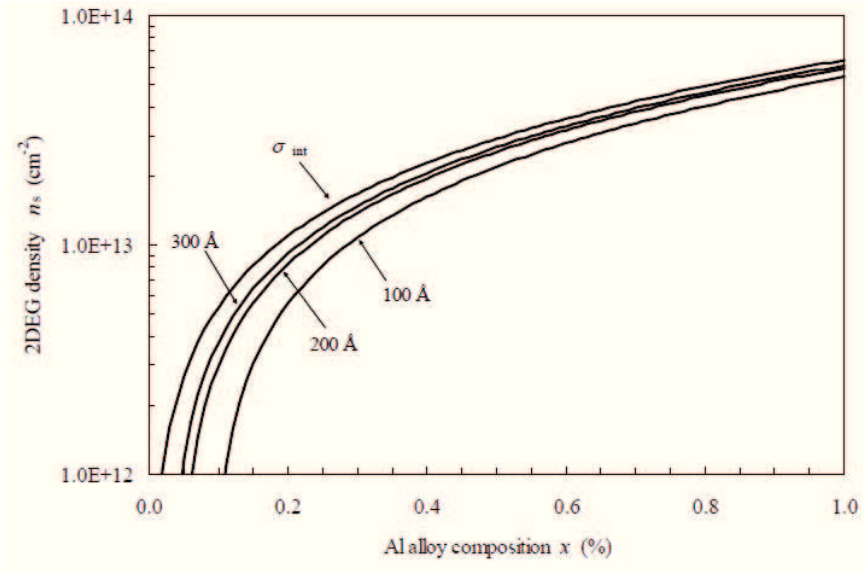

Fig. 2.7: *Calculated 2DEG density as a function of the Al alloy composition of the $Al_xGa_{1-x}N$ barrier layer for three different thicknesses. The bound polarization induced sheet charge (σ_{int}) is plotted as a reference.*

2.4 HEMT working principle

The original idea of the *high electron mobility transistor* (HEMT) based on the presence of a 2DEG, was first introduced for the AlGaAs/GaAs heterostructures and can be attributed to Takashi Mimura in 1979 [83]. The first HEMT fabricated with an AlGaN/GaN heterojunction was demonstrated only in 1991 by another pioneer in this field as M. Asif Khan [35].

The HEMT is a peculiar device, since it can offer optimal characteristics in terms of both high voltage, high-power and high frequency operation. Its operation principle is founded on the presence of the 2DEG at interface of an heterostructure, like for example an AlGaN/GaN system. It is a three

terminal device where the current between the two Ohmic contacts of *source* and *drain*, flowing through the 2DEG, is controlled by the electrode of *gate* (typically a Schottky contact). Practically, the bias applied to the gate controls the flow of electrons through the channel. *Fig. 2.8* shows a schematic of an HEMT device. To confine the electron flow in the 2DEG and isolate HEMT devices, deep trenches (cutting the 2DEG) or ion implantation are typically used.

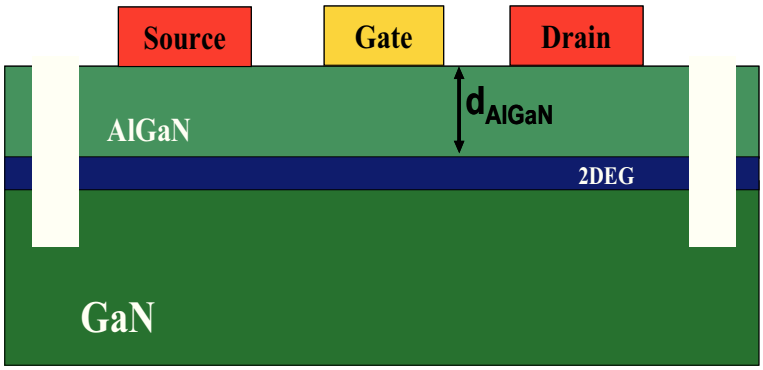

Fig. 2.8: *Schematic of AlGaN/GaN HEMT*

The *Fig. 2.9* illustrates, in a schematic band diagram of an AlGaN/GaN HEMT structure, how the 2DEG is influenced by the different gate bias conditions. This schematic is reported for the case of a n-type doped AlGaN barrier layer.

At V_g= 0 V there are allowed levels below the Fermi level in the subbands of the quantum well, resulting in the presence of a high sheet carrier concentration and in the on-state of the device. By increasing the gate bias (V_g > 0 V), the Fermi level rises, increasing the density of allowed states below the Fermi level in the conductive band, and therefore increasing the sheet carrier concentration of the 2DEG. By decreasing the gate bias V_g towards negative values (V_g < 0 V) the Fermi level drops depleting the 2DEG, until the position of the Fermi level lies below the quantum well.

Under this condition, the level in the energy subbands are completely empty and the device is in the off-state.

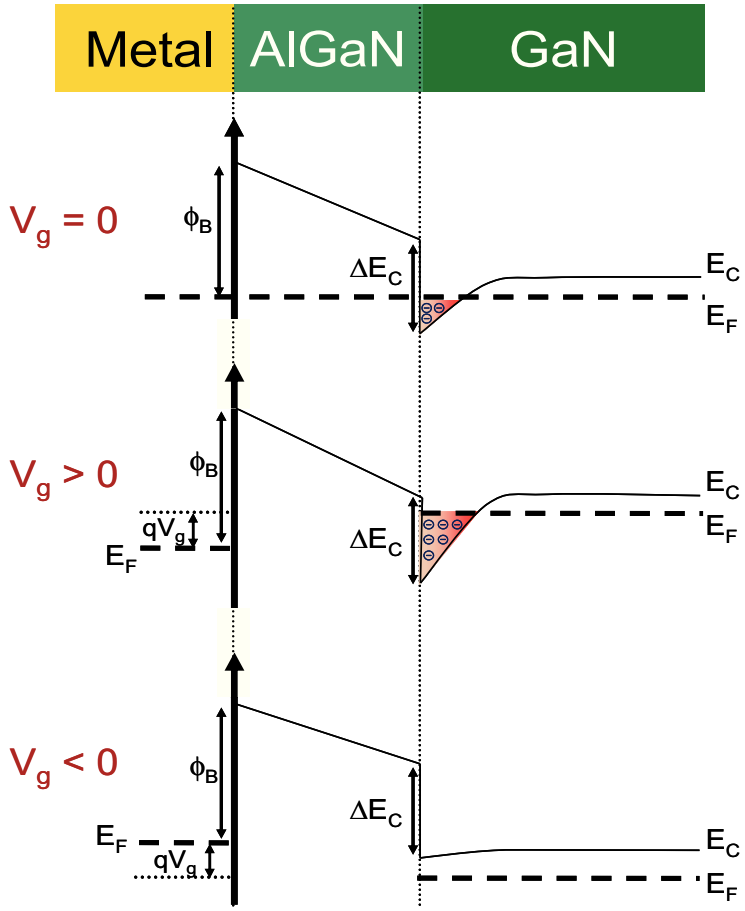

Fig. 2.9: *Schematic of the influence of the gate bias on the band diagram (and on the 2DEG) in a n-type doped AlGaN/GaN heterostructure.*

In *Fig. 2.10* typical I_{DS}-V_{DS} characteristics of a HEMT, fabricated during this work of thesis, as a function of the gate bias V_g (a) and the device transcharacteristic, i.e. the I_{DS}-Vg at a fixed V_{DS} (b), are reported as an example.

In the I_{DS}-V_{DS} characteristics by applying a positive potential difference between source and drain *(V_{DS})*, the current will start to flow in the 2DEG. By increasing the drain bias, the current flow in the channel will increase linearly up to certain value. After this value the current through the channel starts to saturate. The maximum saturation value I_{DSS} depends on the sheet carrier concentration n_S of the channel. Looking at the transcharacteristics, for a fixed V_{DS} the drain current I_D rises with a parabolic behaviour with increasing gate bias.

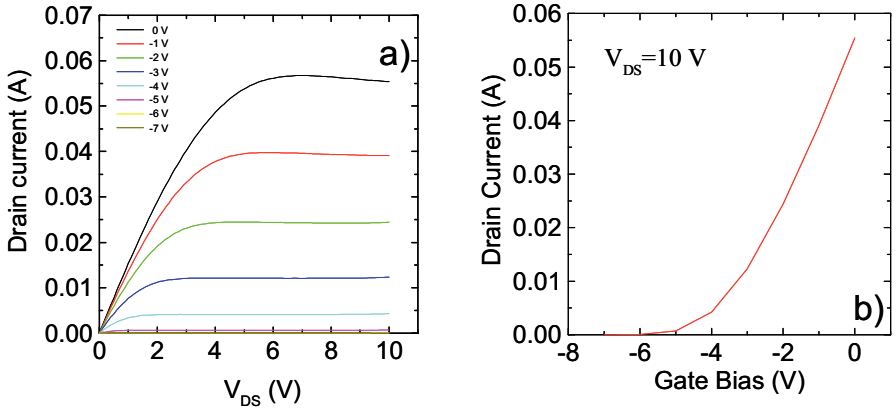

Fig. 2.10: *Example of drain current as function of V_{DS} for Vg from -7 V to 0 V (a), and drain current as function of gate voltage at V_{DS}=10 V (b)*

The drain current *(I_{DS})* can be controlled by the bias applied to the gate electrode. In particular, I_{DS} decreases with increasing the negative value of the gate bias *(V_g)*, since the region of the channel under the gate is depleted. The value of V_g which determines the pinch-off of the channel (where the sheet carrier concentration in the channel becomes zero) is called *threshold voltage (V_{th})* of the device.

In a AlGaN/GaN HEMT at any point *x* along the channel, neglecting the extrinsic series resistance of source and drain, the sheet carrier concentration depend by the applied V_g

$$n_S(x) = \frac{\varepsilon_0 \varepsilon_{AlGaN}}{q d_{AlGaN}} \left[V_g - V_{th} - V(x) \right] \qquad \text{(Eq. 2.13)}$$

where d_{AlGaN} is the distance of the gate to the 2DEG channel, corresponding to the AlGaN thickness.

The gate-to-channel capacitance (per unit of area) can be approximately assumed as independent of n_s, using the expression $C_{2DEG}=\varepsilon_0\varepsilon_{AlGaN}/qd_{AlGaN}$.

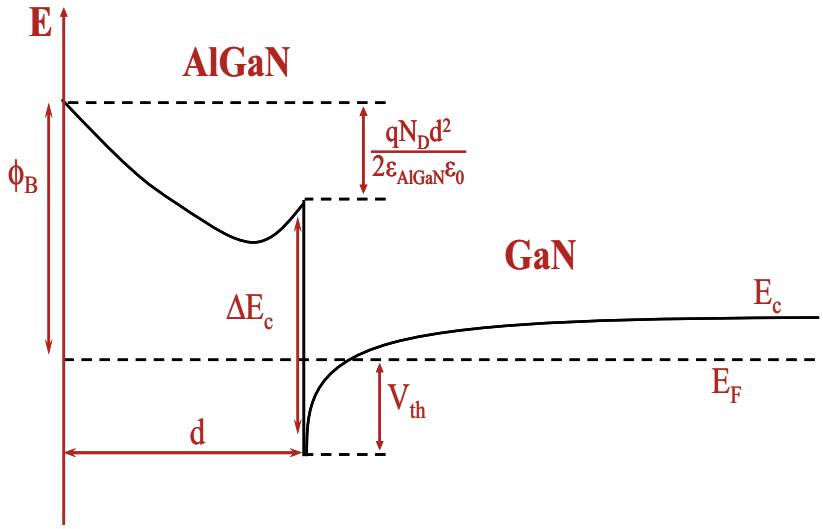

Fig. 2.11: *Schematic band diagram for AlGaN/GaN heterostructure, graphically showing the relation between the threshold voltage and other parameters.*

It is now possible to define the *threshold voltage* of the device, as the gate bias necessary to turn-off the 2DEG, resulting in a $n_S=0$. Looking at the AlGaN/GaN schematic band diagram showed in *Fig. 2.11*, is clear that the threshold voltage depends on different parameters like the Schottky barrier height ϕ_B, the conduction band offset at the AlGaN/GaN interface ΔEc, the concentration of donor atoms in the AlGaN layer N_D, the relative dielectric

constant ε_{AlGaN}, the thicknesses d_{AlGaN} and the Al concentration of the AlGaN. Besides these parameters (indicated in *Fig. 2.11*), in order to have a complete expression of the threshold voltage the contribution of the polarization induced charge density σ must be taken into account. Hence, in a simple form, the threshold voltage can be express as [84]

$$V_{th} = \Phi_B - \Delta E_C - \frac{qN_{D_{AlGaN}} d_{AlGaN}^2}{2\varepsilon_0 \varepsilon_{AlGaN}} - \frac{\sigma}{\varepsilon} d_{AlGaN} \qquad \text{(Eq. 2.14)}$$

Assuming a constant mobility and remembering the Ohmic law, for a two-dimensional electron gas the conductivity σ of the channel will be directly proportional to the sheet carrier concentration n_S and to the electrons mobility in the channel μ

$$\sigma = q \cdot n_S \cdot \mu \qquad \text{(Eq. 2.15)}$$

It is possible to write the drain current as:

$$I_D = -\mu \cdot W \cdot Q(x) \frac{dV(x)}{dx} \qquad \text{(Eq. 2.16)}$$

where *Q(x)* is the charge considered in the channel.

Integrating both sides in the all length of the channel and considering the expression of *Q(x)* we have

$$I_D = \mu \cdot \frac{W}{L} \cdot C_{2DEG} \int_{V_S}^{V_D} \left[V_g - V_{th} - V(x) dV(x) \right] \qquad \text{(Eq. 2.17)}$$

The drain current of a HEMT in linear region is often expressed in a form similar to that used for a MOSFET, i.e., :

$$I_D = \mu \cdot \frac{W}{L} \cdot C_{2DEG} \left(V_g - V_{th} - \frac{V_{DS}}{2} \right) V_{DS} \qquad \text{(Eq. 2.18)}$$

Increasing V_{DS} up to certain value called V_{DSsat} , the drain current I_D start to saturate. In this region the I_D is constant and so the derivate of I_D will be zero.

$$\frac{dI_D}{dV_{DS}} = \mu \cdot q \frac{W}{L} C_{2DEG}\left(V_g - V_{th} - V_{DS}\right) = 0 \qquad \text{(Eq. 2.19)}$$

and V_{DSsat} is given by

$$V_{DSsat} = V_g - V_{th} \qquad \text{(Eq. 2.20)}$$

At bias condition of V_{DSsat} the I_D will be express as

$$I_{DSS} = \frac{1}{2} \mu \cdot \frac{W}{L} \cdot C_{2DEG}\left(V_g - V_{th}\right)^2 \qquad \text{(Eq. 2.21)}$$

that represent the drain current in saturation region.

Eq. 2.21 is an approximation valid for long channel devices. However, for HEMTs with a short gate length (l_g < 10 μm), the electron transport occurs under high electric fields and the expression of the saturation current is different. If the electric fields exceeds a certain critical value, the speed of the electrons in the 2DEG begins to saturate. Taking into account the effects of the saturation velocity model [85] the saturation current is expressed as

$$I_{DSS} = q \cdot n_S \cdot v_{sat} \qquad \text{(Eq. 2.22)}$$

Considering the expression of the drain current, it is also possible to define the transconductance of the device as the change in drain current I_D resulting from a variation of gate voltage V_g for a fixed V_{DS} :

$$g_m = \left.\frac{\partial I_D}{\partial V_g}\right|_{V_{DS}=const} \qquad \text{(Eq. 2.23)}$$

Similarly the output conductance of the device is defined as the I_D response to a V_{DS} variation for a fixed gate bias V_g

$$g_d = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_g=const} \qquad \text{(Eq. 2.24)}$$

2.5 Determination of the 2DEG properties from the HEMT characteristics

According to the description given in the previous section, it is clear that the characteristics of HEMT devices depend strongly on the properties of the 2DEG, namely on the carrier concentration and mobility of the electrons in the channel.

This paragraph describes how it is possible to determine the relevant properties of the 2DEG, reporting some examples of experimental data acquired on test-devices fabricated during the work of this thesis.

A common way to study the 2DEG properties is the combined analysis of the current voltage (I-V) and capacitance voltage (C-V) measurements on HEMT test structures.

In particular, by C-V measurements performed on the gate-source diode it is possible obtain important information, such as the sheet carrier concentration n_S, the carrier density profile as a function of the depth, and the distance d of the 2DEG from the AlGaN surface. Furthermore, from the I-V characteristics of the devices it is possible to determine the channel conductance. Combining the information obtained by C-V and I-V measurements, the electron mobility in the channel μ_{2DEG} can be extracted.

A schematic of the variation of the depletion region with the applied gate bias is shown in *Fig. 2.12*. Considering a Schottky diode with a contact area A formed onto a heterostructure with a uniform 2DEG concentration, under

an applied reverse bias V_R the width of the depletion region under the contact is

$$w = \sqrt{\frac{2\varepsilon_0 \varepsilon_{AlGaN}(V_{bi} - V_R)}{qN}} \qquad \text{(Eq. 2.25)}$$

where V_{bi} is the intrinsic potential difference at gate voltage zero and V_R is the reverse bias applied to the Schottky gate contact.

For a HEMT with a Schottky gate contact biased at V_g=0 V, the capacitance normalized by the Schottky contact area A of the depletion region is express as

$$C_{V_g=0} = \left.\frac{dQ}{dV}\right|_{V_g=0} = \frac{\varepsilon_0 \varepsilon_{AlGaN}}{w} \qquad \text{(Eq. 2.26)}$$

where w in this case extends up to the 2DEG and corresponds to the distance d of the 2DEG from the AlGaN surface (see *Fig. 2.12a*).

By applying a negative bias to the gate contact (*Fig. 2.12b*), the depletion region under the contact starts to expand, depleting the 2DEG and extending inside the intrinsic GaN buffer layer.

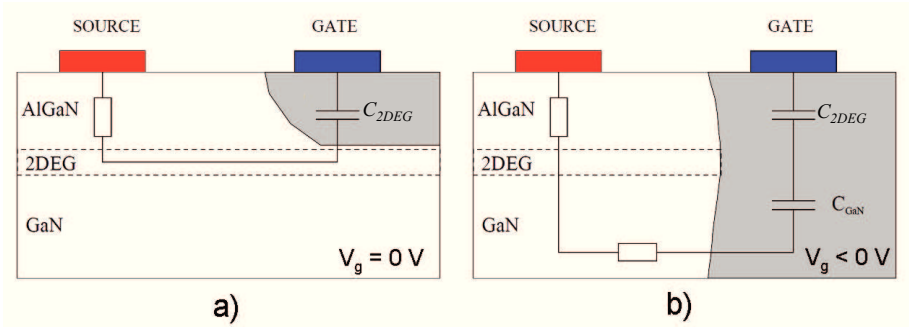

Fig. 2.12: *Schematic of the depletion region at V_g=0 V (a) and in case of V_g<0 V (b). Figure is taken from [86].*

When the channel is completely depleted, the capacitance of the depletion region will be given by the contributions of two capacitances in series, the capacitance due to the 2DEG and the capacitance due to the intrinsic layer of GaN. Because of its intrinsic state and its significantly larger thickness, the GaN layer contributes to the total capacitance with a smaller capacitance $C_{GaN} < C_{2DEG}$, that in case of two capacitance in series become dominant.

$$\frac{1}{C_{tot}} = \frac{1}{C_{2DEG}} + \frac{1}{C_{GaN}} \qquad \text{(Eq. 2.27)}$$

The *Fig. 2.13* shows an example of a C-V measurement acquired on a HEMT structure in the gate bias range from -10 V to 0 V.

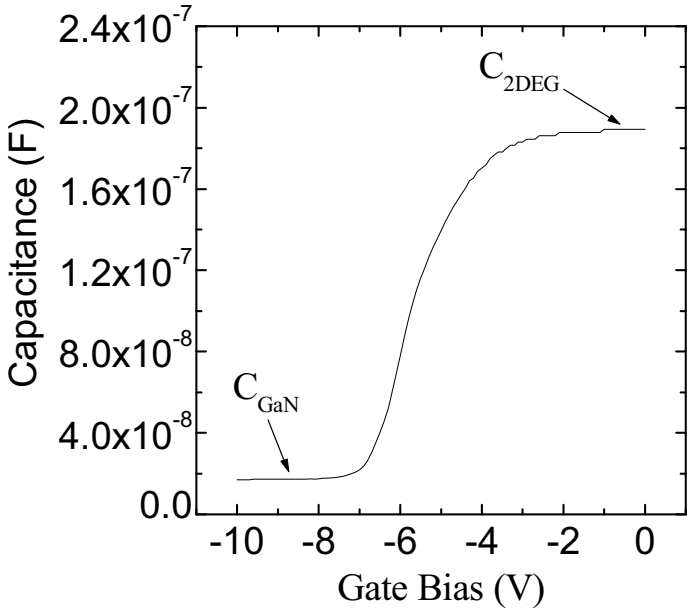

Fig. 2.13: *Capacitance of a HEMT as function of gate voltage*

By combining Eq. 2.25 and Eq. 2.26 it is possible obtain the capacitance for a depletion region w

$$C = \frac{1}{\sqrt{\frac{2(V_{bi} - V_R)}{qN \cdot \varepsilon_0 \varepsilon_{AlGaN}}}} \qquad \text{(Eq. 2.28)}$$

from which

$$\frac{1}{C^2} = \frac{2(V_{bi} - V_R)}{qN \cdot \varepsilon_0 \varepsilon_{AlGaN}} \qquad \text{(Eq. 2.29)}$$

From a C-V measurement it is possible to have information on the carrier concentration N [74]

$$N = -\frac{2}{q \cdot \varepsilon_0 \varepsilon_{AlGaN} \frac{d\left(\frac{1}{C^2}\right)}{dV}} \qquad \text{(Eq. 2.30)}$$

In particular, the C-V curves allow the determine the carrier concentration N_C as a function of depth d_{2DEG}

$$N\left(d_{2DEG}\right) = \frac{C^3}{q\varepsilon_0 \varepsilon_{AlGaN}} \frac{1}{\left(\frac{dC}{dV}\right)} \qquad \text{(Eq. 2.31)}$$

(see *Fig. 2.14*), and the depth d_{2DEG} can be expressed as

$$d_{2DEG} = \frac{\varepsilon_0 \varepsilon_{AlGaN}}{C} \qquad \text{(Eq. 2.32)}$$

In this way it is possible obtain the carrier concentration profile as a function of the depth and determine the position of the 2DEG. As shown in

Fig. 2.14, the peak of the carrier concentration can be associated to the depth of the 2DEG.

From the analysis of the C-V curves it is also possible to have information on the sheet charge density of the 2DEG, by integrating the concentration profile of free carriers:

$$n_S = \int_{-\infty}^{+\infty} N(d_{2DEG}) d(d_{2DEG}) \qquad \text{(Eq. 2.33)}$$

The sheet carrier concentration n_S is reported in *Fig. 2.15* as a function of the gate bias V_g.. Such a representation is typically used to determine the threshold voltage V_{th} of the device (see *Fig. 2.15*). In fact, from the fit of the linear region of this curve, is possible extrapolate the value of V_g at which the sheet charge density becomes zero, i.e. the threshold voltage.

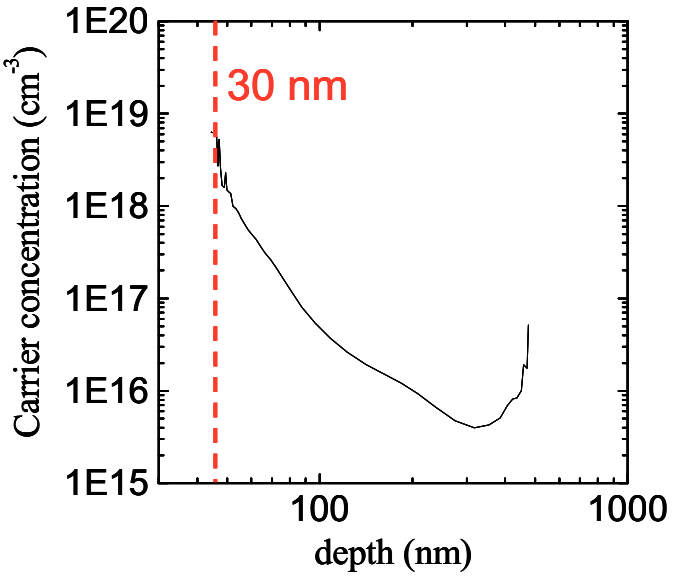

Fig. 2.14: *The carrier concentration as function of the AlGaN/GaN heterostructure depth.*

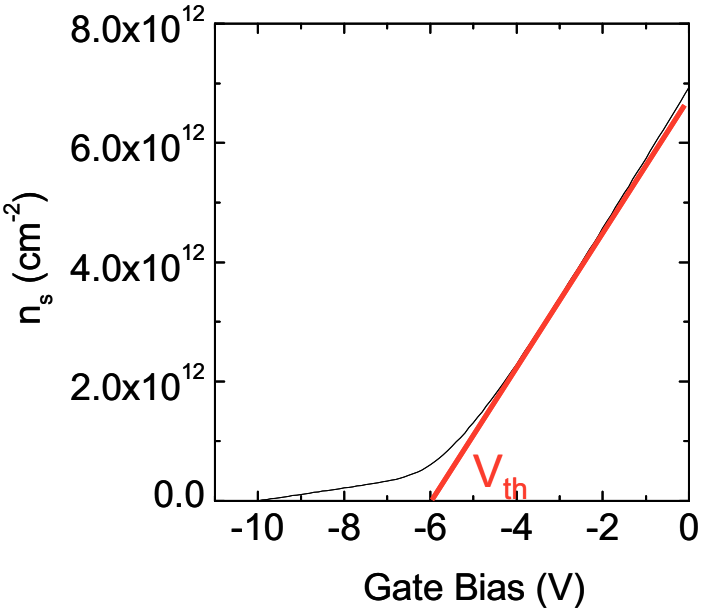

Fig. 2.15: *The sheet carrier concentration extrapolated by the C-V curves*

In order to determine the 2DEG mobility, the I-V characteristics of the devices must be considered. The mobility of the electrons moving in the 2DEG channel is related to the *channel conductivity* σ

$$\mu = \frac{\sigma}{q \cdot n_S} \qquad \text{(Eq. 2.34)}$$

The conductivity in the 2DEG is proportional to the product $n_S \cdot \mu$, and is an important parameter to estimate the quality of the channel in a HEMT, that can be determined from the I-V characteristic of the device.

Considering the drain current I_D in the linear region (Eq. 2.18) and the output conductance g_d (Eq. 2.24) for a constant value of V_g, we have that [87]

$$g_d(V_g) = \mu(V_g) \cdot q \frac{W}{L} C_{2DEG}(V_g) \cdot \left[V_g - V_{th} - V_{DS}\right] = \mu(V_g) \cdot q \frac{W}{L} n_S(V_g) \qquad \text{(Eq. 2.35)}$$

Clearly, from a measurement of the device output conductance g_d it is possible to determine the product $n_S \cdot \mu$ as a function of the gate bias V_g (Eq. 2.34). Then, combining this information with that extracted from the C-V measurements (the ns versus Vg) it is possible to determine the mobility of the 2DEG as a function of the sheet carrier density.

Another important parameter typically used to characterize AlGaN/GaN heterostructures is the *sheet resistance* R_{sh}, defined as:

$$R_{sh} = \frac{1}{q \cdot n_S \cdot \mu} \qquad \text{(Eq. 2.36)}$$

Clearly, an AlGaN/GaN heterostructure with a highly conductive channel is characterized by a low sheet resistance, that is important to reach a high power density in the device. For a sheet carrier density of about 10^{13} cm^{-2} and a mobility in the order of 1000 cm^2/Vs, the values of the sheet resistance are in the order of 600Ω/sq. The minimization of the sheet resistance R_{sh} depends clearly on the optimization of the heterostructure parameters (thickness, Al concentration, etc.). The sheet resistance of the 2DEG in AlGaN/GaN heterostructures is typically determined by four point probe I-V measurements (e.g., using Van der Paw structures) but can be also determined using Transmission Line Model (TLM) patterns or even contactless methods [168]

2.6 Open issues in current GaN HEMT technology

GaN HEMTs can have applications in several fields, from power conditioning to microwave amplifiers and transmitters, but also for satellite

communication, front-end electronics, commercial ground base stations or high performance radar applications.

In the recent years, high output power (900 W at 2.9 GHz and 81 W at 9.5 GHz), high cut-off frequency (f_T = 181 GHz at L_g=30 nm) and high-power efficiency (PAE = 75% at P_{sat} = 100 W) have been reported for GaN HEMTs [88]. In spite of these enormous progress, there are still several physical issues that limit the performances of GaN-based HEMTs**.**

One of the big issues concerning the device operation is the presence of trapping centres close to the surface or in the bulk of the material. Their presence is the origin of several commonly observed phenomena like current collapse [89,90], threshold voltage shift [91], reduction of short channel effect [92], limited microwave power output [93] and light sensitivity [94].

In particular the current collapse strongly reduces HEMT performance especially under high frequency operation, reducing also the device output power. Basically, it consist in the persistent reduction of the dc drain current caused by the application of a high drain-source bias [90]. In this cases, it is possible observe a reduction of the current level, with an increase in knee voltage, i.e. an increase in the V_{DS} value at which the I_{DS} enter in the saturation region. The presence of defects, traps and deep level affect the charge transfer process, reducing the number of electrons available for current conductions [95]. Depending if the current collapse is related to traps present in the bulk material or related to the surface states, it is possible to distinguish two different situations, called respectively drain lag or gate lag events. The drain lag is related to the transient in the drain current when the V_{DS} is changed between two different values [96]. On the other hand, the gate lag is referred to the slow transient response of the drain current when the gate voltage is changed abruptly [97].

Thanks to photoionization measurements, it was possible to correlate the occurrence of current collapse with the presence of traps located into the AlGaN/GaN layer stack [98]. The trapping of hot 2DEG electrons, inside the layer stack, accelerated by the high drain-source bias, has been related to traps center located in the semi-insulating substrate or in the high resistivity GaN buffer or in the AlGaN buffer layer [18]. Moreover several works showed that also the high-density distribution of surface states can cause the I_{DS} collapse [99,100].

Current collapse measurements have been seen more pronounced in the case of devices with a semi-insulating buffer layer, with respect to conductive ones. A dependence of the drain current recovery with the temperature and light wavelength was observed. By increasing the temperature it was possible to improve the drain current, due to the thermal emission of trapped electrons from deep traps [101]. By the decreasing the light wavelength it was also possible to improve the recovery of the drain current [102].

On the other hand, also the surface states play a fundamental role in the current collapse issue [103]. For this reason a passivation of the surface (i.e. with the use of a dielectric layer, like SiN_x, Si_3N_4, SiO_2, Al_2O_3, SiON, etc.) can be an efficient way to partially overcome this problem [104,105,106,107].

Because of the high electric field at the drain edge of the gate and due to the presence of surface states related to material defects (like dislocations), a low gate leakage can reside between the drain and the gate, also when the device is off [108,109]. The neutralization of these charges present at the surface leads to a depletion of the 2DEG under this surface states. When a fast signal is applied to the gate, the depleted region between drain and gate, cannot immediately turn-on because of the slow response of the deep levels traps or the low electrons mobility along the surface. In this case, under this region the 2DEG is affected by a high resistivity, due to the low carrier concentration. If the gate signal is long enough, the electrons are released from the traps increasing the carrier concentration and the drain current as well. This behaviour can be explained by the so called *virtual gate* model [110]. In this model, the I-V characteristics depend on the potential of the virtual gate, that in turn depends on the spatial distribution of trapped charge along the gate-drain access region. The presence of these traps acts as an additional gate in series that limits the maximum current of the device. A significant fraction of V_{DS} drops across this virtual gate, preventing the increasing of the electric field at source and limiting the increasing of the I_{DS}. In *Fig. 2.16* is shown the schematic of the I_{DS} response for a gate pulse V_G according the virtual gate model.

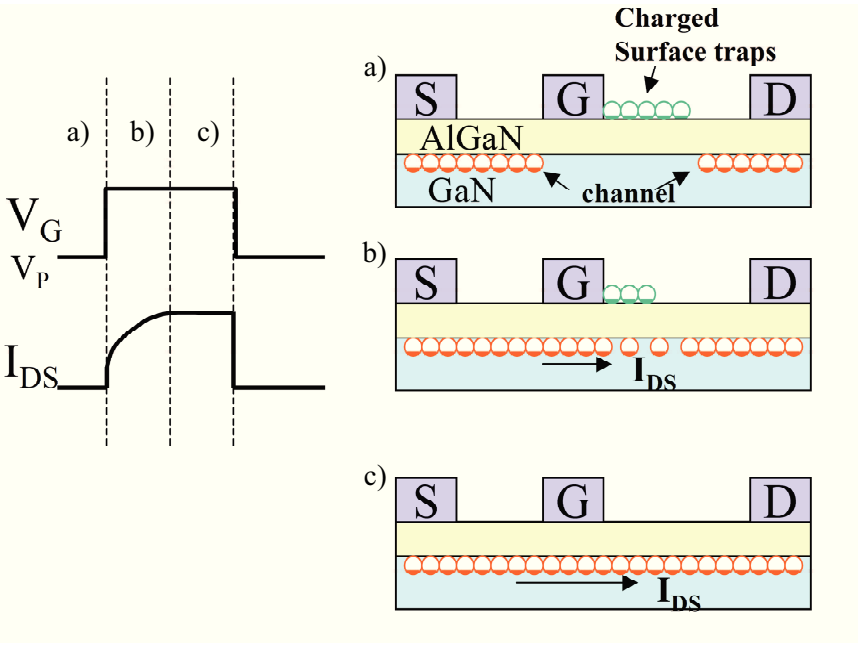

Fig. 2.16: *Schematic of the virtual gate model explaining the current collapse due to the surface traps charge. Figure taken from [111].*

Another problem that strongly affects the device performance in AlGaN/GaN HEMTs is related to the high gate leakage currents. For high voltage applications, when the gate electrode is strongly reverse biased with respect to the drain, the gate leakage can seriously increase. Although different techniques were proposed to prevent this problem [112,113], most of the works suggest the use of dielectric under gate Schottky contact in order to reduce the leakage current [114,115].

Different oxides (SiO_2, Al_2O_3, Ga_2O_3, HfO_2, Sc_2O_3, La_2O_3 etc.) have been studied as possible gate dielectrics in GaN transistor technology [115,116,117,118,119]. In this respects, the use of high permittivity dielectric materials can be advantageous to limit the reduction of the gate-to-source capacitance occurring in insulated gate HEMTs, which in turn impact the device transconductance.

In this thesis, the case of Nickel Oxide as gate dielectric for GaN HEMTs will be preliminarily discussed in chapter 6.

In the recent years the research activity on GaN was also focused on the demonstration of reliable devices working in enhancement mode *(normally-on),* i.e. operating at positive gate bias. This latter is an important request for high power switches. In fact, enhancement mode AlGaN/GaN HEMTs would offer a simplified circuitry (eliminating the negative power supply), in combination with favourable operating conditions for device safety. A schematic band diagram of an AlGaN/GaN heterostructure under normally-on and normally-off condition is reported in *Fig. 2.17*.

Clearly, in order to obtain a normally-off device the accurate control of the threshold voltage V_{th} is essential. In Eq. 2.14 an expression of the threshold voltage V_{th} has been given, depending on the Schottky metal/semiconductor barrier height (Φ_B), on the thickness of the AlGaN barrier layer (d_{AlGaN}), on the distribution of the residual doping concentration in the AlGaN layer (N_D), on the polarization charge at the AlGaN/GaN interface (σ).

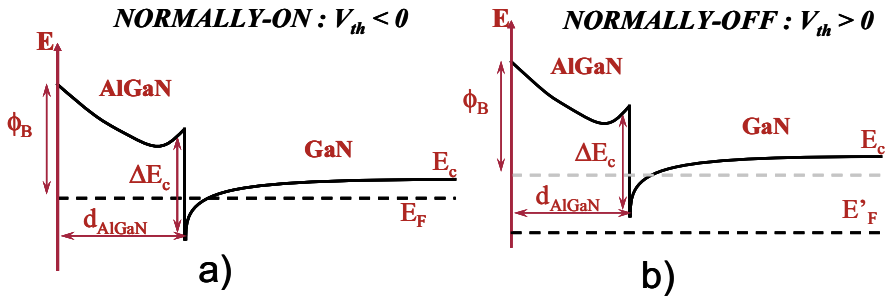

Fig. 2.17: *Schematic band diagram for AlGaN/GaN heterostructure in normally-on (a) and in normally-off configuration (b).*

Basing on the Eq. 2.14, it is clear that there are some possibilities to shift the threshold voltage towards more positive values in order to achieve a normally-off behaviour ($V_{th} > 0$).

Firstly, it must be pointed out that the increase of the metal semiconductor Schottky barrier height can increases the threshold voltage. However, the typical values of metal/AlGaN Schottky barrier height Φ_B

range between 0.7 and 1eV [120]. Hence, tailoring the barrier height of the metal gate is not an efficient solution.

Several approaches have been recently reported in literature to achieve reliable normally-off AlGaN/GaN HEMTs: the recessed gate process [121], the fluorine-based plasma etch under the gate [49], the surface oxidation process [122], the use of thin layer of AlGaN barrier layer [123], or the use of different thin barrier layer under the gate contact [51,53] are all investigated approach that led the possibility to reach an enhancement mode operation HEMT.

As can be also deduced from Eq. 2.14, a reduction of the barrier thickness d_{AlGAN} leads to a positive shift of V_{th}. As a matter of fact, this concept is the basis for the conventional approach of the recessed gate for normally-off HEMTs[124]. Typically, recessed gate structures are formed by selective plasma etchings.

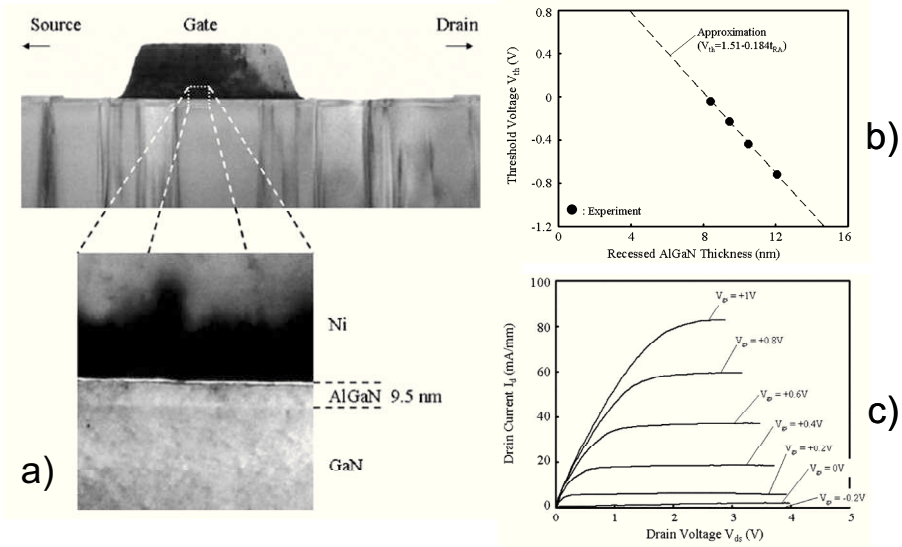

Fig. 2.18: *Cross section TEM for recessed-gate structure (a), the variation of V_{th}, by the recessed AlGaN thickness (b) and I-V characteristics for normally-off device fabricated with recessed approach (c). Data are taken from Ref. [50].*

Saito et al. [50] showed as the increasing of the V_{th} is proportional to the reduction of the AlGaN barrier layer (see *Fig. 2.18*). However, etching just a

few nanometers can represent a problem in terms of reproducibility and uniformity of the process at a wafer level.

The introduction of negative charges in the near-surface region of the AlGaN barrier can be a possible method to control the carrier sheet concentration of the 2DEG and, hence, the value of V_{th}. Based on this idea, *Cai et al.* [49] demonstrated the possibility to shift the threshold voltage of AlGaN/GaN HEMTs to positive values by introducing fluorine ions by means of a Reactive Ion Etching (RIE) plasma process in CF_4 (see *Fig. 2.19a*). The amount of negative charge included at the AlGaN layer is controlled by the duration of the etched process. In this way these authors were able to have a variation of the threshold voltage depending on the plasma RF power (*Fig. 2.19b*) or on treatment time (*Fig. 2.19c*).

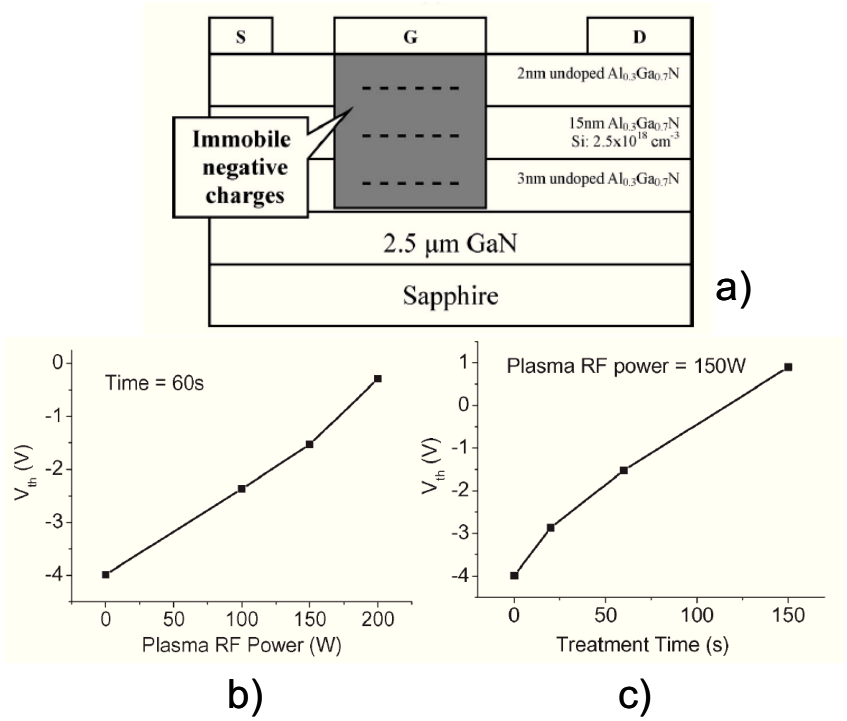

Fig. 2.19: *Schematic cross section of HEMT with fluorine plasma treatment (a) and variation of V_{th}, by the plasma RF power (b) and the treatment time (c). Data are taken from Ref. [49].*

However, also this process has some potential drawbacks, like the introduction of defects in the AlGaN barrier layer, which can lead to a degradation of the 2DEG mobility. Hence, an annealing process after the gate fabrication is needed to repair the damage and recover the mobility. The use of other plasma techniques, like inductive coupled plasma (ICP), could be also considered to reduce the damage and better control the parameters defining the normally-off operation (threshold voltage and sheet carrier concentration of the 2DEG).

Recently, Roccaforte *et al.* [125,126] studied the effect of a selective oxidation of AlGaN/GaN heterostructures, with the aim to locally insulate the 2DEG conductive channel. They demonstrated that the isolation in AlGaN/GaN heterostructures grown on sapphire can be achieved even though the thickness of a surface oxide formed at 900°C for 12 hours does not reach the depth of the 2DEG. The results were discussed considering the possible effects of high-temperature oxidation on the material properties [126]. Lately, similar approaches based on the local oxidation of the surface region have been also used to achieve normally-off operation in nitrides HEMT devices. As an example, *Chang et al.* [127] reported, in the case of AlN/GaN heterostructures, that a near surface oxidation process can be useful to convert into aluminium oxide a surface-layer of AlN and, then, to reduce the thickness of the barrier layer below the critical thickness. In this way, a normally-off device was achieved, whose I-V characteristic are shown in *Fig. 2.20*.

Also in this case the threshold voltage V_{th} depends on the time of the oxidation process *Fig. 2.20b*. A similar result has been reported also by Medjdoub et al [128], showing also a great reduction of the drain leakage current (about three order of magnitude). Harada et al. [129] used a selective electrochemical oxidation of AlGaN/GaN heterostructures to create recessed oxide gate, with a consequential normally-off behaviour.

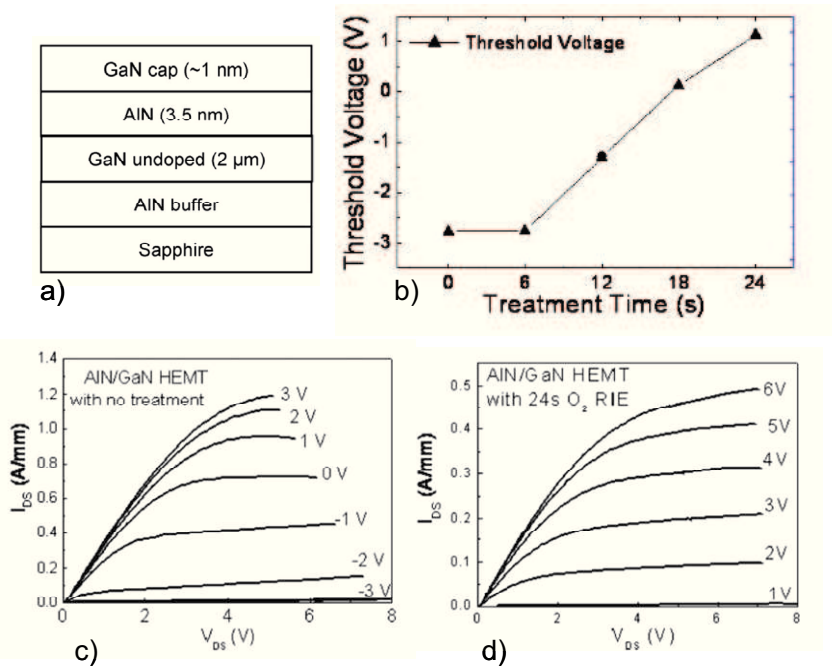

Fig. 2.20: *Cross section of the treated sample (a), variation of V_{th}, by the treatment time (b), I-V characteristic of the untreated (c) and the oxidized sample (d). Data are taken from Ref. [127].*

An innovative and promising solution to achieve enhancement mode operation for AlGaN/GaN HEMTs consists in the use of a p-type semiconductor capping layer, i.e. p-AlGaN or p-GaN, under the gate electrode [130,131]. In this way the p-type semiconductor lifts up the potential at the channel depleting the 2DEG and leading the normally-off condition (see *Fig. 2.21*).

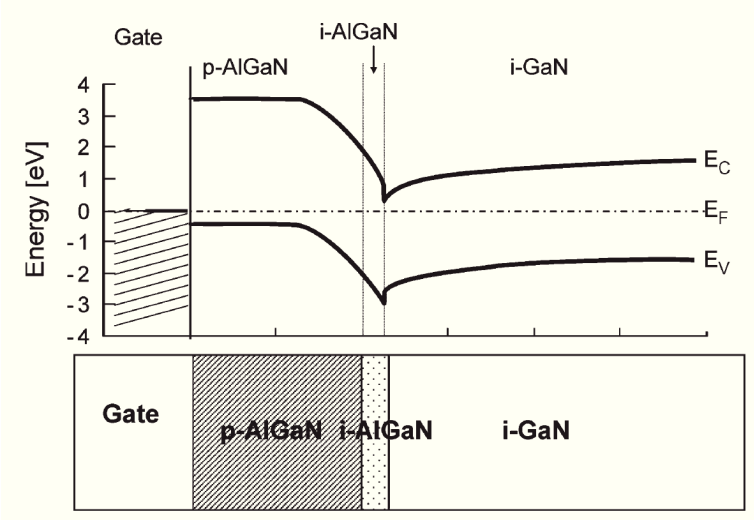

Fig. 2.21: *Band diagram for a p-AlGaN/AlGaN/GaN heterostructure for HEMT in enhancement mode operation. Data are taken from Ref.[52]*

Fig. 2.22 shows the I-V characteristics of a normally-off HEMT fabricated with the with the use of a p-AlGaN cap layer. When the gate is biased at 0 V or less, the 2DEG under p-type gate is fully depleted and the drain current can not flow in the channel. When a positive bias is applied to the gate, the channel starts to be refilled by electron until the channel will be fully restored (with positive V_{th}). Applying an increasingly positive voltage, at a certain value of V_g, an injection of hole from the p-type material to the 2DEG. The hole injection will result in an increase of the number of electrons in the channel to keep the charge neutrality at the channel. The electrons collected at the channel will increase the carrier concentration of the 2DEG, increasing the drain current with an high mobility, while the injected holes will stay around the gate because the lower hole mobility (at least two orders of magnitude) with respect the electron mobility. The presence of holes near the gate region will also increase the device performance keeping low the leakage current from the gate. A schematic of this behaviour is showed in *Fig. 2.23*.

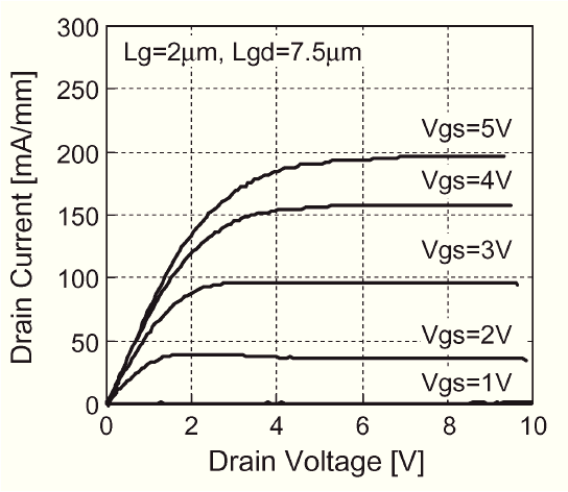

Fig. 2.22: *I-V characteristic of a normally-off operation with the use o p-AlGaN cap layer. Data are taken from Ref. [52].*

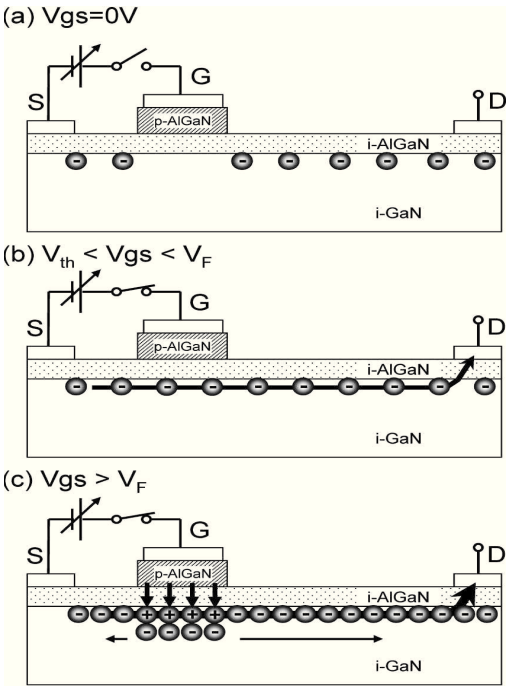

Fig. 2.23: *Working principle of HEMT with the p-AlGaN cap layer under the gate contact at Vg=0V (a), Vg<Vg<VF (b), Vg>VF (c),*

Due to the above described conduction mechanism in the channel, this device has been called *Gate Injection Transistor* (GIT) [52]. Basing on this approach, recently devices with a high V_{th} of +3 V and a low gate leakage current (0.1 mA/mm @ V_{DS}=+12 V) was presented by the Samsung Electronics Co. [132].

Great part of this work of thesis was focused to clarify some important physical issues related to the fabrication of normally-off HEMTs using a p-GaN gate electrode.

In particular, to fully exploit the intrinsic advantages offered by this approach, a good Ohmic contact for the gate electrode is required. The fabrication of Ohmic contact on p-GaN material was the subject of discussion of chapter 4 and one of the topics investigated in more detail. The fabrication and characterization of enhancement mode AlGaN/GaN HEMTs with the use of a p-GaN capping layer is described in chapter 5.

Chapter 3: Nanoscale characterization of AlGaN/GaN heterostructures after near-surface processing

In this chapter, the modification of the 2DEG properties after specific near-surface processing (fluorine-based plasma and local oxidation processes) were investigated, either by macroscopic and nanoscale characterization techniques. Although a positive shift of the threshold voltage can be obtained, it will be shown that these treatments can strongly compromise the conductivity of the 2DEG channel, due to the difficulty to control the plasma or oxidation processes in the gate region. Hence, the use of a p-GaN cap layer was defined as the most reliable strategy to achieve a normally-off condition.

3.1 Fluorine-based plasma treatment of the AlGaN surface

As mentioned in the previous chapter, one of the possible methods to achieve normally-off operation in AlGaN/GaN HEMT devices is the fluorine-based plasma treatment of AlGaN surface in the gate region [49]. The negative fluorine charges introduced by this kind of treatment have been shown to produce a positive shift of the HEMT threshold voltage. However, this approach can lead to a degradation of the 2DEG mobility due to a large

amount of defects introduced by plasma irradiation in the AlGaN barrier layer. Hence, to partially mitigate this drawback, accurate plasma etching techniques, like inductive coupled plasma (ICP) using very low power, can be used to have a better control of the electrical properties of the heterostructure.

In the first part of the work of thesis, the effect of a fluorine plasma treatment on the properties of the 2DEG at AlGaN/GaN heterointerface was studied using either nanoscale measurements or properly fabricated Schottky contacts on the fluorine treated surface.

The material used for this experiment was an AlGaN/GaN heterostructure grown on 150mm diameter Si wafers in the AIXTRON CCS MOCVD reactor at ST Microelectronics. The heterostructure consisted of a 40nm AlGaN barrier layer with an Al concentration of 25% grown on top of a unintentionally doped GaN buffer (1 μm thick). The plasma treatment was performed at room temperature with a CHF_3/Ar gas mixture using the Roth & Rau Microsys 400 ICP equipment of the clean room of CNR-IMM. The CHF_3/Ar gas flux was 20/40 sccm and the operating pressure in the chamber was 5×10^{-2} mbar. The control bias, the power and the process duration were 200 V, 250 W and 300 s, respectively.

Two Schottky diode structures were fabricated using the equipments of the clean room of CNR-IMM and used for this study: (i) a reference diode, with the Schottky contact fabricated directly on AlGaN/GaN not subjected to plasma treatment (see schematic in *Fig. 3.1a*), and (ii) a modified diode with the Schottky contact on plasma treated heterostructure (see schematic in *Fig. 3.1b*).

For both kind of structures, source and drain Ohmic contacts were initially formed by defining a Ti(15nm)/Al(200nm)/Ni(50nm)/Au(50nm) multilayer, by optical photolithography and metal wet etch. Ohmic characteristics were obtained after a rapid thermal annealing at 800 °C [133]. On the modified structure, the fluorine plasma treatment was carried out on selectively defined surface regions (where the Schottky contact will be deposited) using a photoresist hard mask patterned by photolithography. Both for the reference and modified diodes, the Schottky contact was subsequently obtained by sputtering a Pt/Au bilayer and lift-off. [133]. Finally, both samples were subjected to an annealing process at 400 °C, in

order to recover the damage induced by the plasma process. It is worth noting that this annealing process does not cause degradation of the reference Schottky contact.

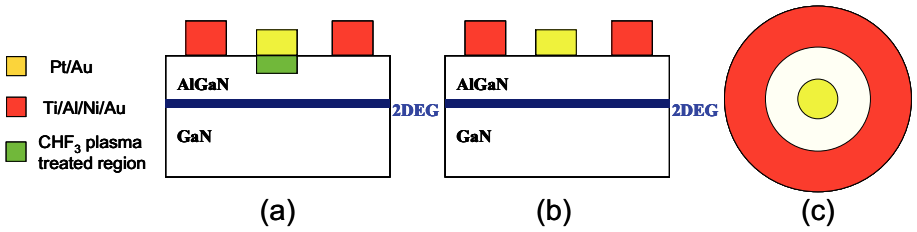

Fig. 3.1: *Schematic cross section of the Schottky diode fabricated on the modified heterostructure surface by the selective plasma process (a) and on the untreated surface (b). The top view of the fabricated Schottky diode is also reported (c).*

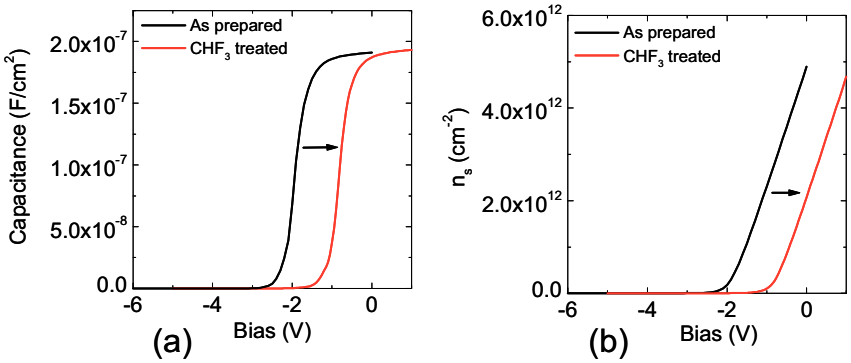

Fig. 3.2: *Capacitance (a)and extracted n_S (b) as a function of the bias for the reference and plasma treated device.*

On these fabricated devices, an electrical characterization by capacitance-voltage (C-V) measurements has been carried out. The C-V characteristics for the reference device and for the device treated with the CHF_3 plasma are reported in *Fig. 3.2a*. These C-V curves clearly show a shift towards less negative values, for the plasma treated sample. The sheet carrier concentration n_S extracted by the integration of the C-V curves (using the procedure described in Chapter 2), is shown in *Fig. 3.2b*. As can be seen,

a reduction of the n_S for the CHF_3 treated device is observed. For a bias of 0 Volts, a decrease of n_s from 5×10^{12} cm^{-2} in the reference sample to 2×10^{12} cm^{-2} after the plasma treatment was found. From the linear fit of these curves, it was possible to quantify the shift of the threshold voltage, towards less negative values, for the plasma treated device. The threshold voltage was V_{th}= -1.92 V for the reference device, and increased to V_{th}= -0.8 V for the device processed in CHF_3.

The near-surface modification induced by the plasma were monitored by cross section TEM micrographs, acquired below the Pt/Au Schottky contact in the device subjected to the plasma process (see *Fig. 3.3*). The dark contrast in the AlGaN region underneath the Pt gate contact can be associated to a considerable amount of crystalline imperfections (defects). This defect-rich interface region could be highly resistive and could affect the leakage current behaviour of the Schottky contact. Indeed also *Chu et al.* [134] suggested that the fluorine plasma can react with GaN (or AlGaN) to form non volatile F-containing compounds, leading to the creation of an insulating surface region.

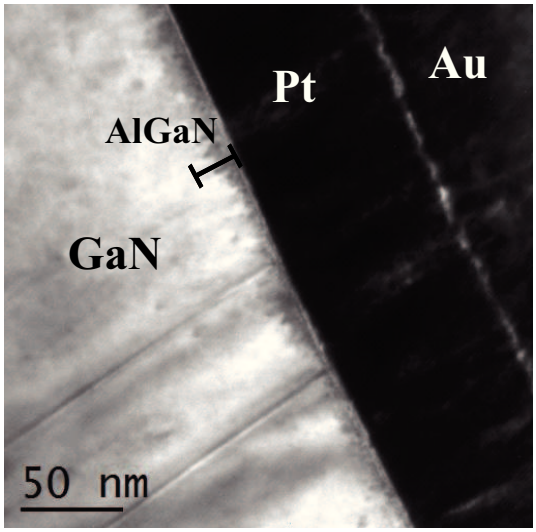

Fig. 3.3: *TEM image of the region below the gate of AlGaN/GaN HEMTs processed with a CHF_3 plasma treatment.*

In order to monitor the local electrical modification induced by the plasma treatment on the 2DEG, and corroborate the previous hypothesis, a nanoscale characterization approach was adopted. For this purpose Conductive Atomic Force Microscopy was used [171]. C-AFM scans were performed on appropriate samples, in which the plasma treatments were performed in selected regions, using a patterned photoresist as hard mask. In particular, photoresist stripes were defined on the sample surface by means of optical lithography, in order to selectively expose the sample surface to CHF_3 process. The transversal current between the nanometric conductive tip of the AFM and the sample backside was measured by a high sensitivity current sensor in series with the tip, as schematically illustrated in *Fig. 3.4*.

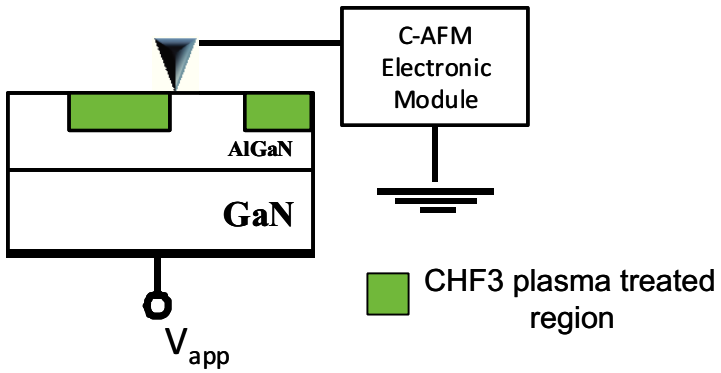

Fig. 3.4: *Schematic of the C-AFM measurement setup used to monitor the conductivity changes in a sample locally treated with CHF_3 plasma.*

A bias of +2 V has been applied between the probe and the backside of the sample. *Fig. 3.5a* reports the AFM morphological image of the sample. As can be seen, a slightly difference, can be observed between stripes processed with CH_3 plasma and stripes without any treatment. It consists in the presence of some features (similar to small cracks) appeared in the plasma treated regions. On the other hand, a significant difference can seen by the transversal current map acquired by C-AFM and shown in Fig. 3.5. This picture clearly shows the electrical changes of the material due to the plasma treatment. The local current is significantly reduced (2 orders of magnitude) on the stripes processed with fluorine-based plasma, with respect

to the ones without plasma treatment. This behaviour is consistent with an increased local resistance in the etched regions, which in turn can be associated whether to a partial depletion of the 2DEG channel or more simply to an increase of the local resistance of the AlGaN barrier layer due to plasma-induced damage.

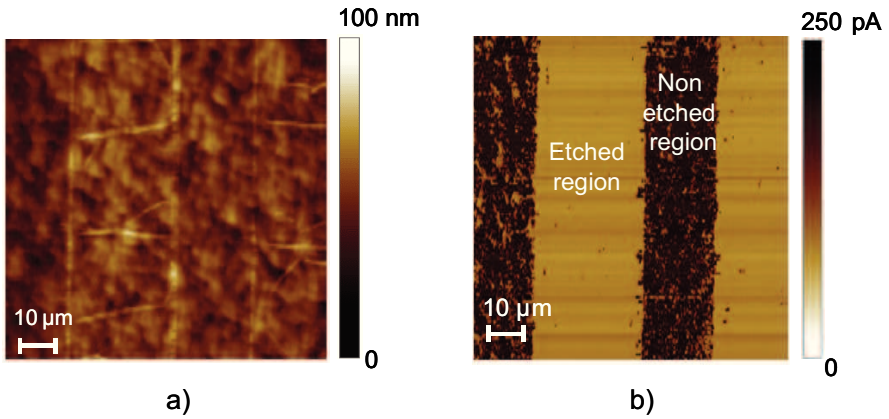

Fig. 3.5: *Morphology (a) and current map (b) of stripes locally treated with CHF_3 plasma*

The experimental results found from the macroscopic C-V characteristic of the devices and the nanoscale electro-structural analysis of the near-surface region (C-AFM) suggest that the observed electrical modifications are not only due to the introduction of negative fluorine ions, as already reported in the literature [49,134], but also due to the plasma-induced damage.

3.2 Rapid local thermal oxidation of AlGaN/GaN

As reported in chapter 2, local thermal oxidation received considerable attention in the last years due to the possibility to modify the properties of the heterostructure and lead to a normally-off behaviour [127,128,129]. Here, to better understand the effects of a rapid thermal oxidation on the electrical properties of AlGaN/GaN HEMT structures, a set of nanoscale structural an electrical analyses were carried out using a similar approach like that employed for the fluorine-based plasma treatments. In particular, appropriate test patterns consisting of locally oxidized AlGaN regions (stripes) alternating with non-oxidized regions were fabricated on the surface of an AlGaN/GaN sample grown on a Si substrate. For the fabrication, the sample was patterned with a 800 nm SiO_2 thick hard mask and then a local oxidation has been performed by rapid annealing process in the Jipelec JetFirst furnace at 900 °C in O_2 for 10 minutes.

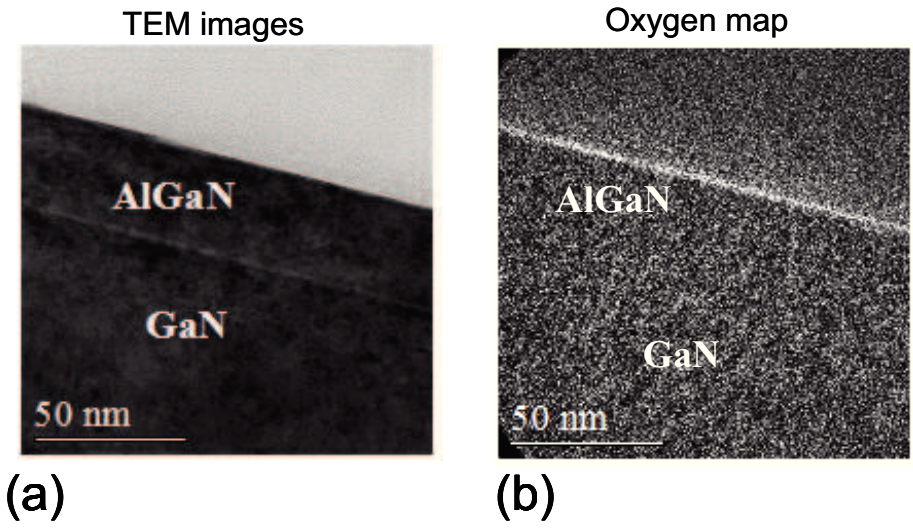

Fig. 3.6: *Bright field TEM analysis (a) and EFTEM for oxygen (b) on a the sample region oxidized by RTA at 900°C for 10 min.*

Under these conditions, a thin oxide layer is formed on selected areas of the sample surface, that is visible in the TEM images in *Fig. 3.6a*. Combining the bright field image (a) with the oxygen map acquired by EFTEM (Energy-Filtered Transmission Electron Microscopy) analysis (b) allowed to demonstrate the presence of a surface oxide layer of a thickness of about 2 nm grown after the process at 900°C. Even if in this case it was difficult to accurately determine the composition of the formed oxide, a long oxidation at same temperature showed the formation of mixed oxide of Al_2O_3 - Ga_2O_3 with a high chemical stability [126].

Fig. 3.7 shows the surface morphology and current map measured by C-AFM on the patterned sample surface. During the scan, a bias is applied to the sample backside and a map of the current flowing from the tip to the back-contact across the AlGaN/GaN heterostructure is measured. As can be seen, the surface morphology of the non-oxidized AlGaN region is almost undistinguishable from that of the oxidized areas (*Fig. 3.7a*). On the other hand, the two dimensional current map acquired with a sample bias of 3V (*Fig. 3.7b)* clearly shows an electrical contrast that resembles the geometry of the locally oxidized pattern created on the sample surface. In particular, it is worth noting that the current flowing through the oxidized AlGaN areas (brighter region) is almost two orders of magnitude lower than the current flowing through the non-oxidized AlGaN surface (darker regions). Hence, this result demonstrates the higher resistivity of AlGaN/GaN region subjected to a rapid thermal oxidation at 900°C for 10 min in O_2. By the comparison of the morphological and current maps (*Fig. 3.7a* and *Fig. 3.7b*) it is also possible to notice an enhanced conduction in the oxidized region in the proximity of surface steps present on the AlGaN surface. A similar effect has been already observed for thin thermal oxides grown on another wide band gap material (3C-SiC), and attributed either to oxide thickness variations or to a local electric field concentration at the step edges [135].

The reduced conductivity across the AlGaN/GaN region subjected to a rapid thermal oxidation can be ascribed both to the presence of the thin insulating surface oxide layer and to an increase of the sheet resistance of the 2DEG.

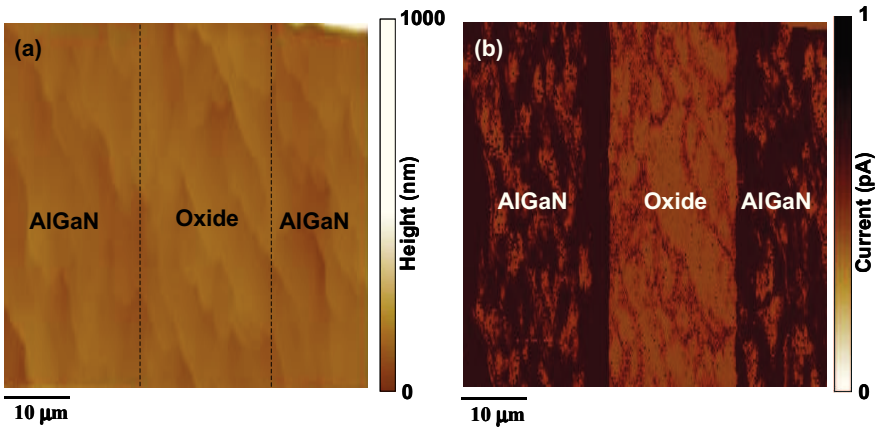

Fig. 3.7: *Surface morphology by AFM (a) and current map by C-AFM at 3V (b). The current flowing through the oxidized AlGaN surface is between one and two order of magnitude lower compared to the native bare AlGaN surface.*

The modifications produced on the 2DEG properties by the thermal oxidation was also monitored by macroscopic measurements. For this purpose, three kinds of diode structures (as shown in *Fig. 3.8a*, *Fig. 3.8b* and *Fig. 3.8c*) have been fabricated and electrically characterized: (i) a "reference" diode, with the Pt/Au Schottky contact deposited on the untreated AlGaN surface; (ii) a metal-insulator-semiconductor (MIS) diode with Pt/Au contact deposited on AlGaN covered by a thin (~ 5 nm) SiO_2 layer (called "MIS deposited" diode); (iii) a MIS diode with the Pt/Au contact deposited on thermally oxidized AlGaN covered the thin SiO_2 (called "MIS thermal" diode).

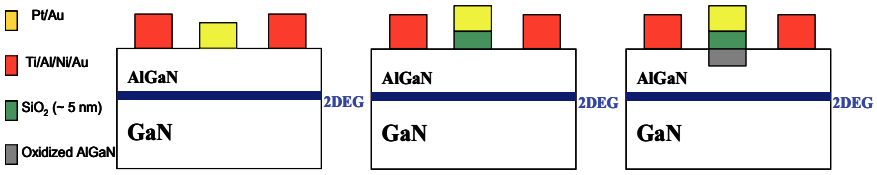

Fig. 3.8: *Schematic cross section for the "reference", the "MIS deposited" and the "MIS thermal" investigated devices.*

The fabrication procedure of the three device structures is here described. $Al_{0.27}Ga_{0.73}N$/GaN heterostructures grown on Si (111) substrates, with a nominal AlGaN thickness of 40 nm were used. First, the sample surface was cleaned in a diluted HF:HCl solution to remove the native oxide. The fabrication of the stripes test-structures was done with a similar procedure like that used for the fluorine-based plasma treatment. Using a 800 nm of SiO_2 as hard mask, local oxidation has been performed at 900 °C in O_2 for 10 minutes. After removing the hard mask, a thin (~ 5 nm) SiO_2 layer was deposited on the bare surface by plasma enhanced chemical vapor deposition (PECVD). Afterwards, this SiO_2 layer was selectively defined by wet etching to cover both the thermally oxidized and some not-oxidized AlGaN regions. Therefore, the Pt/Au bilayer Schottky contacts (defined by lift-off) [136] were fabricated on the three kinds of devices. The Ohmic contacts for these devices were formed by a Ti/Al/Ni/Au stack annealed at 800°C [133].. It is important to point out that the three types of devices were fabricated all on the same wafer.

Fig. 3.9 shows the forward and the reverse I-V characteristics of the three different fabricated devices. By fitting the forward [137], an increase of the ideality factor *n* from 2.13 to 3.16 has been obtained from the "reference" to the "MIS deposited" diode, while a similar value of the Schottky barrier was determined (~0.9 eV). On the other hand, a strongly non- ideal behaviour (n = 4.99) is observed for the "MIS thermal" diode, which is also accompanied by a reduction of the conduction current, as can be observed by the I-V curves in forward bias (Fig. 2a). From the reverse I-V characteristics (Fig. 2b), a strong reduction of the leakage current is observed in the "MIS thermal" diode, which incorporates both the thermal oxide and the deposited oxide below the Schottky contact, with respect to the "reference" and "MIS deposited" diodes. As an example, at the reverse bias of -5V the leakage current density of the "MIS thermal" diode was 10^{-5} A/cm^2 , i.e. three orders of magnitude lower than that of the "MIS deposited" and even five orders of magnitude lower than in the "reference" device.

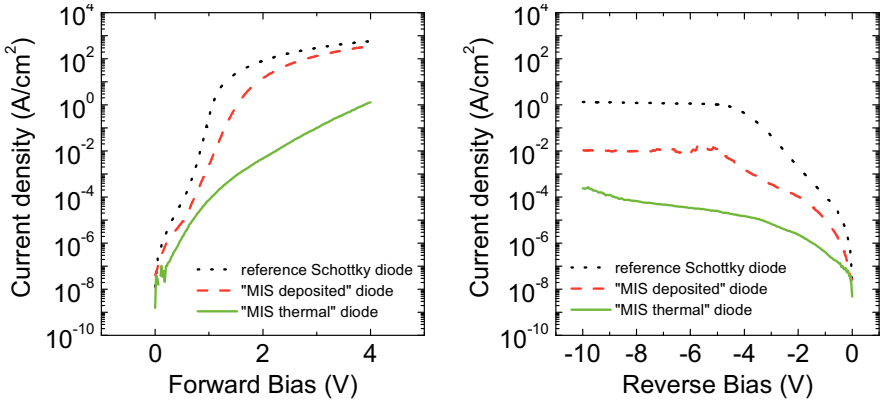

Fig. 3.9: *Forward (a) and reverse(b) I-V characteristics of the three devices: "reference" (dot line), "MIS deposited" (dash line) and "MIS thermal" (continues line) diode.*

Fig. 3.10 reports the C-V curves acquired on the three test devices. By comparing the C-V curves of the "reference" with that of the "MIS deposited" device, a decrease of the accumulation capacitance (from 3.34×10^{-7} F/cm^2 to 2.42×10^{-7} F/cm^2) is observed, clearly due to the presence of the insulating SiO_2 layer. Furthermore, in the "MIS deposited" diode the transition from accumulation to 2DEG depletion takes place at a more negative bias, as expected in a Schottky structure with an insulated gate, since part of the applied gate bias drops on the dielectric. On the other hand, this trend is not followed by the "MIS thermal" diode. In fact, in this case the transition from accumulation to depletion in the C-V curves occurs at more positive bias values, and the maximum saturation capacitance value (5.9×10^{-8} F/cm^2) is significantly reduced with respect to the other devices. The strong reduction of the capacitance in the thermally oxidized structure indicates a local depletion of the 2DEG.

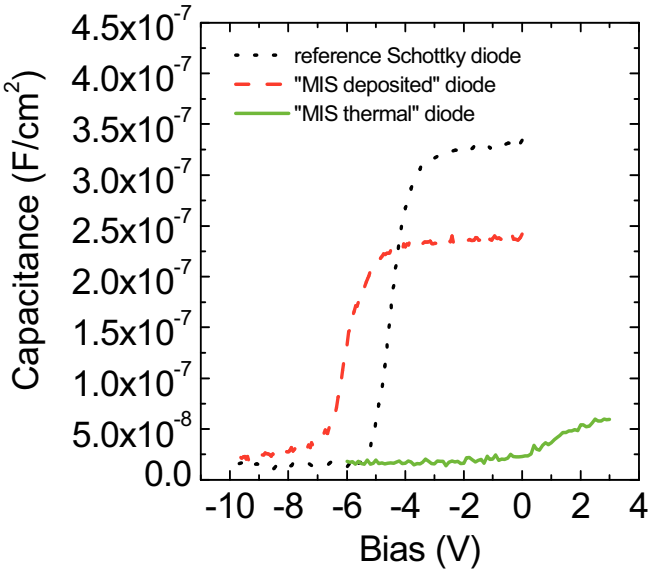

Fig. 3.10: *C-V curves characteristics of the three devices: "reference" (dot line), "MIS deposited" (dash line) and "MIS thermal" diode (continues line).*

The sheet carrier concentration n_S as a function of the gate bias was extracted by the integration of the C-V curves. From these curves, not reported here, the values of the threshold voltage V_{th} could be estimated: while the "reference" diode has a value of V_{th} of -4.69 V, the values of V_{th} in the "MIS deposited" and in the "MIS thermal" diodes were -6.39 V and -1.26 V, respectively. The positive shift of V_{th} of +4.95 V obtained in the "MIS thermal" diode with respect to the "MIS deposited" is fully consistent with the experimentally observed reduction of the n_S from 9.35×10^{12} cm^{-2} to 6.87×10^{11} cm^{-2} upon rapid oxidation.

Basing on these results, the possibility to tailor the 2DEG properties by local rapid oxidation and to obtain a positive shift of the threshold voltage can be considered as a promising step for a normally-off GaN transistors technology. However, this first experiment showed that even if a relatively rapid process was used (10 min), the sheet carrier density below the oxidized regions can be severely compromised. Additionally, the fabrication of AlGaN/GaN HEMTs using this local oxidation approach has been tried

during this thesis but the electrical characteristics were always strongly affected by the presence of a high leakage current. Hence, more work must be done to optimize the annealing condition and to understand the extent to which the process can be really useful for enhancement mode transistor.

Chapter 4: Au/Ni Ohmic contacts to p-GaN

The formation of Ohmic contacts to p-GaN is a key issue for the fabrication of normally-off devices using a p-GaN gate contact. In this chapter, the structural and electrical evolution of a Ni/Au bilayer deposited on p-GaN has been monitored after the annealing treatments in two different atmosphere (Ar and N_2/O_2) between 400 and 700 °C. The electrical measurements showed a reduction of the specific contact resistance in oxidizing atmosphere. Structural characterizations of the metal layer carried combined with nanoscale electrical measurements by C-AFM, allowed to give a possible scenario on the Ohmic contact formation mechanisms. The temperature dependence of the specific contact resistance was also studied in the two cases, and enabled the extraction of the metal/p-GaN barrier.

4.1 State of the art

The formation of good Ohmic contacts with a low specific contact resistance ρ_c is one of the crucial issues for GaN technology. The intrinsic difficulty to form good Ohmic contacts to p-type GaN is related both to the difficulty to find metals with low Schottky barriers to p-type wide band gap materials, and to the high ionization energies of p-type dopant impurities (typically in the range of 150-200 meV for Mg, that is the most common p-type dopant in GaN) [138,139]. While for the traditional optoelectronics applications the formation of good Ohmic contacts is not the most serious concern, the minimization of the specific resistance becomes a crucial issue in power and RF devices, where the improvement of the efficiency of

devices and modules is strictly related to the reduction of the power consumption (and, hence, of the parasitic resistance contributions).

For n-type GaN different solutions to achieve a low specific contact resistance were reported [140] and the current transport mechanisms have been widely discussed [141]. Typically, Ti-based multilayers, such as Ti/Al/Ti/Au [142], Ti/Al/Pd/Au [143]; Ti/Al/Mo/Au [144] and Ti/Al/Ni/Au [145,146] are commonly used to form Ohmic contact to n-type GaN. Multilayers system are largely preferred to Ti or Ti/Al bilayers in order to avoid oxidation during annealing [147]. The transition from Schottky to Ohmic behaviour is normally attributed to the formation of an interfacial TiN layer, through the reaction of Ti with GaN. The formation of TiN layer is associated to the outdiffusion of nitrogen atoms from GaN, that ultimately results into an increase of the carrier concentration in the GaN below the interface [148]. In particular, the nitrogen vacancies left in GaN as a consequence of TiN formation act as donors [149], increasing the carrier concentration of the material below the metal contact and favouring the electron tunnelling. As result a Ohmic contact with reduced specific contact resistance is formed.

On the other hand, for p-type GaN, the optimal solution to achieve Ohmic contacts and the mechanisms of carrier transport remain still under investigation.

Besides the possible application in optoelectronics devices (LEDs), as anticipated at the end of paragraph 2.6, the interest towards metal/p-GaN contacts has recently increased, due to the importance that they can have in the fabrication of normally-off device HEMTs using a p-GaN cap layer grown on the conventional AlGaN/GaN heterostructure. The introduction of a p-GaN cap under the gate requires at the same time the formation of a contact with a Ohmic behavior on the p-GaN, in order to optimize the performance of the normally-off HEMT, increasing the positive threshold voltage V_{th} and the current capability in the on-state [150,130].

In the recent years, several metallization schemes have been proposed in order to form good Ohmic contacts onto p-GaN materials, like Pd/Au [151], Ni/Pt/Au [152], Cr/Ni/Au [153] or Ni/Au [154,155,156]. Among them, the most commonly adopted solution has been the use of annealed Ni/Au bilayers. *Table 4.1* reports some literature data of specific contact resistance of Au/Ni-based contacts to p-type GaN. All these data refer to epitaxial p-

GaN material. In fact, p-type doping of GaN by ion-implantation is not widely used, due the high annealing temperatures (>1100°C) required for the activation of Mg [157,158].

p-type epitaxial GaN				
Metal	**N_A(atm/cm^3)**	**Annealing**	**ρ_c(Ω·cm^2)**	**Ref**
Au (100nm)	*Mg doped concentration 1×10^{20} cm^{-3}*	*As deposited*	2.6×10^{-2}	[159]
Ni (100nm)		*As deposited*	1.5×10^{-2}	
Ni (20nm)	2×10^{17}	450°C for 10 min in air	1.9×10^{-1}	[154]
Ni(20nm)/Au(5nm)		400°C for 10 min in air	2.5×10^{-2}	
Ni(5nm)/Au(5nm)		500°C for 10 min in air	4×10^{-6}	
Ni(20nm)/Au(50nm)	2.9×10^{17}	600°C for 30 s in N_2	6.1×10^{-4}	[155]
Ni(20nm)/Au(20nm)	1.2×10^{17}	500°C for 5 min in air	2×10^{-4}	[160]
Ni(50nm)/Au(50nm)	2×10^{17}	500°C for 10 min in N_2	3.4×10^{-3}	[156]
		500°C for 10 min in O_2	1.2×10^{-4}	
Ni(20nm)/Au(20nm)	1×10^{17}	500°C for 1 min in air	7.6×10^{-3}	[161]
Ni(50nm)/Au(20nm)	6×10^{16}	500°C for 10 min in N_2/O_2	3.7×10^{-2}	[162]
	1×10^{18}		4.4×10^{-3}	
Ni(25nm)/Au(20nm)	2×10^{17}	500°C for 10 min in N_2/O_2	1×10^{-5}	[163]

Table 4.1: *Specific contact resistance ρ_c of Au-Ni -based Ohmic contacts on epitaxial p-type GaN.*

As can be seen, many authors propose the use of Au/Ni bi-layers annealed in an oxidizing ambient (air, O_2, N_2/O_2) for Ohmic contacts to p-

GaN, reporting values of ρ_c in an extremely wide range (10^{-1}-10^{-5} $\Omega \cdot cm^2$), depending on the material and experimental conditions [162,163,164].

The structural evolution of the contacts after annealing in oxidizing ambient has been also discussed under different points of view, in order to explain the occurrence of an Ohmic behaviour.

Ho *et al.* [154] argued that the oxidation of thin Ni films leads to the formation of an interfacial nickel oxide layer (NiO), acting as a p-type semiconductor with a low Schottky barrier height (0.185 eV). To explain the formation of an Ohmic contact, they assumed that such a low barrier can be overcome by a pure tunnelling mechanism [154]. Nevertheless, more recent calculations contradicted this work, demonstrating that a significantly higher barrier (2.28 eV) must be expected for the NiO/p-GaN system [165].

Lately, Jang *et al.* [156] proposed that an oxidizing annealing atmosphere promotes the out-diffusion of Ga atoms from the substrate, leaving acceptor-like Ga-vacancies that locally increase the carrier concentration below the contact. In this way, the increased hole concentration below the interface leads to a thinner metal/p-GaN barrier, that favours the tunnel of the carriers and, hence, a significant reduction of the contact resistance. However, a similar interpretation was given to justify the Ohmic contact formation also in the case of an annealing in N_2, i.e. in the absence of oxygen in the atmosphere [155]. Considering all these works, even if the use of a Au/Ni bi-layer is undoubtedly useful to obtain Ohmic behaviour on p-GaN, many aspects related to the Ohmic contact formation and to the current transport mechanisms have not been fully explained yet. In this context, an exhaustive correlation of the macroscopic electrical parameters (like the specific contact resistance and the barrier height) with the contact microstructure is required. To clarify some of the open issues, in this thesis the electrical and structural evolution of Au/Ni contacts formed onto p-GaN was studied.

4.2 Electrical characterization of Au/Ni contacts to p-GaN

In our experiment a p-type (Mg-doped) GaN epitaxial layers grown on a (0001) sapphire substrate were used. The samples were supplied by the Institute of High Pressure Physics (Unipress) in Warsaw, Poland. The p-GaN epilayer had a thickness of 0.5 μm, and a nominal hole concentration of 6.8×10^{17} cm^{-3}, as determined by Hall measurements performed after growth by Unipress. A schematic (in cross section) of the used wafer is shown on *Fig. 4.1*.

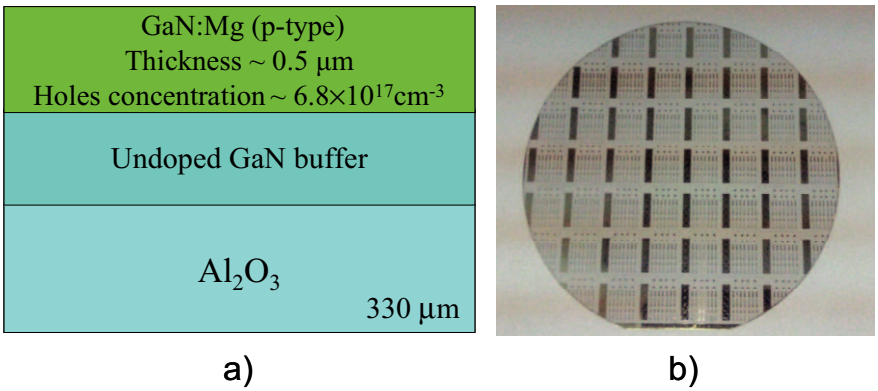

Fig. 4.1: *Schematic cross section of the p-GaN wafer used in our experiment (a), and picture of the entire processed wafer.*

The contacts were formed by sequential e-beam evaporation of Ni (20 nm) and Au (80 nm) on the sample surface. Even if many authors used very thin metal stacks to form Ohmic contacts to p-GaN (see *Table 4.1*), in our case we preferred to increase the thickness of the layers in order to guarantee the uniformity of the film over the entire 2-inches wafer.

The linear transmission line model (L-TLM) was used to determine the specific contact resistance of the contacts [166]. In this method, rectangular metallic pads at different distance are fabricated. The total resistance R_T

between adjacent pads is determined by four points probe current-voltage (I-V) measurements at the different distances *d*. By reporting the total resistance R_T as function of the pad distance *d*, a linear plot is obtained. From the linear fit of this plot, is possible achieve information on the contact properties. In particular, the sheet resistance of the material and the specific contact resistance can be extracted respectively from the slop and the intercept of the linear plot [167].

In order to fabricate the TLM patterns, first a lateral isolation of the structures was obtained by a plasma etch in Cl_2/Ar chemistry, creating deep trenches up to the Al_2O_3 substrate. Then the Au/Ni metal layer was deposited onto the sample surface, and the rectangular TLM pads (100×200 μm) were defined by standard lithography and sequential metal wet etch. The samples were subjected to rapid thermal annealing (RTA) for 60 s in a temperature range of 400-700 °C either in a N_2/O_2 mixture simulating the air composition (80% N_2, 20% O_2) or in Ar by using a Jipelec JetFirst furnace. In this way it was possible to compare the evolution of the Ni/Au bi-layer both in neutral and oxidizing ambient. A picture of the processed wafer after the electrical test-patterns formation is shown on *Fig. 4.1b*.

In order to determine the specific contact resistance ρ_c, current-voltage (I-V) measurements on several TLM patterns were carried out [168], before and after each annealing step, using a Karl Suss Microtec probe station equipped with a HP 4156B parameter analyzer.

The electrical characterization was first carried out by TLM measurements. The as-deposited contacts clearly exhibited a rectifying behaviour. Such a behaviour was maintained also after annealing at temperature up to 400 °C, irrespective of the annealing atmosphere (i.e., N_2/O_2 or Ar). The contacts showed an improvement of the I-V characteristic upon annealing above 400 °C. *Fig. 4.2* reports the I-V curves taken between two TLM pads at a distance of 5 μm, for the sample annealed in N_2/O_2 and Ar ambient at different temperatures. Clearly, with increasing the annealing temperature a reduction of the contact resistance occurs in both samples.

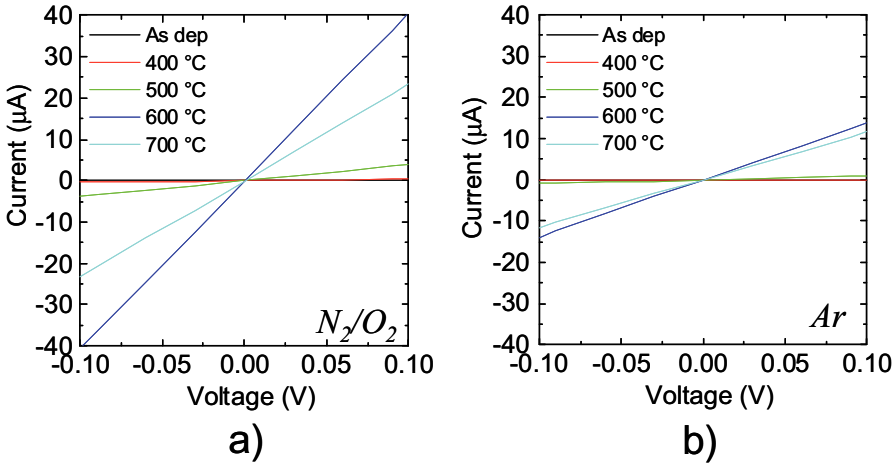

Fig. 4.2: *I-V characteristics for two TLM structure placed at distance of 5 μm. The curves are related to the as-deposited samples and the samples annealed in a temperature range between 400 and 700 °C in N_2/O_2 (a) and Ar (b) ambient.*

Fig. 4.3a and *Fig. 4.3b* show the I-V characteristics measured between TLM contacts at different distances for the sample annealed in N_2/O_2 and in Ar atmosphere at temperature of 600 °C. At this annealing temperature the best electrical characteristics (the highest current) were obtained. From the linear fit of the single I-V curves it is possible extract the total resistance for each distance (see *Fig. 4.4*). Then, by fitting the dependence of the R_T on the distance d, using the TLM method it was possible to possible extract information on the R_{sh} and ρ_c in the two different samples.

After annealing at 600 °C a specific constant resistance of $\rho_c = 2.85\times10^{-1}$ $\Omega\cdot cm^2$ was found for the sample annealed in Ar. On the other hand, the process in N_2/O_2 resulted into a ρ_c more than two orders of magnitude lower (2×10^{-3} $\Omega\cdot cm^2$). From TLM analysis similar values of the R_{sh} of the p-GaN layer were determined for the two samples, i.e. 19.7 kΩ/sq and 17.7 kΩ/sq, for the annealing in N_2/O_2 and in Ar, respectively. This latter result indicates that the annealing process (temperature and atmosphere) do not significantly modify the electrical properties of the p-GaN epilayer. The experimental values of R_{sh} extracted by TLM analysis are consistent with the value

determined by Hall measurements carried out by the material supplier (~ 17 kΩ/sq).

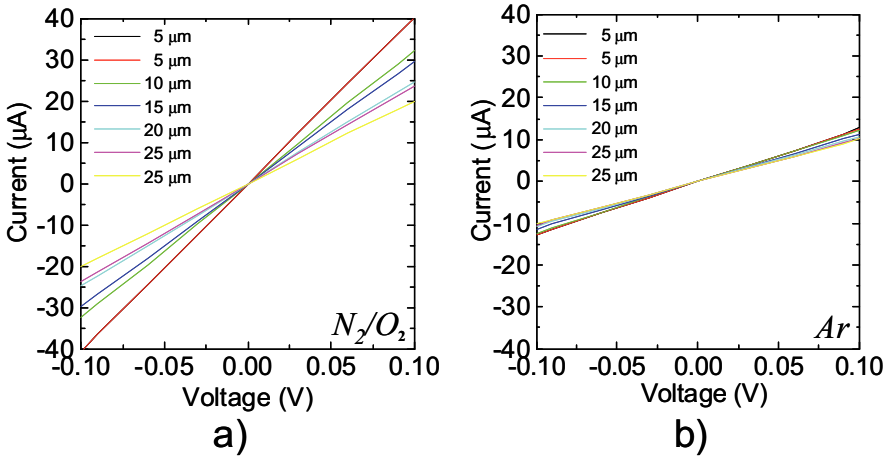

Fig. 4.3: *I-V characteristics for TLM structures at annealing temperature of 600 °C in in N_2/O_2 (a) and in Ar (b) ambient.*

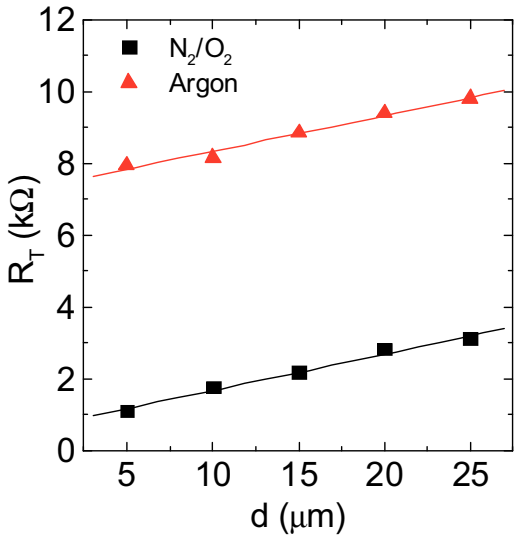

Fig. 4.4: *Total resistance R_T as a function of the distance d between TLM structures for Ni/Au contacts to p-type GaN annealed at 600 °C in in N_2/O_2 or Ar. The linear fits of the data are also reported.*

The values of the specific constant resistance ρ_c, determined using TLM analysis, are reported in *Fig. 4.5* as a function of the annealing temperature. Several measurements were carried out on different patterns and the statistical error bars are reported in the figure for each value. As can be seen, a gradual improvement of the electrical properties of the contacts occurs independently of the atmosphere, as the values of ρ_c decrease with increasing the annealing temperature. It is worth noting that, independent of the annealing temperature, the contacts annealed in N_2/O_2 always showed better I-V characteristics and lower specific contact resistance of that those annealed in Ar.

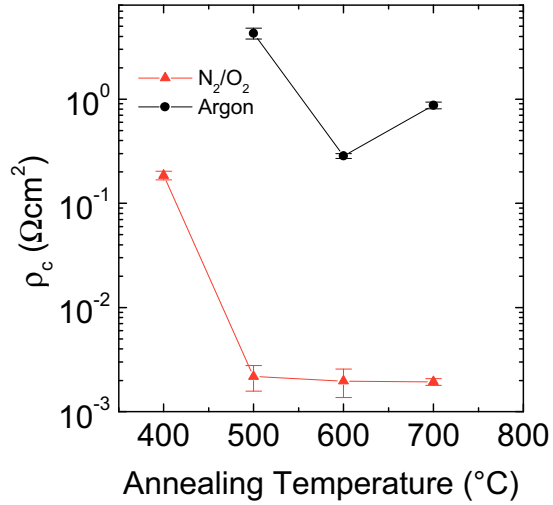

Fig. 4.5: *Specific constant resistance versus annealing temperature in N_2/O_2 and in Ar ambient.*

4.3 Structural characterization

The changes of the electrical properties of the contacts after annealing treatments described in the previous paragraph were correlated with the evolution of the contact microstructure. The structural characterization has

been performed using X-Ray Diffraction (XRD) analysis and Transmission Electron Microscopy (TEM). In particular, by XRD analysis it was possible to monitor the structural evolution of the samples at different annealing temperatures in terms of phases formation, while TEM analysis in cross section was used to observe the difference at the interfaces (for the samples annealed at 600°C).

The XRD analysis was performed in grazing mode using a Bruker-AXS D5005 θ-θ diffractometer operating with a Cu K_α radiation at 40 kV and 30 mA. The XRD patterns of Au/Ni contacts onto p-type GaN after rapid thermal treatments in Ar and N_2/O_2 at the temperatures of 400, 500 and 600 °C have been collected in order to follow the structural evolution of the system. They are shown in *Fig. 4.6*.

Up to an annealing temperature of 400°C in Ar (*Fig. 4.6a*), the XRD pattern showed only peaks at 2θ = 38.2° and 44.4° due to the (111) and (200) Au reflections, respectively. Ni reflections were not observed since the Ni layer is very thin and its major intensity peak is overlapped to the (200) Au reflection. Thus, no difference has been observed by XRD patterns with respect to the as-deposited Au/Ni stack.

At temperatures higher than 400°C, an additional peak at 2θ = 38.9° is present in the XRD patterns of the sample annealed in Ar, that can be attributed to the formation of a Au-Ni solid solution. Indeed, the phase diagram of Au-Ni system indicates a mutual solubility in the solid state, since both metals possess a fcc structure, but with an atomic size difference of 13.6% [169]. In particular, the peak at 38.9° can be associated to a compound having a smaller plane distance with respect to the pure Au, which in turn is consistent with the incorporation of smaller Ni atoms into the Au lattice.

A different evolution of the metal structure was observed in the sample annealed in N_2/O_2 mixture (*Fig. 4.6b*). Also in this case no change of the XRD pattern was observed up to 400°C. However, additional features, associated with the formation of nickel oxide (NiO), appear beside the Au peaks at an annealing temperature of 500°C, i.e. at the onset temperature where a significant reduction of the specific contact resistance was observed by TLM analysis (see *Fig. 4.5*).

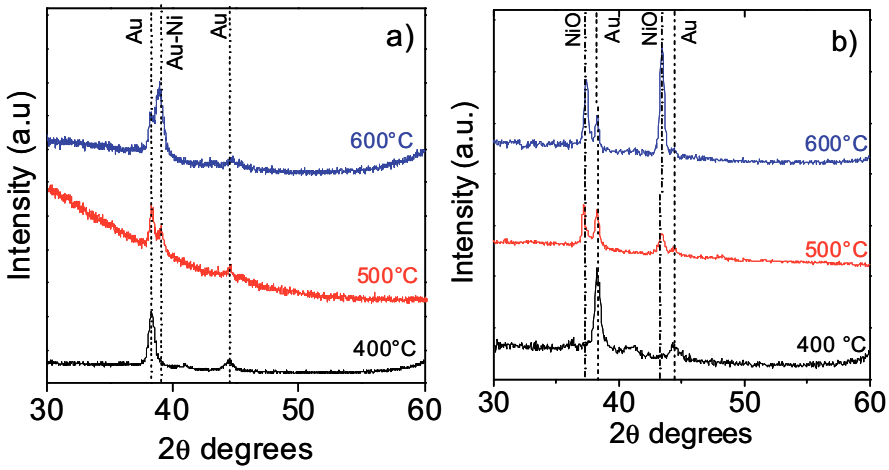

Fig. 4.6: *XRD patterns for Au/Ni contacts onto p-GaN, annealed in Ar (a) and N_2/O_2 (b) at temperatures of 400, 500 and 600°C.*

Although some authors correlated the improvement of Au/Ni/p-GaN contacts with the formation of NiO, contrasting interpretations on its impact on the electrical properties have been reported [160,165]. For that reason, besides the phase identification obtained by means of XRD, it is important to get insights on the contact morphology and on the spatial arrangement of the formed phase (grains) inside the annealed layer. Hence, in this work complementary information on the sample microstructure was obtained by cross section TEM analysis.

The TEM analysis in cross section was performed using a 200 kV JEOL 2010 F microscope, equipped with Energy Dispersive X-Ray diffraction (EDX).

These analyses were carried for the samples annealed at 600° C to obtain a direct imaging the distribution of the different phases inside the metal layer. *Fig. 4.7a* and *Fig. 4.7b* show the TEM micrographs of the sample annealed in Ar and the sample annealed in N_2/O_2 ambient, respectively. The sample annealed in Ar (*Fig. 4.7a*) shows that the original deposition sequence of the metals is almost unaltered, with the Ni layer that is present at interface at the with p-GaN and a Au layer on the top of it. However, on the contact surface a thin non-uniform layer is also observed, identified as

oxidized Ni by a local energy dispersive X-ray analysis. This experimental evidence clearly indicates that Ni diffused inside the Au layer (as confirmed by the Au-Ni signal observed in the XRD patterns), and a partial oxidation of the Ni atoms reaching the surface has occurred.

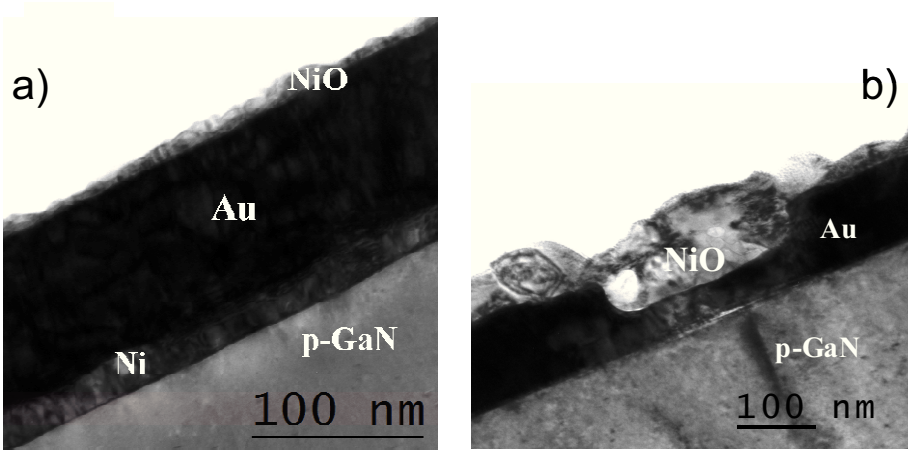

Fig. 4.7: *Bright field TEM micrographs in cross section for Au/Ni/p-GaN contacts annealed at 600 °C in Ar ambient (a) and in N_2/O_2 ambient (b).*

On the other hand, in the sample annealed in N_2/O_2 ambient, TEM analysis showed a modification of the original sequence of the metal layers (*Fig. 4.7b*). After annealing at 600°C a Au layer is found directly in contact with the p-GaN, while the Ni is fully oxidized and a continuous NiO layer is visible with a brighter contrast on the sample surface. The different microstructure of the samples observed after annealing in N_2/O_2 suggests that the out-diffusion of Ni is enhanced by the presence of oxygen in the annealing atmosphere. It must be noted that the absence of the NiO directly at the interface with the p-GaN is in contrast with the previous interpretation considering interfacial NiO, acting as a p-type semiconductor, as a key factor for ohmic contact formation [154].

At this point, the structural evolution of the analyzed system can be explained with a simple scenario based both on the information achieved by the XRD and TEM analysis and on thermodynamic considerations taken

from the literature. A schematic is reported in *Fig. 4.8*. For temperature higher than 400 °C the metallic species as Au and Ni become mobile and a mutual inter-diffusion occurs. In particular, due to the higher solubility of Ni in Au (25%) with respect to that of Au in Ni (5%), incorporation of Ni inside the Au layer is favoured [156]. On the other hand, Ni atoms, diffused inside the Au and reached the surface, where they could be easily oxidized during N_2/O_2 annealing. The formation of NiO is energetically favoured (with respect to Au-Ni solid solutions) because of its more negative value of the Gibbs free energy (ΔG= -83.7 kJ/mol) [170]. This fast oxidation process acts as a driving force for further out-diffusion of Ni atoms, until the entire Ni metal layer is transformed in the observed continuous NiO surface layer. As a consequence of this process, the reversal of the original deposition sequence of the metal layer occurs (NiO/Au/p-GaN).

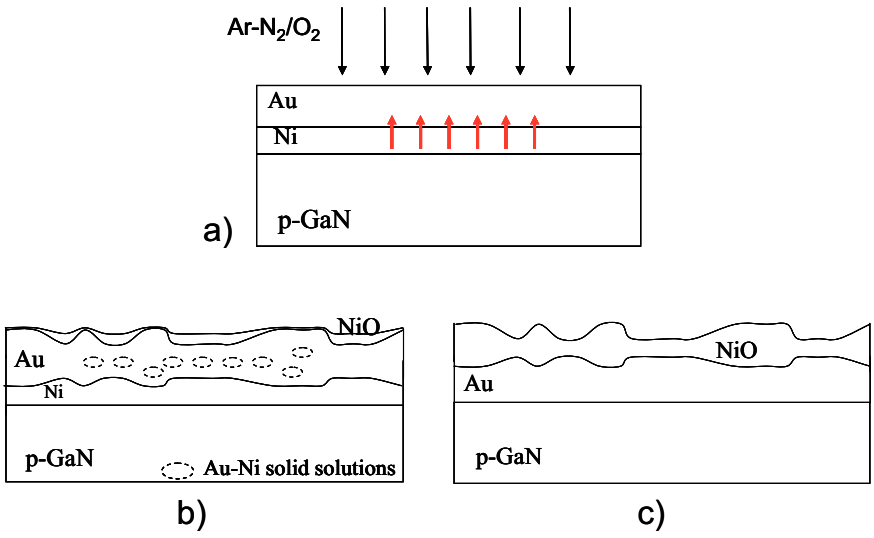

Fig. 4.8: *Schematic of the possible scenario of the evolution of Au/Ni bilayers upon annealing: indiffusion of Ni inside the Au layer (a), and subsequent evolution in the case of annealing in Ar (b) or in N_2/O_2 ambient (c).*

Obviously, Ni diffusion inside the Au film takes place also when the annealing is performed in Ar atmosphere. However, in this case, only a

partial oxidation occurs at the surface due to residual oxygen in the annealing chamber and/or to the subsequent exposure to air of the metal stack. Hence, during annealing in Ar the complete out-diffusion of Ni does not occurs, and a significant fraction of the original deposited Ni layer remains at the interface with p-GaN.

4.4 Nanoscale morphological and electrical analysis

To better investigate the role of the NiO formed in the annealed contacts, the measure of surface morphology of the contacts and the local electrical measurements on the metal layers were performed respectively by Atomic Force Microscopy (AFM) and by Conductive Atomic Force Microscopy (C-AFM). These measurements were performed using a Veeco Dimension 3100 in AFM and C-AFM mode operation, respectively. The morphological analysis (by AFM) and local current measurements (by C-AFM) were performed in the samples annealed at 600 °C in the two different conditions. The use of C-AFM has been already described in chapter 3, as a tool to monitor the modification of AlGaN after near-surface processing. Additionally, this nanoscale technique has been already successfully employed in the past to study the nanoscale transport properties of Ti/Al/Ni/Au Ohmic contacts to GaN-based materials. In particular, C-AFM, combined with XRD and TEM, allowed to demonstrate that the current transport through Ti/Al/Ni/Au Ohmic contacts is strongly dependent on the nanostructure of the entire reacted metal layer and on the electrical properties of the different phases formed (AlNi, $AlAu_4$, Al_2Au) [133].

The C-AFM measurements were carried out in two different configurations, a lateral configuration (see *Fig. 4.9a*) to extract information about the conductivity of the metal stack, and a vertical configuration (see *Fig. 4.9b*) to evaluate the local current transport at metal/p-GaN interface.

In the lateral configuration, a large-area electrode was deposited on part of the contact to GaN. A dc bias was applied between this macroscopic electrode and a nanometric conductive AFM tip scanned on the metal surface. For each tip position during the scan, the current between the macro and nanoscale contacts was measured by a current amplifier connected to the tip and a two-dimensional current map was collected. Current flow between the two electrodes is mainly limited by current spreading from the nanometric tip contact to the underlying metal. Since this spreading resistance contribution is related to the local resistivity of the metal region under the tip, the measured current map provide nanoscale information on the homogeneity of the metal film electrical properties [171]. Those properties can be correlated with the morphology and microstructure of the contacts.

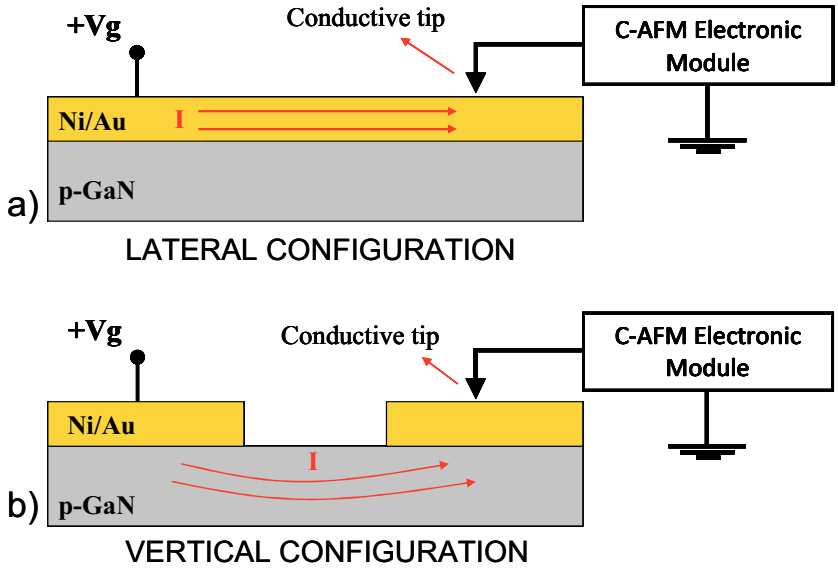

Fig. 4.9: *Schematic of the system used for C-AFM measurements in lateral (a) and vertical (b) configuration.*

In Fig. 3.10, it is possible to observe an interesting correlation between the surface morphologies (determined by AFM) and the corresponding two-

dimensional current maps (determined by C-AFM), for both annealing conditions. The sample annealed in Ar shows a surface roughness with a *root mean square (RMS)* of 5.5 nm, lower than in the sample annealed in N_2/O_2 (RMS=13.5 nm). The morphology of the contacts annealed in Ar exhibit surface "hillocks" that could be associated with the NiO agglomeration at the surface, region well visible also in the corresponding TEM images (*Fig. 4.7a*). The corresponding current map is inhomogeneous and shows a lower conductivity close to the NiO grains present on the surface. A similar correlation between the morphology and the current maps could be established also for the contacts annealed in N_2/O_2. In this case the region that presents a local lower conductivity can be associated to regions with a different thickness of the metal layer, i.e. where a thinner underlying Au layer below the NiO surface layer is observed. Also this point is consistent with the corresponding TEM images (*Fig. 4.7b*).

Moreover comparing the current maps related to the two samples it is clear that the sample annealed in Ar shows an overall higher level of current with respect to the sample annealed in N_2/O_2.

This results has been found to be consistent with macroscopic *four point probe* [168] measurements of the sheet resistance performed on the two samples. These experimental measurements gave the values of 0.51 Ω/sq and 1.18 Ω/sq, respectively for the sample annealed in Ar and in N_2/O_2 ambient. The reason of the higher resistivity found in the N_2/O_2 annealed sample can be found in the continuous NiO layer presents on the surface of the metal stack.

On the other hand, the C-AFM measurements carried out in the vertical configuration gave information about the local current transport at the metal/p-GaN interface. In this case a large-area electrode was deposited on part of one contact to p-GaN, while the nanometric conductive AFM tip scanned an adjacent (5 μm distance) metal contact. In this way for each tip position during the scan, the current flowing across the metal/p-GaN interface was collected (*Fig. 4.9b*).

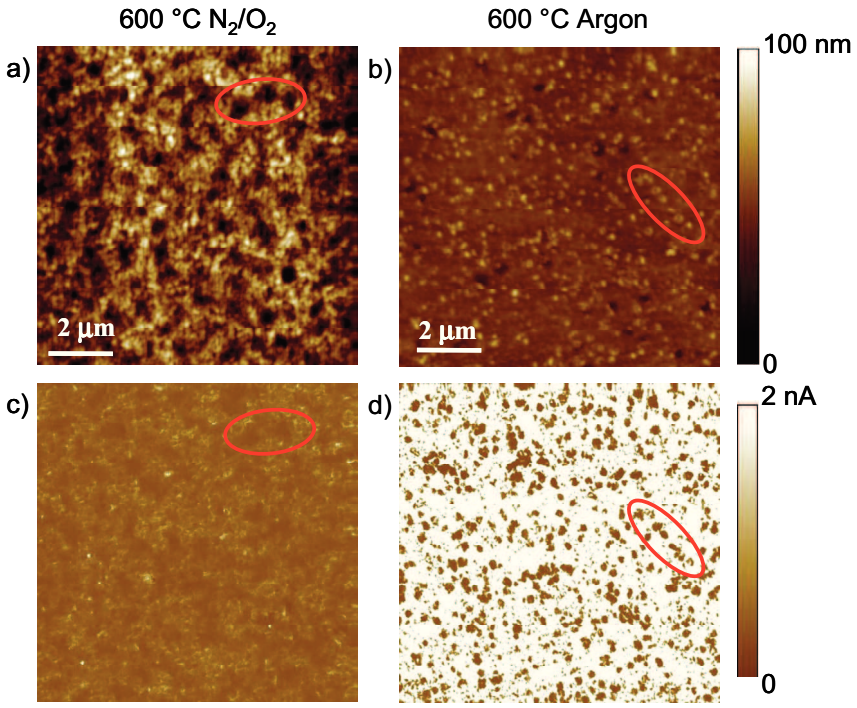

Fig. 4.10: *Morphological AFM images of Au/Ni contacts to p-GaN annealed at 600 °C in N_2/O_2 (a) and Argon (b). Local current maps collected by C-AFM, arranged in lateral configuration, for Au/Ni contacts annealed at 600 °C in N_2/O_2 (c) and Argon (d).*

The current maps acquired in vertical configuration show an inhomogeneous distribution of current in both the samples, that is related to the formation of an inhomogeneous barrier at metal/p-GaN interface. Moreover an opposite result with respect to those acquired in lateral configuration was achieved. In this case, comparing the two maps, it is clear that an higher current flows through the interface in the N_2/O_2 annealed sample, showing a map with an higher level current with respect to the that of the sample annealed in Ar ambient. This results is consistent with the macroscopic electrical measurements that showed a significantly lower specific contact resistance for the sample annealed in N_2/O_2 ambient.

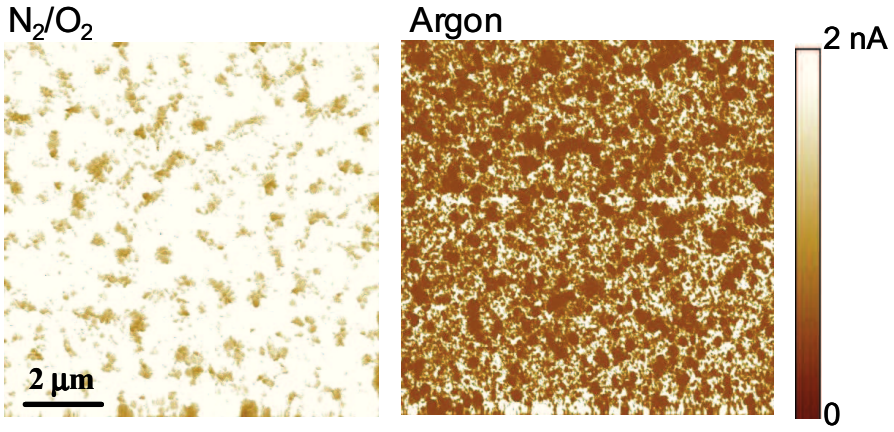

Fig. 4.11: *Local current maps collected by C-AFM, arranged in vertical configuration, for Au/Ni contacts annealed at 600 °C in N_2/O_2 (c) and Argon (d).*

Hence, the improved electrical contact properties cannot be explained by the presence of NiO itself (that actually influences the resistivity of the metal contact and is not present at the interface with p-GaN), but must be correlated with the different interfacial structure of the two samples. In order to obtain further accurate information about the current transport mechanisms at the metal/p-GaN interface, a temperature dependence of the electrical characteristics was carried out and is described in the next paragraph.

4.5 Temperature dependence of R_{sh} and ρ_c

The temperature dependence of the sheet resistance of the p-GaN layer and of the specific contact resistance of the annealed Au/Ni contacts have been studied to achieve information on the carrier transport mechanism through the interface.

The measurements were performed in the range 25-150 °C, varying the chuck temperature using a Lakeshore 331 temperature controller. They were

carried out on the samples annealed at 600 °C in both ambient conditions (Ar and N_2/O_2).

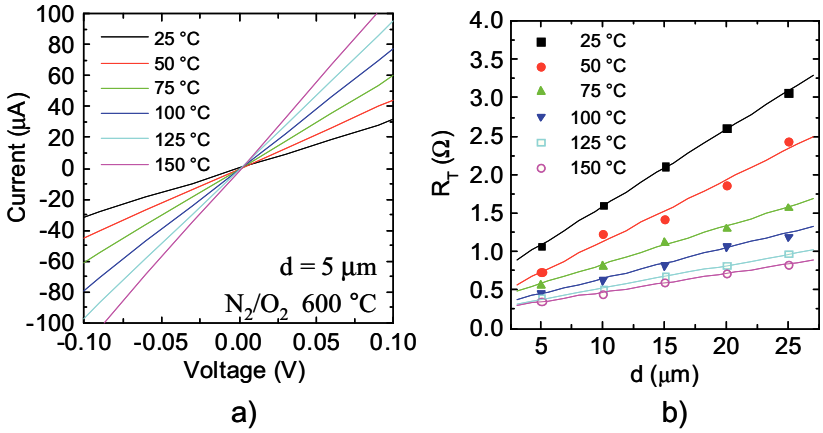

Fig. 4.12: *I-V characteristics acquired between two adjacent TLM pads placed at distance of 5 μm (a) and the total resistance R_T vs distance d (with the corresponding linear fits), at different measurement temperatures , for the sample annealed in N_2/O_2 at 600 °C.*

Fig. 4.12a shows, as an example, the I-V characteristics acquired between two adjacent TLM pads placed at distance of 5 μm at different temperature conditions, for the sample annealed in N_2/O_2 at 600 °C. Using the TLM method, from the linear fit of the *total resistance* R_T it was possible to extract both the sheet resistance R_{sh} of the samples and the specific contact resistance ρ_c of the contact onto p-GaN. *Fig. 4.12b* shows the plots of R_T vs d (and the correspoding linear fits) at different measurement temperatures, for the sample annealed in N_2/O_2 atmosphere at 600°C.

Both annealing conditions gave a R_{sh} that decreases with increasing temperature T, from around 20 kΩ/sq at room temperature to 5 kΩ/sq at 425 K (see *Fig. 4.13a*). Considering a layer of thickness t with a uniform carrier concentration, the temperature dependent sheet resistance $R_{sh}(T)$ is related to the free holes concentration $p(T)$ and to the holes mobility μ_p by the relation:

$$R_{sh}(T) = \frac{1}{q\mu_p(T)p(T)t} \qquad \text{(Eq. 4.1)}$$

where q is the elementary charge.

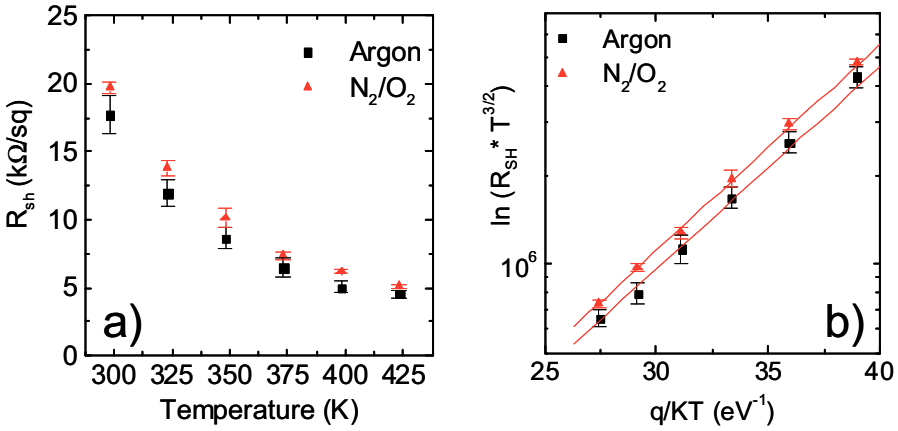

Fig. 4.13: *Temperature dependence (a) of the sheet resistance R_{sh} and (b) semi-logarithmic plot of $R_{sh}\cdot T^{3/2}$ as a function of q/kT, for the samples annealed in Ar and N_2/O_2 at 600°C.*

For a p-type semiconductor, the net free hole density $p(T)$ depends on both the concentration of acceptor (N_A) and of compensating donor centers (N_D) [172]. In particular, in the examined temperature range, the temperature dependence of free hole concentration $p(T)$ can be expressed by a simplified form [168]:

$$p(T) \approx \frac{(N_A - N_D)N_V}{gN_D}\exp\left(-\frac{E_A}{kT}\right) \qquad \text{(Eq. 4.2)}$$

where N_V is the effective density of states in the valence band, g the degeneracy factor for acceptors (usually taken as 2 [173]), k is the Boltzmann constant, T the absolute temperature and E_A the ionization energy of acceptors referred to the top of the valence band.

Hence, using the expression of N_V [172], and combining Eq. 4.1. with Eq. 4.2, it is possible to give an expression for the temperature dependence of R_{sh} :

$$R_{sh}(T) = T^{-\frac{3}{2}} \frac{gN_D}{N_A - N_D} \frac{h^3}{2(2\pi m^* k)^{3/2}} \frac{1}{qt\mu_p} \exp\left(\frac{E_A}{kT}\right) \qquad \text{(Eq. 4.3)}$$

where h is the Plank constant, ε_0 is the dielectric vacuum permittivity, ε_{GaN} is the dielectric permittivity for GaN, m^* is the effective mass for holes in GaN. In Eq. 4.3, the temperature dependence of the hole mobility has been neglected with respect the exponential dependence contained in the expression of $p(T)$.

Hence, reporting in an Arrhenius plot the logarithm of $R_{sh} \cdot T^{3/2}$ as a function of the inverse of the absolute temperature *1/T,* the activation energy (E_A) for Mg-dopant impurities has been determined. The semi-logarithmic plot of $R_{sh} \cdot T^{3/2}$ as a function of *q/kT,* is reported in *Fig. 4.13b* for both Ar and N_2/O_2 annealed samples. As it can be seen, the experimental data follows an Arrhenius law according to Eq. 4.3. From a linear fit of the data, a value of the activation energy E_A of about 160 meV was found in both samples.

For Mg-doped GaN, the values of the activation energy E_A for acceptors are typically in the range 150-180 meV, and exhibit a strong dependence on the acceptor concentration N_A [174]. Indeed, the experimental value of 160 meV found in our samples is consistent with the data reported by Kozodoy et al. [175] for an acceptor concentration N_A of the order of ~8.6×10^{19} cm^{-3}.

On the other hand, from the temperature dependence of the ρ_c it was possible to obtain information on the current transport mechanism at metal/semiconductor interfaces [141,176]. According to the classical description, comparing the *thermal energy kT* with the *characteristics energy* E_{00} that depends on the doping density of the semiconductor N is possible have information on the dominant carrier transport mechanism at the metal/semiconductor interface. The *characteristics energy* E_{00} establishes a relation between the temperature T and the semiconductor net doping concentration $N=(N_A-N_D)$, and can be express as [168]

$$E_{00} = \frac{h}{4\pi}\left(\frac{N}{m^{*}\varepsilon_{GaN}\varepsilon_{0}}\right)^{\frac{1}{2}} \qquad \text{(Eq. 4.4)}$$

By the ratio kT/qE_{00} is possible to quantify the predominance of *thermionic emission* (TE) of the carriers over the barrier on other contributions, like *thermionic field emission* (TFE) or *field emission* (FE) [177]. Comparing the thermal energy kT with the characteristic energy E_{00} calculated using the estimated acceptor concentration level (Eq. 4.4), in the investigated range (25-150°C), a value of $kT/qE_{00} \approx 1.65\text{-}2.47$ is obtained. This ratio suggests that TFE can be assumed to be the dominant current transport mechanism [178]. in fact a simple thermionic emission model was not able to fit the experimental dependence of ρ_c on temperature. The experimental dependence of the specific contact resistance ρ_c as a function of the temperature T was fitted using the TFE model.

The values of ρ_c as a function of T and the corresponding TFE fits, for both Ar and N_2/O_2 annealed samples, are shown in *Fig. 4.14*. According to the TFE model, the specific constant resistance can be expressed as:

$$\rho_C(T) = \left(\frac{1}{qA^{*}}\right)\frac{k^2}{\sqrt{\pi(\phi_B + V_n)E_{00}}}\cosh\left(\frac{E_{00}}{kT}\right)\times \\ \times\left[\sqrt{\coth\left(\frac{E_{00}}{kT}\right)}\right]\exp\left(\frac{\phi_B + V_n}{E_0} - \frac{V_n}{kT}\right) \qquad \text{(Eq. 4.5)}$$

where

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right) \qquad \text{(Eq. 4.6)}$$

and A^{*} is the Richardson constant, V_n is the energy difference between the valence-band edge and the Fermi level. For all our calculations we used the literature value of $\varepsilon = 8.9\varepsilon_0$, ε_0 being the permittivity in free space, $A^{*} = 27.9$ A/cm^{2}K^2, and $m^{*} = 0.81m_0$, m_0 is the free electron mass [179]**.**

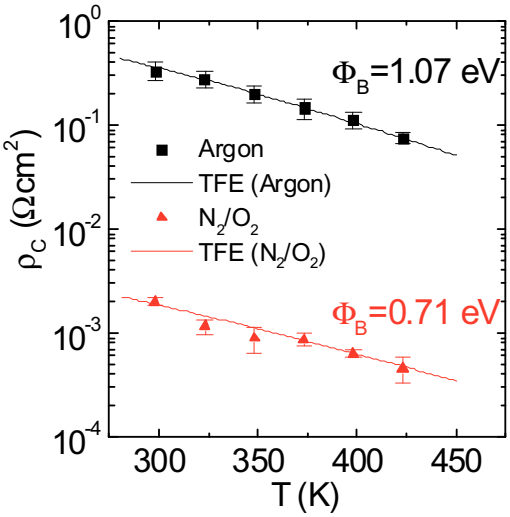

Fig. 4.14: *Specific contact resistance ρ_c as a function of temperature T for the Au/Ni contacts to p-GaN annealed at 600 °C in Ar and N_2/O_2 ambient. The continuous lines are the fits obtained using the TFE model, from which the values of the barrier height Φ_B were determined.*

The fit of the data with the TFE expression of ρ_c allowed to determine the metal/p-GaN barrier height Φ_B and the carrier concentration N. In particular, for the Ar annealed sample a Schottky barrier height of 1.07 eV was found, with a carrier concentration N= 6×10^{19} cm^{-3}. On the other hand, in the case of the sample annealed in N_2/O_2 the barrier Φ_B was lowered to 0.71 eV, while N had a similar value (5×10^{19} cm^{-3}). The two different values of Schottky barrier height are explained by the different interfacial microstructure observed by TEM analysis (see *Fig. 4.7*), i.e. the formation of NiO/Au/Ni/p-GaN system upon annealing in Ar atmosphere, and NiO/Au/p-GaN in N_2/O_2 atmosphere. This results is also consistent with the C-AFM analysis conducted in vertical configuration, that showed a high level current flowing the interface in case of the sample annealed in oxidizing ambient.

Basing on all the aforementioned experimental data, considering previous literature finding as supporting arguments it was possible to imagine a possible scenario which explains the results.

For Ni/Au contacts to p-GaN annealed in N_2/O_2 similar value of Φ_B was estimated by Koide *et al.* [180]. They attributed the reduction of ρ_c in oxidizing atmosphere to an increase of the hole concentration in p-GaN, rather than to a decrease of the barrier height [180]. However, an increase of the carrier concentration could not be demonstrated by our analysis, since the values of N and R_{sh} of p-GaN (determined by the TLM) were similar in both samples, and consistent with the nominal concentration given by the supplier. Therefore, the main explanation for the improvement of the specific contact resistance should be mainly attributed to the lower barrier height (0.71 eV) of the sample annealed in N_2/O_2.

To further corroborate this picture, it should be noted that NiO was not observed at the interface with p-GaN, in contrast with the previous interpretation, that consider NiO an interfacial p-type semiconductor with a low barrier, beneficial for Ohmic contact formation [154]. Moreover the presence of Au at the interface to p-GaN does not explain the electrical behaviour of the contacts. In fact, only a non-Ohmic behaviour or a high specific contact resistance are typically observed for pure Au/p-GaN contacts [159,160].

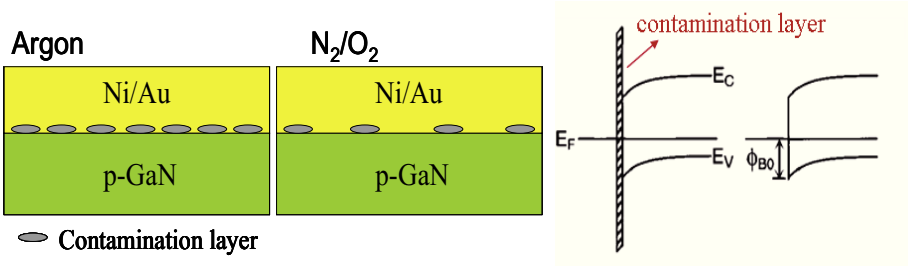

Fig. 4.15: *Schematic of the possible scenario that explain the lowering of the effective Schottky barrier height by the reduction of the elimination of the contamination layer at metal/p-GaN interfaces.*

Rather, it can be argued that the entire structural evolution process leading to the reversal of the original sequence of the deposited layers is crucial for the improvement of the contact properties. Ishikawa *et al.* [181] compared the behaviour of different metals (Ti, Ta, Ni, Pt, Au) on p-GaN upon annealing, showing that a native surface contamination layer (consisting of GaO*x* and adsorbed carbons) can be efficiently removed by annealing Ni and Ta contacts deposited on GaN. Hence, in our case it can be inferred that during annealing in N_2/O_2, the Ni out-diffusion can favour the partial elimination of any native contaminant present on the p-GaN surface. Schematic of this explanation is showed in *Fig. 4.15*. This latter in turn leads to a reduction of the effective Schottky barrier height and, hence, to a lower specific contact resistance. Indeed, the elimination of the contamination layer at metal/p-GaN interfaces is expected to produce a lowering of the barrier height of 0.2-0.3 eV [181], similar to that observed experimentally in our samples.

Chapter 5: AlGaN/GaN enhanchement mode HEMTs structures using p-type GaN gate contact

The impact of a p-GaN cap layer on the AlGaN/GaN heterostructure has been investigated in this chapter. In particular, the fabrication and characterization of specific test patterns and HEMT devices demonstrated that the presence of a p-GaN cap layer promotes the depletion of the 2DEG, leading to a significant positive shift of the threshold voltage. Hence, basing on simulation of the band structures, an optimized layout was defined, that allowed to obtain a normally-off condition with a threshold voltage of 1.4 V.

5.1 Critical issue for an enhancement mode HEMT using a p-GaN gate

As widely discussed in the chapter 2, the realization of enhancement mode (normally-off) HEMT devices represents an important challenge for applications of GaN in power electronics [182,183]. However, the normally-on ($V_{th} < 0$) operation is intrinsic in the nature of a conventional AlGaN/GaN heterostructure, in which a two dimensional gas of electrons (2DEG) is present at the interface between the two materials. Hence, it is important to understand the possible physical mechanisms that can be used

to control the threshold voltage V_{th} in such a two dimensional system, by studying appropriate treatments of the near-surface region (few nanometres) of the AlGaN barrier layer.

An overview of the possible approaches for the fabrication of normally-off AlGaN/GaN HEMTs reported in the literature has been already given in chapter 2, showing that a lot of work is still required before reaching an enhancement mode structure with an accurate control of the 2DEG.

Among these approaches, in the last years, the possibility to achieve a normally-off behaviour using a p-type GaN cap layer under the gate contact has been investigated by some authors [52,131,184]. The use of p-type doped semiconductor as gate onto the AlGaN/GaN heterostructure is able to lift up the potential in the channel region depleting the 2DEG channel even in the absence of an external applied bias. With respect to other methods, the use of a p-type GaN gate can combine the high-mobility of the 2DEG channel known from AlGaN/GaN HEMTs with secure normally-off operation, required in power switching applications. Furthermore, such an approach can benefit by the conductivity modulation effect provided by the injection of holes from the p-gate to the channel, leading to an increase of the drain current [52]

Several possible solutions based on this new concept have been investigated, as the use of a Mg-doped GaN [131] or AlGaN [130] cap layer. . Also enhancement mode HEMTs fabricated with the use of a p-type semiconducting nickel oxide (NiO_x) layer as gate layer has been presented [185].

Clearly, although the physical concept at the basis of this approach seems to be easy, several practical difficulties arise when fabricating devices onto p-GaN/AlGaN/GaN heterostructures and obtaining a normally-off behaviour is not straightforward.

In this chapter , the mechanism of the modulation of the threshold voltage using of a p-GaN cap layer has been studied considering different heterostructures. Several fundamental parameters have to be considered when studying the physics of the p-GaN/AlGaN/GaN system. As an example, key factors are the Mg concentration in p-GaN, the residual donor concentrations in undoped AlGaN and undoped GaN layers, the Al concentration and the thickness of the AlGaN barrier layer. In particular, in

order to obtain a good quality p-n junction, these heterostructures should contain an high acceptor concentration in Mg doped p-GaN, while the residual donor concentration in AlGaN and GaN layers should be low [186]. Anyway, by increasing the Mg concentration in p-GaN (up to 3×10^{19} cm^{-3}) can lead to a deterioration of the crystalline quality of the layer and to a decrease in the hole concentration [187]. Concerning the Al content and the thickness of the AlGaN barrier layer, in chapter 2 it has been already discussed the way how these parameters influence the sheet carrier concentration n_S of the 2DEG (see for example Eq. 2.8 and *Fig. 2.7*). In the following paragraphs, the experimental data and simulation performed during this work of thesis will be shown, demonstrating that the depletion of the 2DEG channel in a p-GaN/AlGaN/GaN heterostructure can only arise from an optimal balance of key parameters like the sheet carrier concentration n_S of the AlGaN/GaN channel, the Al concentration and the thickness of the AlGaN barrier layer [186]. The results pave the road to achieve a reliable control of the threshold voltage in the 2DEG and, ultimately, an optimal normally-off GaN HEMT.

5.2 Fabrication and characterization of p-GaN/AlGaN/GaN HEMTs

This paragraph describes the fabrication procedure and the results of electrical characterization of p-GaN/AlGaN/GaN HETM structures, which was used as first investigation to understand the effect of the p-GaN capping layer under the gate contact on the threshold voltage V_{th}.

For this study p-GaN/AlGaN/GaN heterostructures grown onto 150 mm Si (111) wafers supplied by STMicroelectronics were used. A schematic of the cross section of the processed sample and the corresponding bright field TEM image acquired in the upper part of the heterostructure are showed in *Fig. 5.1a* and *Fig. 5.1b*, respectively. As can be seen, there is a good agreement between the nominal and the real thickness of the p-GaN and

AlGaN layers. The mask design included different test patterns for electrical analysis, i.e. TLM structures, linear test structures to evaluate the impact of the p-GaN, round Schottky diodes, HEMTs structure both with a linear and a circular geometry. The mask design is reported in *Fig. 5.2*.

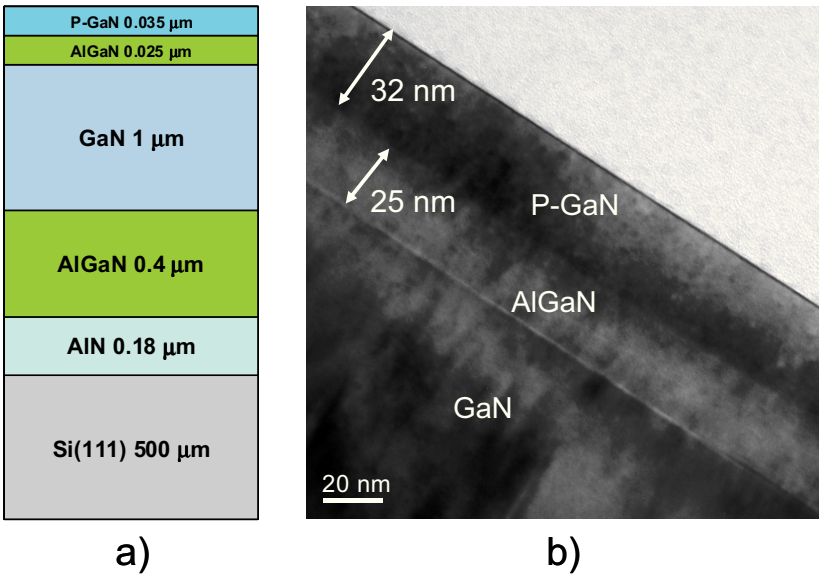

Fig. 5.1: *Schematic cross section of the sample used in our experiment (a), and the bright field TEM micrograph image of the upper part of the heterostructure (b).*

Diodes and HEMTs structures have been fabricated with the gate electrode onto the p-GaN cap layer. As a reference, the same test structures were fabricated with the gate electrode on the regions where the p-GaN cap layer was etched. The Ohmic contacts were done onto the AlGaN (e.g., where the p-GaN cap was etched). A description of the fabrication flowchart for these devices and test patterns is reported in the *Table 5.1*. The processing was carried out using the clean room

equipments of CNR-IMM: some steps were performed in the R&D line at ST Microelectronics of Catania.

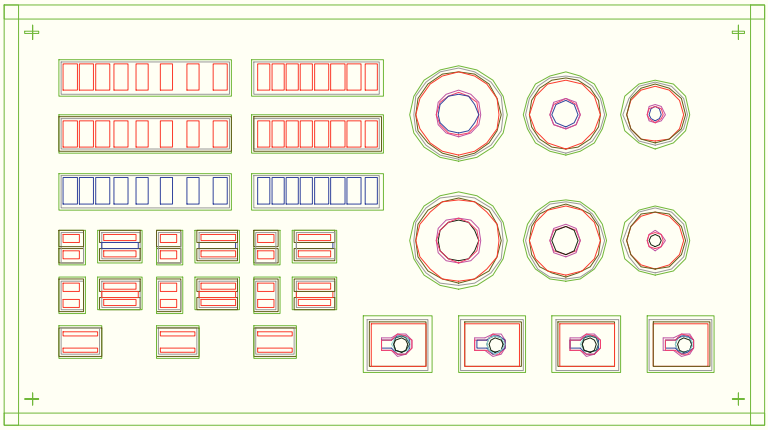

Fig. 5.2: *Mask design used to fabricate the test pattern*

Step #	Process	Description	Laboratory
1.	Cleaning of the wafer	Solution of HF:HCl:H_2O = 1:1:10	CNR
2.	Hard mask deposition	800 nm of SiO_2 (8k TEOS)	ST
3.	Photolithography zero layer	Resist AZ1518	CNR
4.	Etching of the SiO_2 mask	Solution NH_4F:HF = 7:1	CNR
5.	Isolation trench fabrication for linear structures	65nm GaN dry etch in CHF_3	CNR
6.	Photolithography for definition of the p-GaN	Resist AZ1518	CNR
7.	Etching of the SiO_2 mask	Solution of NH_4F:HF = 7:1	CNR
8.	Selective plasma etch of the p-GaN layer (35 nm)	Plasma selected etching in $Cl_2/Ar/O_2$	ST

9.	Removal of the residual SiO_2	Solution of NH_4F:HF = 7:1	CNR
10.	Metal deposition (Ti/Al/Ni/Au)	Thickness of 15/200/50/50 nm	CNR
11.	Photolithography for the Ti/Al/Ni/Au metal definition	Resist AZ1518	CNR
12.	Etching of the Ti/Al/Ni/Au metal	- Au etched by KI:I_2:H_2O - Ni etched by HNO_3:H_2O=1:20 - Ti etched by NH_4OH:H_2O_2:H_2O = 1:1:5 - Al etched by H_3PO_4:HNO_3:CH_3COOH:H_2O	CNR
13.	Annealing of the Ti/Al/Ni/Au metal	800 °C in Ar atmosphere	CNR
14.	Photolithography for the gate definition	Resist ARP-5350	CNR
15.	Metal deposition (Ni/Au)	Thickness of 30/120 nm	CNR
16.	Lift-off for the Ni/Au gate definition	Acetone	CNR
17.	Annealing of the Ni/Au gate	400 °C in Ar atmosphere	CNR

Table 5.1: *Schematic flow chart for the fabrication of HEMTs using p-GaN cap layer under the gate contact.*

A key factor for the fabrication of a functional p-GaN/AlGaN/GaN HEMT is the selective plasma etch of the p-GaN layer. In fact, the p-GaN layer must be removed everywhere, except in the region below the gate

electrode of the transistor. The selective plasma etch was carried out in the STMicroelectronics using the equipment LAM 9600. The etch was carried out in a chemistry of Ar, O and Cl [188]. To evaluate the results of the etching process, both AFM and TEM analysis were used.

The AFM images, showed on *Fig. 5.3*, compare the morphology of the p-GaN cap layer surface with the surface of the AlGaN after the p-GaN etch. The roughness measurements showed a root mean square (RMS) of 5.02 nm for the p-GaN surface. while RMS=5.54 nm was found for the surface of the AlGaN after the p-GaN etch. Hence, the surface morphology of the AlGaN layer after the plasma etch was not significantly degraded (in terms of roughness) with respect to the morphology of the p-GaN.

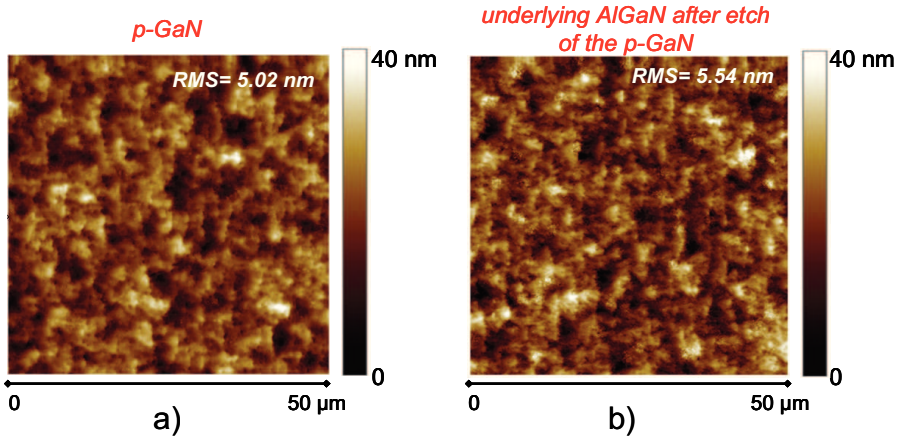

Fig. 5.3: *AFM images of the p-GaN surface (a)and the underlying AlGaN surface (b) after the p-GaN etch.*

Furthermore, TEM analysis has been carried out on one of the devices, at the edge of the gate region (see *Fig. 5.4*). The cross section TEM image shows as the p-GaN was completely etched in the desired area, while the AlGaN thickness was almost unaffected by the process.

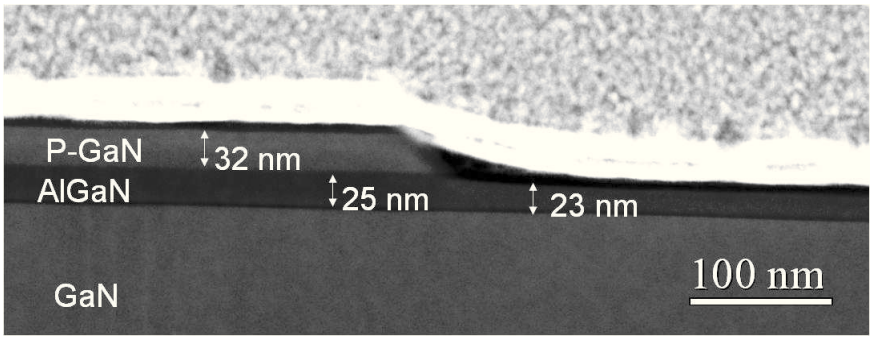

Fig. 5.4: *Bright field TEM micrographs in cross section for a p-GaN/AlGaN/GaN devices acquired at edge of the gate region.*

As first step, in order to evaluate the impact of the p-GaN cap layer on the AlGaN/GaN heterostructure, very simple test structures were fabricated. These HEMT-like structures consisted of two rectangular Ti/Al/Ni/Au source-drain contacts fabricated on the etched regions. Between the two contacts, a rectangular p-GaN unetched "finger" was left. As a reference, a test structure without the p-GaN was also fabricated. The test structure were isolated by trenches obtained by plasma etching. *Fig. 5.5* reports the pictures and the relative cross section for both structures with and without the p-GaN region in between.

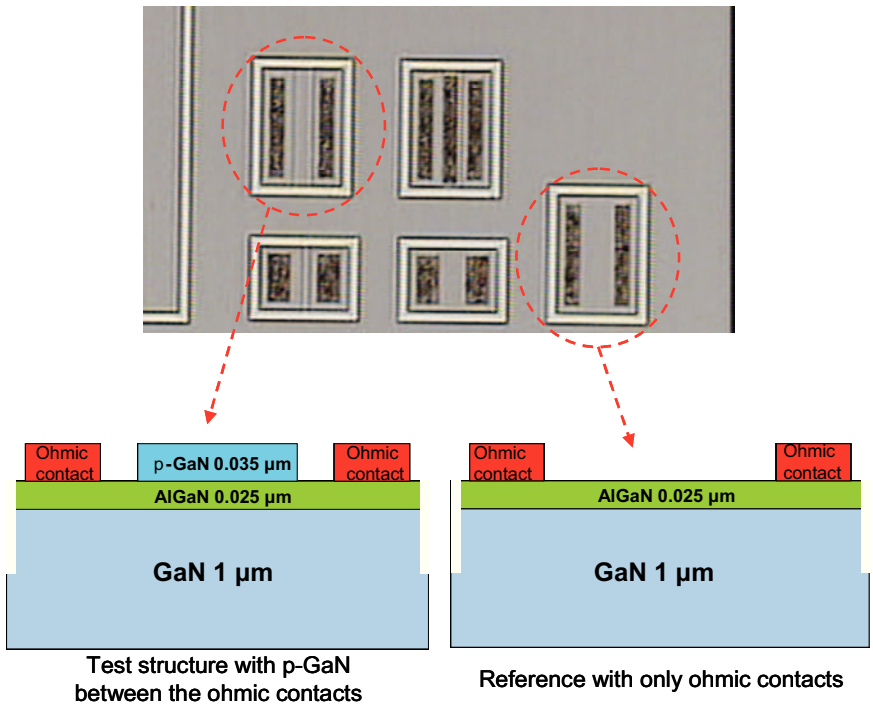

Fig. 5.5: *Picture and schematic cross section of the test structures with and without the p-GaN region between the Ohmic contacts.*

A quick electrical evaluation of these test structures showed the effect of the p-GaN in the depletion of the 2DEG. In particular, three different current-voltage measurements were carried out: (1) on the reference structure without p-GaN; (2) on the structure with p-GaN "floating"; (3) on the structure with p-GaN contacted with a third probe put at V= 0 V. As can be see from *Fig. 5.6*, the presence of a the p-GaN leads to a reduction of the current flowing between source and drain (in the 2DEG) with respect to the reference structure. The drain current is further reduced when the p-GaN gate is contacted with a third probe put at V= 0 V.

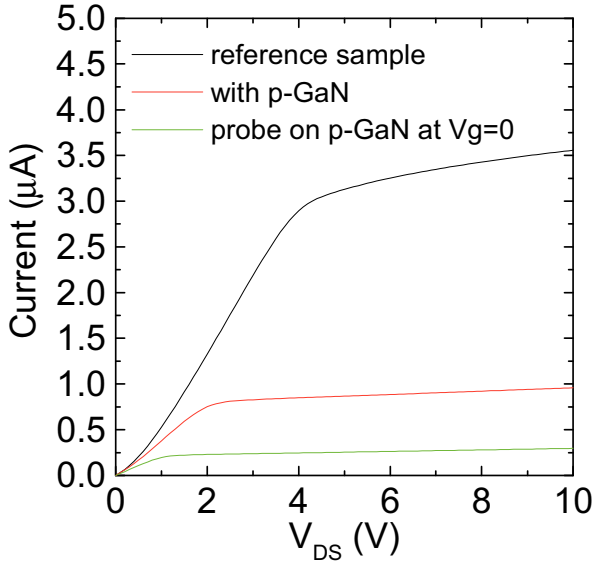

Fig. 5.6: *I-V characteristics for test structure fabricated with and without the p-GaN cap layer in between the two Ohmic contacts*

After that, field effect transistors (FETs) were fabricated and characterized. In these structures, the source and drain Ohmic contacts was formed using a Ti/Al/Ni/Au metal stack annealed at 800 °C. As a gate contact, either Ti/Al/Ni/Au annealed at 800 °C or in Ni/Au annealed at 400 °C has been used. A schematic with the cross section and the top view of the fabricated HEMTs is showed on *Fig. 5.7*. Such a HEMT-like structures with non-critical dimensions are sometimes called FAT-FETs and are a useful tool to determine the properties of the 2DEG like carrier concentration and mobility [189].

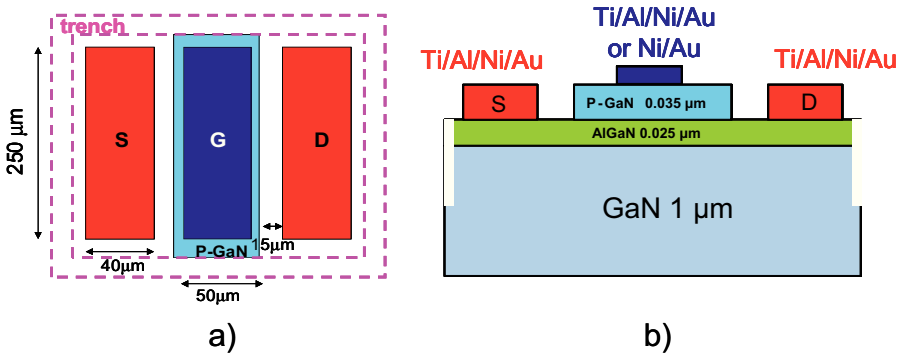

Fig. 5.7:: *Top view (a) and cross section of the fabricated HEMTs.*

First the quality of the source and drain contacts fabricated on the regions where the p-GaN was evaluated using TLM structures. The I-V characteristics acquired on TLM structures and the plot of the total resistance as a function of the pad distance are shown in *Fig. 5.8*.

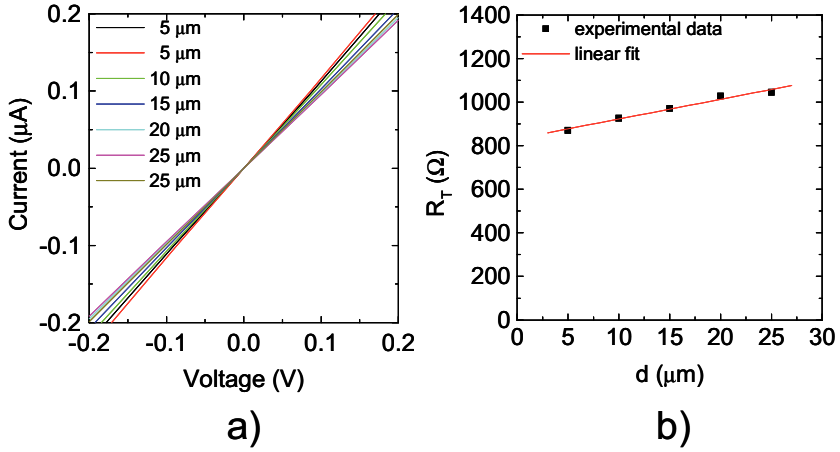

Fig. 5.8: *I-V characteristics for a TLM structures of Ti/Al/Ni/Au contacts, annealed at 800°C, fabricated on the etched region (a) and plot of the total resistance as function of the TLM pad distance (b). The linear fit of the R_T is also reported in the graph.*

From the TLM analysis a specific contact resistance of 1.3×10^{-3} Ω·cm^2 and a sheet resistance of 1600 Ω/sq were obtained. Typical values of the sheet resistance and of the specific contact resistance in AlGaN/GaN heterostructures are in the order of 600 Ω/sq and 10^{-4}-10^{-5} Ω·cm^2, respectively. Clearly, the plasma etch process performed on the sample surface induced a degradation of the material properties, which in turn resulted in an increase of the specific contact resistance of the Ohmic contact fabricated on it. The optimization of this etching process in order to preserve the AlGaN properties and achieve good Ohmic contact is still under investigation.

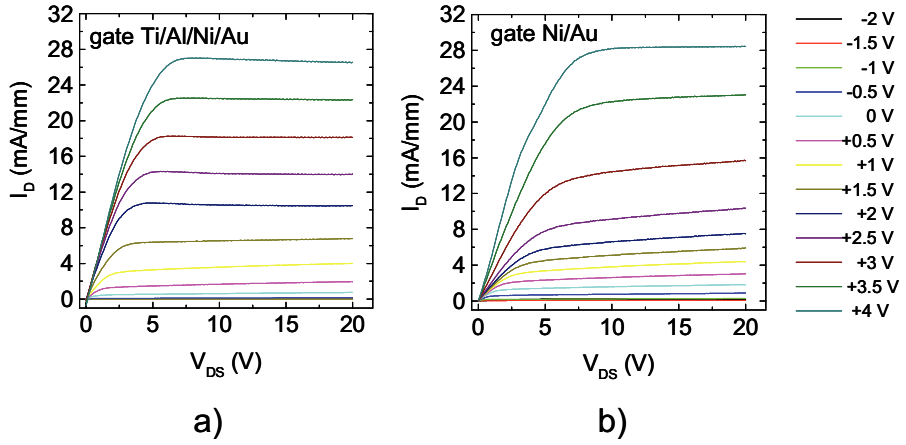

Fig. 5.9: *Electrical characteristics of p-GaN/AlGaN/GaN HEMTs fabricated with Ti/Al/Ni/Au (a) and Ni/Au (b) gate contact.*

Then, the HEMT structures (schematically described in *Fig. 5.7*) were characterized by current-voltage (I-V) measurements. *Fig. 5.9* reports the drain current as a function of the drain bias for two representative HEMT structures (representative of the average behaviour of several measured devices) having two different metal gate electrodes on the p-GaN, i.e. Ti/Al/Ni/Au and Ni/Au. The source and drain Ohmic contacts were Ti/Al/Ni/Au in both case. The V_{DS} was varied in a range between 0 and +20 V, while the gate voltage V_{GS} has been changed at step of 0.5 V from -2 V to +4 V. Similar electrical characteristics and similar values of the saturation

drain current were measured in the two cases (about 7 mA at gate voltage of +4 V). From this measurements, it is already possible to note that at V_{GS} = 0 V, the device show a drain current about +0.2 mA and +0.4 mA, respectively for the Ti/Al/Ni/Au and the Ni/Au gate device, i.e., indicating a normally-on behaviour.

Fig. 5.10 shows the transcharacteristics for the Ti/Al/Ni/Au and the Ni/Au gate device, i.e. the drain current, taken for V_{DS} = +15V, as function of the gate voltage. The gate voltage has been changed at step of 0.5 V from -2 V to +4 V. Both metals shows a similar behaviour.

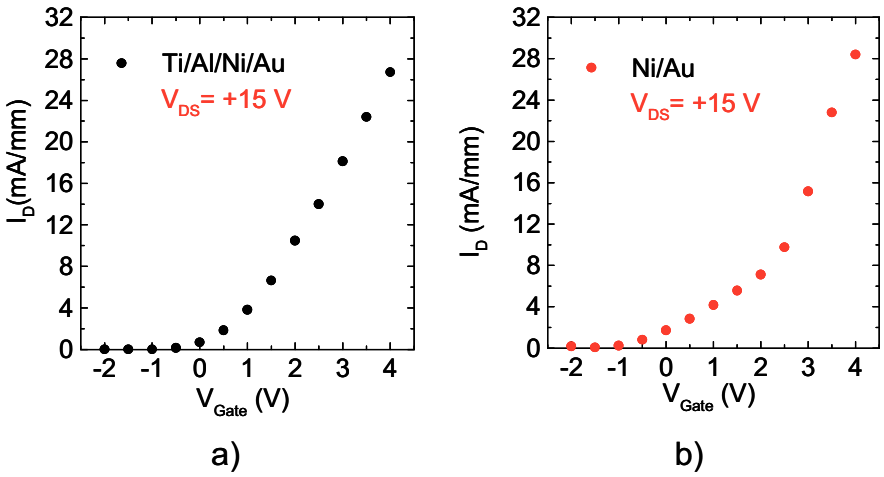

Fig. 5.10: *Transcharacteristics of the HEMTs fabricated with Ti/Al/Ni/Au (a) and Ni/Au (b) gate contact.*

The I-V characteristics of the gate-source diode were acquired in the two cases in order to monitor the influence of the different metal gate on the gate leakage current. These characteristics are reported in *Fig. 5.11*. Evidently, a lower current (both under forward and reverse bias) was measured in the devices with the Ni/Au gate contact with respect to those with the Ti/Al/Ni/Au gate.

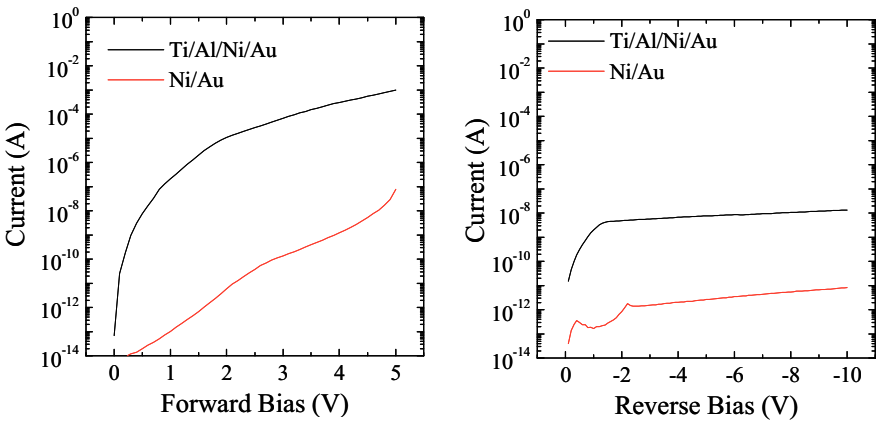

Fig. 5.11: *Forward (a) and reverse (b) characteristics of the gate-source diode in the Ti/Al/Ni/Au and Ni/Au gate HEMTs.*

To clarify the reason of this different behaviour, voltage-stress measurements were carried out on the Schottky diodes fabricated in the same wafer with the two different metal gate (Ni/Au or Ti/Al/Ni/Au). In these measurements, the forward characteristics a diode were acquired by sweeping the bias from V=0 to a different maximum value, i.e., from 2 to 10 V. The characteristics of the diode fabricated with the Ti/Al/Ni/Au gate were not affected by the voltage stress, and are not reported here. On the other hand, a different situation was found in the case of the Ni/Au gate. As can be seen in *Fig. 5.12*, the characteristics were unchanged when the maximum applied forward bias was kept below 7 V. However, at higher bias value, a strong increase of the current was detected. When the same measurement was repeated after this stress cycle, an irreversible degradation of the diode behaviour occurred, with a significantly higher current in the whole bias range. The observed behaviour can be plausibly attributed to the presence of a thin residual oxide at the interface Ni/Au/p-GaN, that locally breaks upon stress at high values of the bias. This scenario also explains the lower forward and reverse gate current in the case of Ni/Au gate device shown in *Fig. 5.11*. Clearly, this phenomenon was absent in the Ti/Al/Ni/Au gate

device, where the thermal reaction occurring between the metal and the GaN probably effectively remove any interfacial contaminant [190].

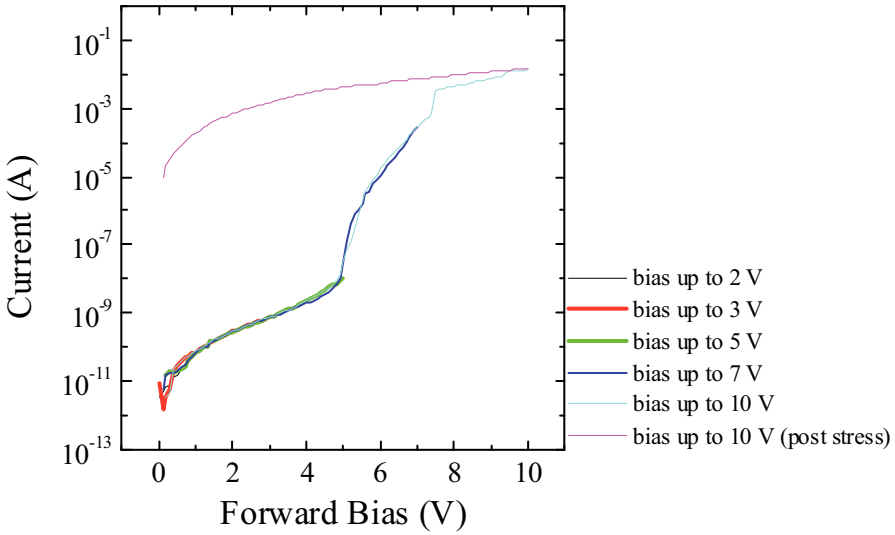

Fig. 5.12: *Voltage stress measurements conducted in Ni/Au gate device.*

In order to determine the sheet carrier concentration of the 2DEG channel and the threshold voltage, capacitance-voltage (C-V) measurements were carried out in the fabricated HEMTs. Comparative C-V measurements carried out in the reference AlGaN/GaN heterostructure (i.e. without p-GaN) just after material growth are also reported. In this case mercury probe analysis was used [191] to extract the C-V curve.

The C-V measurements show a great difference between the reference heterostructure (AlGaN/GaN) and the structure with the p-GaN cap layer (p-GaN/AlGaN/GaN) (see *Fig. 5.13a*). Clearly, lower capacitance values were measured in the devices with the p-GaN cap, thus being an indication of a reduction of the 2DEG charge density. Furthermore, the pinch-off (i.e., where the C-V curves fall due to the depletion of the 2DEG) occurs at less negative gate bias, as can be deduced from a shift of about 4 Volts of the curves with respect to the reference.

From the C-V curves, the sheet carrier concentration n_s and the threshold voltage V_{th} were determined (as explained in chapter 2). It should be noted that, as expected from the measures on test structures (*Fig. 5.6*), a reduction of the sheet carrier concentration is measured in the device with the p-GaN layer under the gate. In fact, at gate voltage of 0 V, if a n_s of 7.41×10^{12} cm^{-2} was found in the reference sample, the devices using p-GaN gate contact result in a lower value of 1.32×10^{12} cm^{-2} for the Ti/Al/Ni/Au and 9.31×10^{11} cm^{-2} for the Ni/Au gate device.

From the plots of the sheet carrier density n_S as a function of the gate bias V_g (see *Fig. 5.13b*) it was possible to quantify the positive threshold voltage shift obtained using the p-GaN cap.

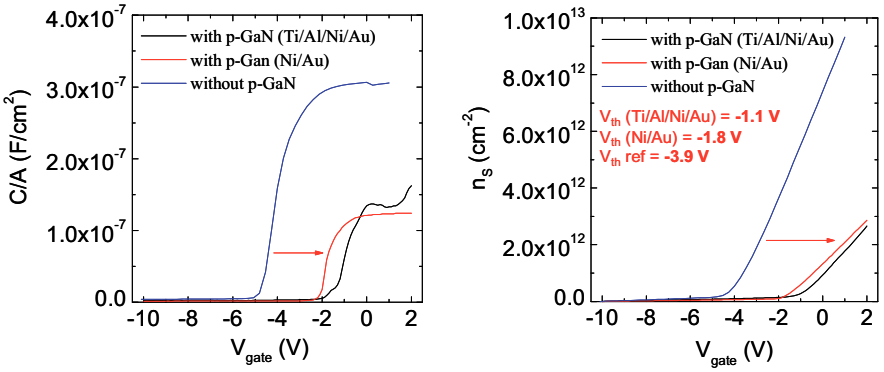

Fig. 5.13: *Capacitance-voltage measurements (a) and sheet carrier concentrations (b) as function of the gate bias for HEMTs fabricated without p-GaN and with p-GaN under Ti/Al/Ni/Au or Ni/Au gate contact.*

In particular, the threshold voltage increased from the value of V_{th} = -3.9 V in the reference heterostructure to -1.1 V in the heterostructure with p-GaN and Ti/Al/Ni/Au gate. A slightly different value of Vth = -1.8V was found when using the Ni/Au gate, most probably due to the presence of residual oxide in the interface, as discussed before. Even if a normally-on behaviour is still observed, the large positive threshold voltage shift obtained

using the p-GaN cap layer under the gate contact makes this approach very promising for the fabrication of enhancement mode HEMTs.

In order to further increase the value of V_{th}, simulations of the band structures in different heterostructures have been carried out and will be described in the paragraph 5.4.

5.3 Development of a “self-aligned” process for the gate of a p-GaN/AlGaN/GaN HEMT

The results shown in the previous paragraph were obtained by defining the p-GaN gate region using a patterned SiO_2 hard mask during plasma etch and, then, employing another aligned photolithography step for the definition of the metal gate on the top of the p-GaN (see *Table 5.1*).
However, this approach can be good for FAT-FETs test pattern but is unpractical for the fabrication of devices with critical source-to-drain distances.

In order to overcome this inconvenience, during this work of thesis a “self-aligned” process for the p-GaN gate has been developed. This process consists in using directly the patterned metal gate (e.g, a Ti/Al bilayer) as a hard mask for the plasma etch of the p-GaN layer. The metal gate is patterned by lift-off technique with the following procedure, showed in *Fig. 5.14*: (1) Photolithography of the desired pattern on the photoresist; (2) Deposition of a Ti/Al metal layer; (3) Lift-off of the photoresist by wet etch in solvents.

Clearly, in this way, only one lithography step is required, without the need of critical alignment, with a significant simplification of the fabrication flow-chart of the devices and test patterns. Similarly, also the Ti/Al/Ni/Au Ohmic contacts (for source and drain) can be defined using the lift-off

technique, i.e. avoiding the use of the complex sequential etch procedure (see step 12 in *Table 5.1*)

The main steps of the fabrication flow chart of the devices using the self-aligned p-GaN gate process are described in *Table 5.2*.

1.	Cleaning of the wafer	Solution of HF:HCl:H_2O = 1:1:10
2.	Photolithography for the definition of the p-GaN and the metal gate	Resist ARP-5350
3.	Ti/Al deposition for the gate contact	Thickness of 30/120 nm
4.	Lift-off for the Ti/Al gate definition	Acetone
5.	Selective plasma etch of the p-GaN layer	Plasma selected etching in Cl_2/Ar/O_2
6.	Photolithography for the Ti/Al/Ni/Au metal definition	Resist ARP-5350
7.	Metal deposition of Ti/Al/Ni/Au	Thickness of 15/200/50/50 nm
8.	Lift-off for the Ti/Al/Ni/Au metal definition	Acetone
9.	Annealing of the Ti/Al/Ni/Au wafer	800 °C in Ar atmosphere

Table 5.2: *Schematic flow chart for the fabrication of HEMTs with gate contact using a self aligned process.*

Obviously, this approach requires that the fabrication of the metal gate is done before that of the source-drain Ohmic contacts (*gate-first* approach). Consequently, the self-aligned metal gate will be subjected the

thermal budged for Ohmic contact formation (typically around 800°C when using a Ti/Al/Ni/Au stack). *Fig. 5.15* shows a cross section TEM analysis of the gate region obtained with the self-aligned process described before.

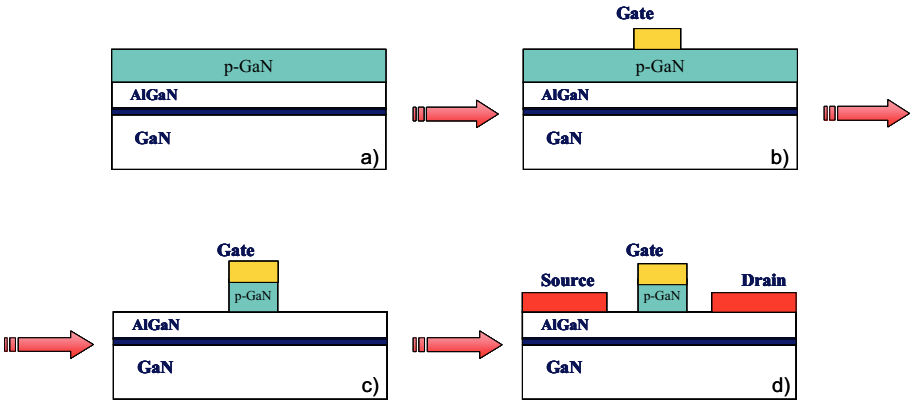

Fig. 5.14: *Illustration of the main steps for the fabrication of HEMTs with a p-GaN gate contact using a self aligned process.*

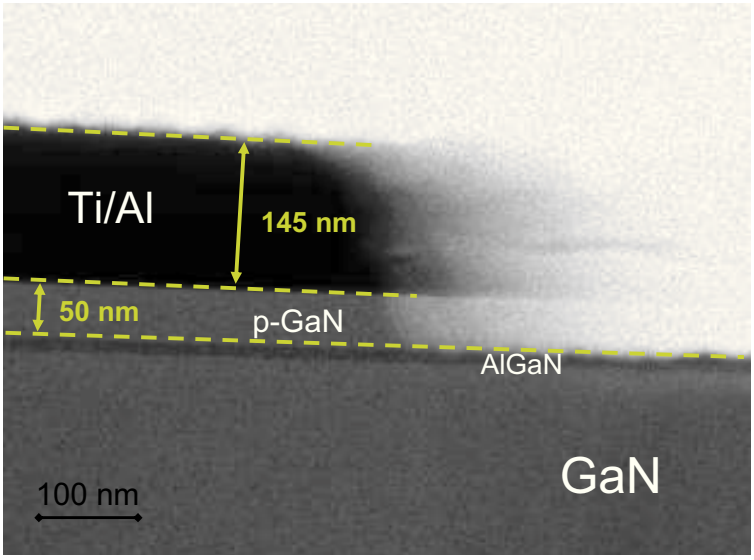

Fig. 5.15: *Bright field TEM micrograph in cross section of a p-GaN/AlGaN/GaN heterostructure patterned with a Ti/Al self-aligned gate.*

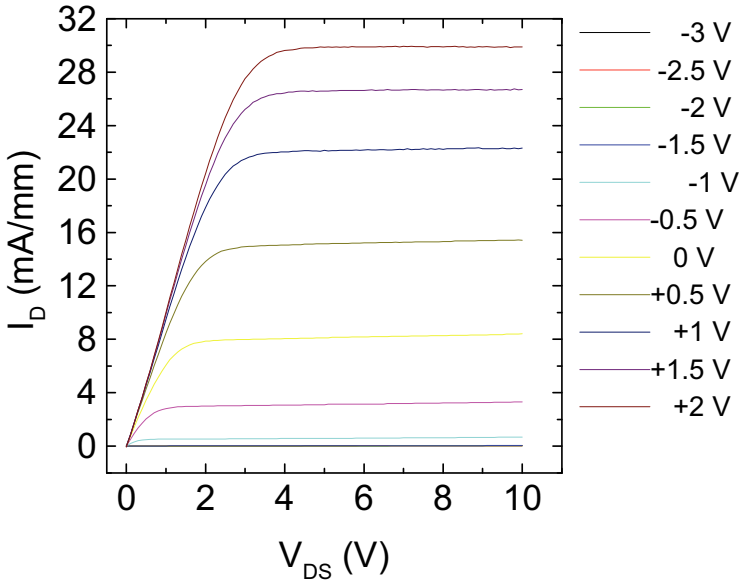

Fig. 5.16: *Output characteristics of HEMTs fabricated by self-aligned process.*

This process was tested on a new p-GaN/AlGaN/GaN heterostructure grown onto 150 mm Si(111) wafer, similar to that schematically described in *Fig. 5.1a* (the only difference was the thickness of the p-GaN layer, i.e. 50 nm in this case). The test patterns were characterized by I-V measurements and a good transistor behaviour was observed (see *Fig. 5.16*). Also in this case, the threshold voltage extracted from the electrical data was around -1V.

5.4 Simulations of the band diagram of p-GaN/AlGaN/GaN heterostructures

From the electrical characterization illustrated in the previous paragraph, a considerable positive shift of the threshold voltage has been demonstrated when using a p-GaN cap onto an AlGaN/GaN heterostructure. Anyway, the characterized p-GaN/AlGaN/GaN heterostructures (35 nm Mg-doped p-GaN with 10^{17} cm^{-3} hole concentrations and 15 nm of AlGaN with an Al concentration of 26 %) showed still a negative value of V_{th} (-1.1 V). To obtain a positive threshold voltage an optimization of the entire heterostructure is required, that can be possible with the help of simulations of the band diagrams of the p-GaN/AlGaN/GaN systems.

The equation that describes the threshold voltage V_{th} has been already reported on the chapter 2:

$$V_{th} = \Phi_B - \Delta E_C - \frac{qN_{D_{AlGaN}} d^2_{AlGaN}}{2\varepsilon_0 \varepsilon_{AlGaN}} - \frac{\sigma}{\varepsilon} d_{AlGaN} \qquad \text{(Eq. 5.1)}$$

While for a conventional AlGaN/GaN heterostructure Φ_B represented the metal-gate/AlGaN Schottky barrier height, in the presence of a p-GaN cap Φ_B in Eq. 5.1 is the energy difference between conduction band minimum and Fermi level of p-GaN [192]. Evidently, considering the Eq. 4.1, the parameters that strongly affect the threshold voltage are Φ_B, σ and the thickness d of the AlGaN. Φ_B depends on the epitaxial proprieties of the p-GaN, while σ depends on the proprieties of the AlGaN layer (like the thickness and the Al molar fraction in the alloy).

Hence, in order to obtain the desired positive threshold voltage, it is necessary to change the properties of both the p-GaN or the AlGaN layer. Hence, the following parameters in the heterostructure can be changed:

- The thickness and the Mg concentration in the p-GaN layer
- The thickness and the Al concentration in the AlGaN layer

In fact the properties of the p-GaN layer (in terms of Mg concentration) will determine the value of Φ_B, while the properties of the AlGaN layer will directly act on the value of the sheet carrier density n_S (see chapter 2).

To better understand how the p-GaN/AlGaN/GaN heterostructure can be optimized in order to efficiently deplete the 2DEG and obtain a normally-off HEMT, the band structures of different heterostructures were simulated using the commercial simulator SILVACO [193]. These simulation have been performed in STMicroelectronics of Catania, Italy.

Basically, SILVACO solves the Poisson equation including the contribution of the mobile and fixed charges, the contributions of the ionized traps, the carrier continuity equations for electrons and holes, and the transport equations using the drift-diffusion model. The built-in fields due to spontaneous polarization and strain (piezoelectric effect) are taken into account as fixed sheet charges at the AlGaN surface and AlGaN/GaN interface. A positive sheet charge $+\sigma_{pol}$ was defined at the interface, and the equivalent negative sheet charge $-\sigma_{pol}$ was defined at the AlGaN surface. Newton numerical method was used in the models for calculations. It consists in a numerical method used to find successively better approximations to the roots of real-valued function. Thus, starting from the three-dimensional structure (1 μm depth), by conducting a "cut-line" perpendicular to the interface, it is possible to extract the band diagram and the dependence of the carrier density as a function of the depth.

As described in chapter 2 (see for example *Fig. 2.17*), the physical condition to have a normally-off behaviour in the heterostructure is that the bottom of the conduction band is located above the Fermi level. Under this condition, no permitted energy levels in the triangular well below the Fermi level are available for the electrons in the conduction band. Clearly, in this condition an extremely low sheet concentration of electrons can be found at the interface (i.e., lower than 10^9 cm^{-2}).

First of all, an AlGaN/GaN heterostructure without p-GaN capping layer has been simulated as a reference. Using a thickness of the AlGaN layer of 25 nm and a Al concentration of 26 %, a sheet carrier density of the 2DEG of $n_S = 9.4\times10^{12}$ cm^{-2} has been obtained. This result is in agreement with the

experimental data (reported in the paragraph 5.2, *Fig. 5.13*). The corresponding band diagram is reported in *Fig. 5.17*.

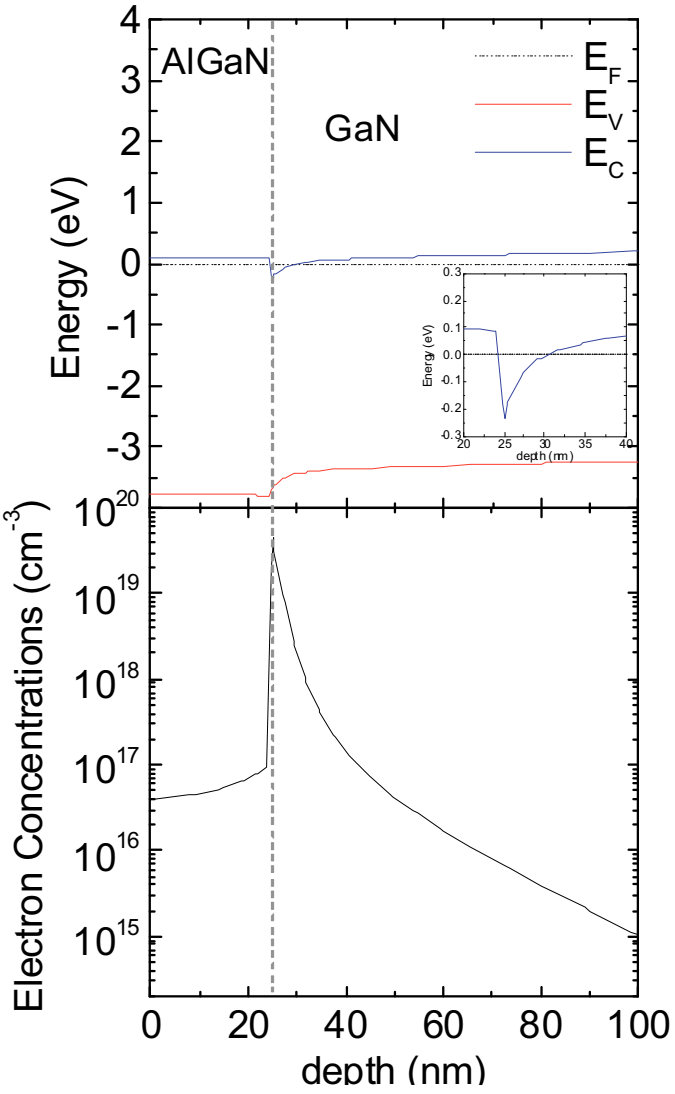

Fig. 5.17: *Band diagram and electron concentration simulated for an AlGaN/GaN heterostructure, with 25 nm thick AlGaN layer with an Al concentration of 26 %.*

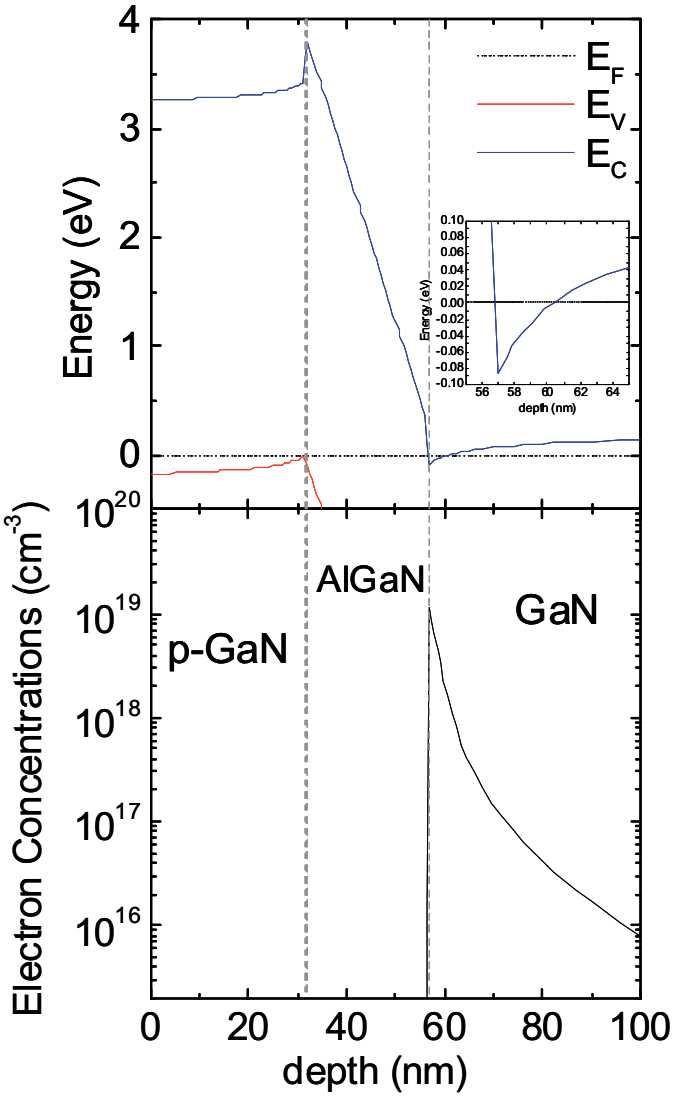

Fig. 5.18: *Band diagram and electron concentration simulated for a p-GaN/AlGaN/GaN heterostructure, with a 32 nm thick p-GaN (10^{17} holes/cm^3), and a 25 nm thick AlGaN layer with Al concentration of 26 %.*

Then a p-GaN cap was added to the AlGaN/GaN system. In particular, the thickness of p-GaN (32 nm) and of AlGaN (25 nm), determined experimentally by cross section TEM analysis (see *Fig. 5.4*) , were used for the simulation. The hole concentration in the p-GaN layer (10^{17} cm^{-3}) has been extracted using experimental data of Secondary Ion Mass Spectrometry (SIMS) analysis and using the activation energy reported in literature [71,194]. The Al concentration in the AlGaN was determined by photoluminescence (PL) measurements after material growth. The simulated band diagram for this heterostructure is reported in *Fig. 5.18*. As can be seen, also in this case the conduction band edge lies still under the Fermi level, thus confirming the presence of the 2DEG. However, the presence of the p-GaN cap slightly modified the properties of the 2DEG, since the sheet carrier density decreased up to 3×10^{12} cm^{-2}. This value is in agreement with the experimental results achieved by the C-V measurements (see *Fig. 5.13*).

As mentioned above, the layers that play a fundamental role in the value of the threshold voltage are the p-GaN and the AlGaN. Hence, several other structures were simulated by changing the properties of the p-GaN (thickness or holes concentration) and of the AlGaN (thickness and Al concentration). A summary of these simulations is reported in *Table 5.3*

Among all the simulated structures, the case of an AlGaN thickness of 15 nm with an Al concentration of 20 % leaving unchanged the p-GaN proprieties **(**35 nm and 10^{17} holes/cm^3), seemed to be the most promising one to obtain a normally-off behaviour.. The extracted band diagram (reported in *Fig. 5.19*) shows, in fact, that the conduction band that above the Fermi level and the sheet carrier concentration is strongly reduced.

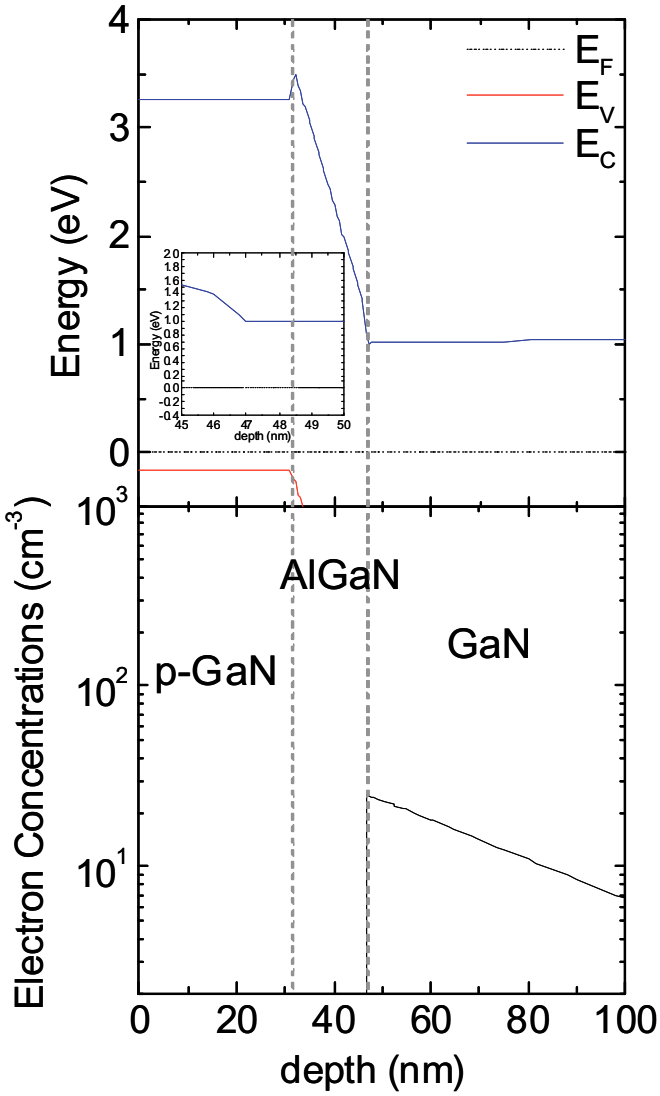

Fig. 5.19: *Band diagram and electron concentration simulated for a p-GaN/AlGaN/GaN heterostructure, with a 32 nm thick p-GaN (10^{17} holes/cm^3) and a 15 nm thick AlGaN layer with an Al concentration of 20 %.*

	p-GaN thickness	*p-GaN (cm^{-3})*	*AlGaN thickness*	*Aluminium concentration*	*2DEG n_S*
#1	-	-	25 nm	26 %	9.4×10^{12} cm^{-2}
#2	32 nm	10^{17} cm^{-3}	25 nm	26 %	3.0×10^{12} cm^{-2}
#3	150 nm	10^{19} cm^{-3}	25 nm	26 %	3.0×10^{12} cm^{-2}
#4	32 nm	10^{17} cm^{-3}	25 nm	20 %	5.8×10^{11} cm^{-2}
#5	32 nm	10^{17} cm^{-3}	15 nm	26 %	2.0×10^{8} cm^{-2}
#6	32 nm	10^{17} cm^{-3}	15 nm	20 %	no 2DEG

Table 5.3: *Summary of the simulation carried out on p-GaN/AlGaN/GaN heterostructures with different characteristics.*

Basing on these simulation, it is clear that combining a reduction of the AlGaN thickness with a lowering of the Al concentration, is the way to obtain an efficient depletion of the 2DEG by the p-GaN gate and, ultimately, to fabricate a normally-off HEMT device.

Similar considerations were reported by Hilt et al. [195], that proposed an optimized heterostructure using a thin AlGaN barrier layer (15 nm) with an Al concentration of 23%. In addiction, Hilt et al. proposed the use of an AlGaN buffer layer with an Al concentration of 5% under the thin layer of GaN (10 nm). The use of back-barrier of AlGaN is useful to obtain a higher electron density in the channel and a more positive potential well at the gate position [195]. This aspect is not explored in this work of thesis as it would require a dedicate study.

In the next paragraph, it will be shown that a normally-off behaviour can be actually obtained using a more suitable p-GaN/AlGaN/GaN heterostructure, as defined by the simulations.

5.5 Normally-off behavior of p-GaN/AlGaN/GaN HEMT structures

Following the simulation results, in order to obtain the complete depletion of the 2DEG using the p-GaN gate, new p-GaN/AlGaN/GaN structures were grown onto 50 mm sapphire substrates at the Institute of High Pressure Physics (UNIPRESS) of Warsaw, Poland.

Fig. 5.20 shows a schematic cross section of the two different heterostructures used for this experiment. The main differences between the two heterostructures consist on the specifications of the AlGaN barrier layer, i.e. in the thickness and the Al concentration. In particular, the sample A had an AlGaN thickness of 31.8 nm, with an Al concentration of 32%. The sample B had a thinner AlGaN layer (18.7 nm) with a lower Al concentration (20%). Clearly, the sample B should be more suitable for normally-off behavior, according to the simulations.

On these samples, different devices and test patterns were fabricated. A picture of one of the processed wafers is shown in *Fig. 5.21*

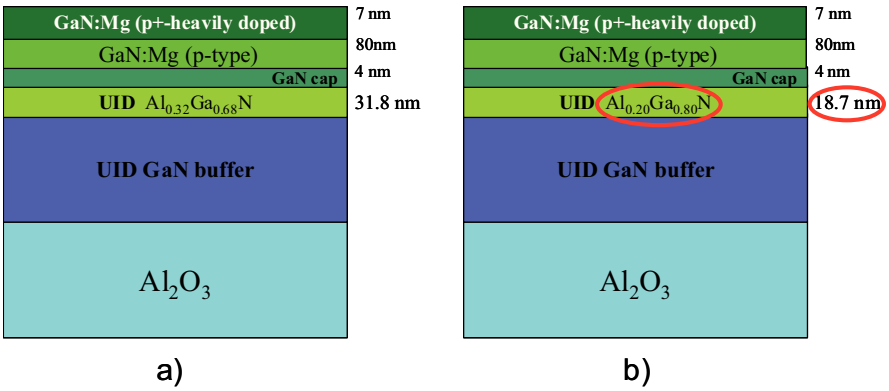

Fig. 5.20: *Schematic cross section of the p-GaN/AlGaN/GaN heterostructures grown on sapphire by UNIPRESS.*

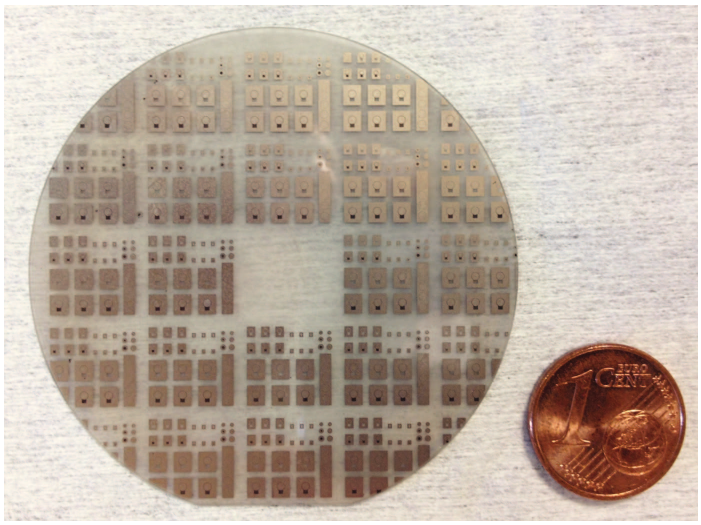

Fig. 5.21: *Picture of the processed 50mm wafer.*

In this case, simple round-HEMTs were fabricated (instead of the linear FATFETs) in order to strongly simplify the fabrication flow, avoiding the use of trenches or ion-implantation for the isolation of the 2DEG. Indeed, round-HEMT consists of a drain contact placed inside the gate ring and a source metallisation that encloses completely the gate [196]. As an example, a picture of a round HEMT fabricated on AlGaN/GaN heterostructures grown on Al_2O_3 substrates is shown in *Fig. 5.22*.

The use of round HEMTs is particularly advantageous when a quick evaluation of the properties of the 2DEG is required to optimize the condition of growth of the heterostructure [197]. On the same wafers, other test structures like diodes and TLM patterns were also fabricated.

The p-GaN gate was first defined using a Ti/Al hard mask, employing the self-aligned process illustrated in paragraph 5.3. After definition of the gate region, Ohmic contacts were defined in the etched region by photolithography and lift-off of a Ti/Al/Ni/Au stack. Finally, a rapid annealing at 800°C in Ar was used to obtain linear I-V characteristics of the contacts.

Fig. 5.22: *Picture of a fabricated round HEMT on AlGaN/GaN heterostructures on Al_2O_3 substrates.*

First of all, C-V measurements were carried out on the p-GaN/AlGaN/GaN diodes, in order to estimate the value of the threshold voltage obtained using this new heterostructure. *Fig. 5.23a* shows the C-V measurements obtained on the diodes fabricated on the sample A and on the sample B. As can be seen, a significant shift of the C-V curves toward more positive bias is observed in sample B with respect to sample A. The values of the sheet carrier density extracted by integration of the C-V curves are reported in *Fig. 5.23b.* From the extrapolation of the ns curves at V_g= 0 it was possible to determine the values of V_{th}= -3.1 V for the sample A (32 nm $Al_{0.32}Ga_{0.68}N$) and of V_{th}= +1.4 V for the sample B (18 nm $Al_{0.2}Ga_{0.8}N$). This result demonstrates the normally-off behaviour of the sample B, as predicted by the simulations of the band structures presented in paragraph 4.4. Furthermore, a strong reduction of the sheet carrier contration occurs in sample B, from 3.47×10^{12} to 1.98×10^{11} cm^{-2} at V_g= 0 V.

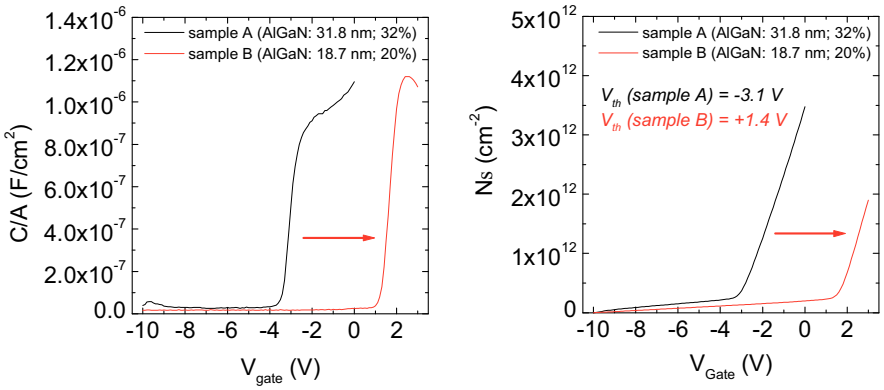

Fig. 5.23: *C-V measurements (a) and the extracted n_S (b) as function of the voltage gate*

The complete depletion of the 2DEG (normally-off behaviour) of the structure B, with a thinner layer of AlGaN and a lower Al concentration, was confirmed by the electrical characteristic of the round-HEMTs shown in *Fig. 5.24*. The output characteristics show a drain current around 15 mA at V_{DS}= +5 V and V_g= +4 V. Already at gate voltage of +1.5 V, the drain current is strongly reduced at value of 2 mA for V_{DS}= +5 V. However, a good pinch-off condition is not achieved, since a significant drain current is measured even upon a further decrease of the gate bias.

In fact, from transcharacteristics I_D-V_G taken at V_{DS}= +5 V (see *Fig. 5.25*) it is possible to observe that a high leakage current (2 mA) persists even with increasing negative gate bias values (V_{DS}=-5V).

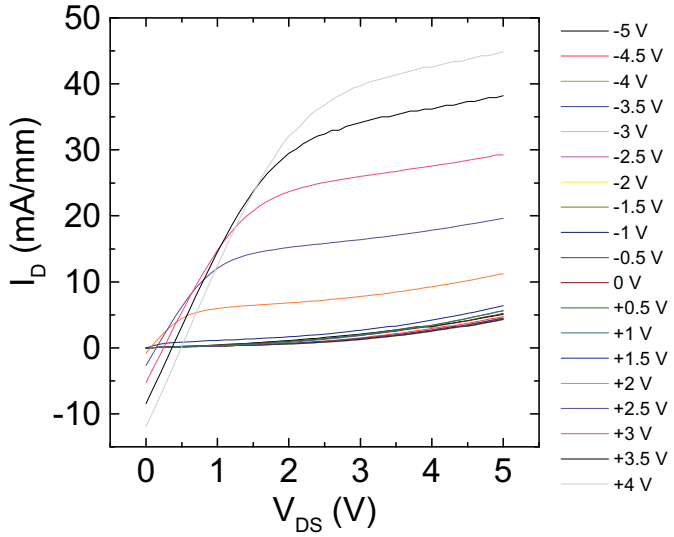

Fig. 5.24: *I_D-V_D characteristics of the normally-off HEMTs (sample B).*

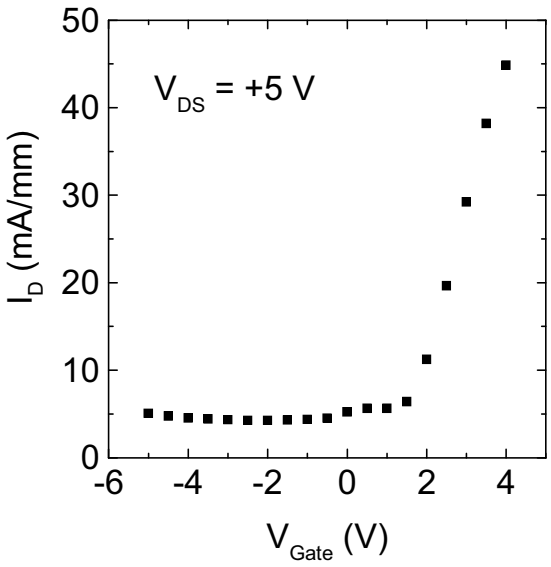

Fig. 5.25: *Transcharacteristics of the normally-off HEMTs (sample B).*

Moreover, as can be seen from the HEMT characteristics in *Fig. 5.24*, when the gate bias exceeds +2 V, negative values of the current are measured at low drain bias. This latter is due to a current flowing between gate and source to gate leakage current, due to the turn-on of the diode.

The forward and reverse I-V characteristics of the gate-source diode are reported in *Fig. 5.26*. The forward characteristic of the gate-source diode show a significant increase of the current when the diode turns on, i.e. in the bias range between 1 and 2 V. On the other hand, the diode under reverse bias has a low leakage current, i.e. in the order of 10^{-6} A at -5V, thus suggesting that the poor pinch-off behaviour cannot be attributed to a leakage current on the gate.

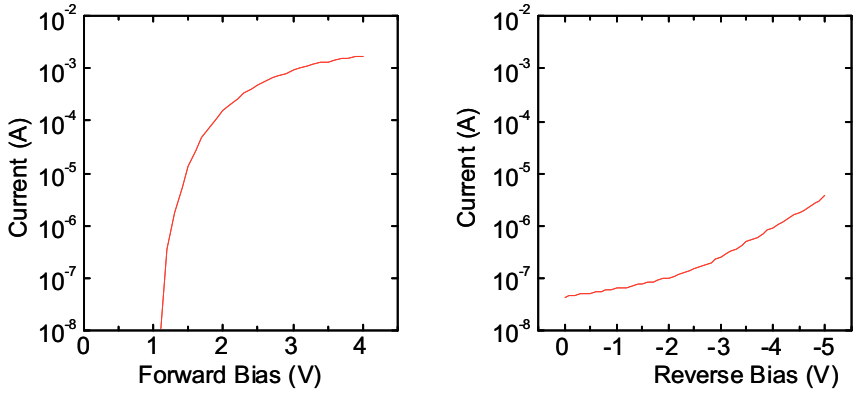

Fig. 5.26: *I-V characteristics measured on the diode gate-source of sample B.*

In order to clarify the origin of the leakage current determining the poor pinch-off condition of the HEMTs, a simple test pattern was fabricated (see *Fig. 5.27*). The test pattern consisted of two Ohmic contacts isolated by a 70 nm deep trench (i.e., completely cutting the 2DEG). The trench was created by plasma etch in CHF_3 plasma; the Ohmic contacts were placed at distance of 25 μm. The current flowing between the two Ohmic contacts is reported in *Fig. 5.28*. As can be seen, although the 2DEG was interrupted by the trench, a large current is measured between the pads, up to 8 mA at 10 V.

This results clearly indicate that there is a high leakage contribution coming from the GaN substrate.

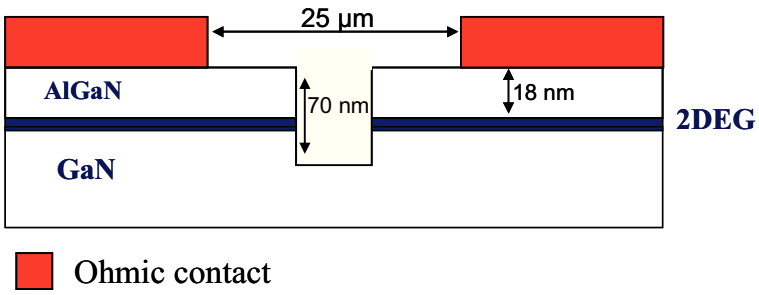

Fig. 5.27: *Schematic cross section of the test structure used for the identification of the the leakage current.*

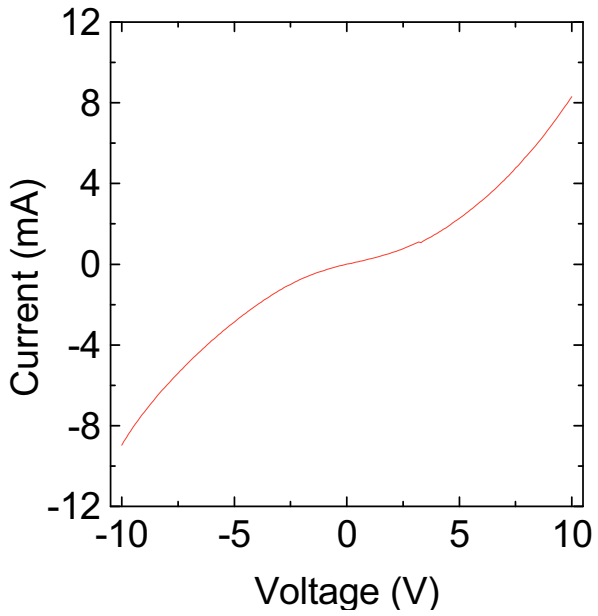

Fig. 5.28: *Current-Voltage measurement on test structure for the leakage current.*

Basing on this result, it is clear that the I-V characteristics of the transistors shown in *Fig. 5.24* are strongly affected by the presence of this leakage current, hindering the complete pinch-off condition of the device. The contribution of the leakage current, normalized for the device geometry, has been subtracted to the experimental curves in *Fig. 5.29*.

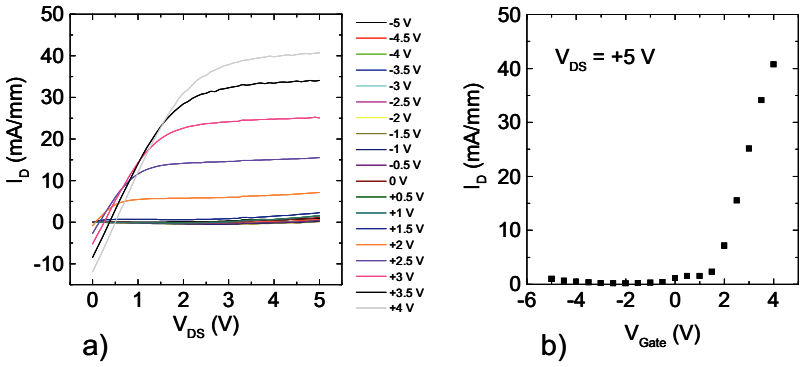

Fig. 5.29: *I_D-V_{DS} characteristics (a) and the transcharacteristics (b) of the normally-off HEMT (sample B) after subtraction of the leakage current.*

The corrected characteristics and the corrected transcharacteristics are shown in *Fig. 5.29a* and in *Fig. 5.29b*. Obviously, even if a better pinch-off condition is obtained, the source to gate leakage contribution occurring at low values of V_{DS} is not eliminated by this correction. If fact, this leakage current is a common problem for normally-off HEMT technology using p-GaN, since the increase of the gate bias needed to drive the HEMT will unavoidably turn on the p-GaN/AlGaN diode. In this case, the use of an insulator layer under the metal contact can lead to an improvement of the device characteristics, both in terms of leakage current and of threshold voltage [53].

Chapter 6: Epitaxial nickel oxide on AlGaN/GaN heterostructures

This chapter reports a preliminary study on nickel oxide as a dielectric below the Schottky gate contact in AlGaN/GaN heterostructures. In fact, as pointed out in some parts in this thesis, the use of a gate dielectric is an important approach to limit the leakage current in HEMTs devices. The first results reported in the following paragraphs can be an input for future research activities.

6.1 Gate dielectrics in GaN HEMTs

As we have seen in the previous chapters, a Schottky contact is typically used to form the gate electrode in AlGaN/GaN HEMTs. However, the device operation can be affected by a high gate leakage current, limiting both the off-state performance, as well as the gate voltage swing (i.e., the maximum on-state current). To overcome these limitations, metal-insulator-semiconductor HEMTs (MISHEMTs) can be fabricated, adding a dielectric film to insulate the Schottky electrode [198].

Different oxides (SiO_2, Al_2O_3, Ga_2O_3, HfO_2, Sc_2O_3, etc.) have been considered as gate insulators in the GaN transistor technology [115,116,117,118,119]. As a matter of the fact, in insulated gate HEMTs, the use of high-permittivity materials is preferred to limit the reduction of the gate-to-source capacitance (and, hence, of the transconductance). In this context, nickel oxide (NiO) can be a promising insulating material for GaN

devices, having a band gap of 4.0 eV and a relatively high permittivity of 11.9 [199].

Recently, NiO formed by thermal oxidation of Ni films has been proposed as the gate insulator in AlGaN/GaN HEMTs [200,201]. However, the thermal oxidation of Ni films can proceed through different stages [202,203] and can result into the formation of voids in the oxide layer [202].

On the other hand, NiO microstructure, and the resulting electronic properties, strongly depends on the material synthesis [204]. In fact, though stoichiometric NiO is an insulator with a resistivity of the order of 10^{13} Ω·cm at room temperature [205],a substoichiometric NiO grown under particular conditions has been found to behave as a p-type semiconductor [206] with a band gap energy from 3.6 to 4.0 eV [207].

Recently, it has been reported the possibility to combine a recessed gate approach with the use of a NiO layer under the recessed gate contact [185]. This method showed that the use of a NiO_x layer with p-type semiconducting properties under the gate contact can allow to achieve a normally off behaviour.

In the specific case of normally-off HEMTs using a p-GaN gate, since the threshold voltage is expected to exceed +1 V, the presence of a gate dielectric can be beneficial to avoid an excess of leakage current in the on-state due to the turn-on of the p-GaN/AlGaN diode.

As an example, Sugiyama et al. [53] reported that the use of a SiN_x layer between the metal gate and the p-GaN can lead to a decrease of the gate leakage coming from the gate electrode. In addition, it was also reported that with this system a further increase of the threshold voltage can be reached. In fact the SiN_x layer, is described as a capacitance in series with the capacitance related to the AlGaN layer. In this way, it limits the current coming from the gate, and even increases the voltage required to turn on the device (the threshold voltage).

Clearly, NiO is an interesting system that deserves to be investigated as a gate material in an HEMT structures to modulate the properties of the 2DEG. Furthermore, as described before, depending on its electronic properties, NiO can be a multifunctional material used either as insulator or, eventually, as p-type semiconductor (as an alternative to the p-GaN gate).

For that reason, in this thesis we have preliminary studied the impact of NiO as a gate dielectric material for GaN HEMT, as it will be discussed in the following paragraphs.

6.2 Characterization of epitaxial NiO as gate dielectric in AlGaN/GaN heterostructures

To study the effects of a NiO layer on the properties of the 2DEG in AlGaN/GaN heterostructures, a Schottky diode has been fabricated using a NiO layer under the Schottky contact. $AlGaN_{0.27}GaN_{0.73}$/GaN heterostructures grown onto Si(111) were used as substrates. The nominal thickness of the AlGaN barrier layer was 40nm. Prior to NiO growth, the substrates were cleaned in an HF/HCl mixture to remove the native oxide.

The samples were deposited by Metal Organic Chemical Vapor Deposition (MOCVD) at the Department of Chemical Science of the University of Catania. Nickel oxide layers were grown using $Ni(tta)_2$tmeda [(H-tta= 2-thenoyl-trifluoroacetone; tmeda= tetramethylethylendiamine)] precursor [208,209]. Depositions were carried out in a hot-wall, low pressure MOCVD reactor. High quality films were deposited using a 150 sccm argon flow as carrier gas and 200 sccm oxygen flow as reaction gas, maintaining the metallorganic precursor at 160°C, the substrate at 450°C during the deposition time (10 minutes) and the total pressure at 3-4 torr. Successively the deposited NiO film was patterned by photolithography and wet etched, to define a circular geometry for metal-insulator-semiconductor Schottky diodes (MIS-Schottky). Then, ring-shaped Ohmic contacts were formed with the Ti/Al/Ni/Au stack annealed in Ar at 850°C [133]. Finally, a Ni/Au metal electrode was defined by lift-off, onto the NiO circular islands. Conventional Schottky diodes, with the Ni/Au gate electrode [136] contacting directly the AlGaN surface, were fabricated on the same sample as a reference.

As first step a structural characterization of the deposited NiO was evaluated by XRD and TEM analysis, carrier out on the blanket samples. The XRD (see *Fig. 6.1*) showed the presence of (0001) reflections from the substrate and the only peaks related to the films were the (111) and (222) reflections. This feature was an evidence for the preferential growth of the NiO films along the [111] direction and suggested an epitaxial growth of the NiO on the AlGAaN substrate.

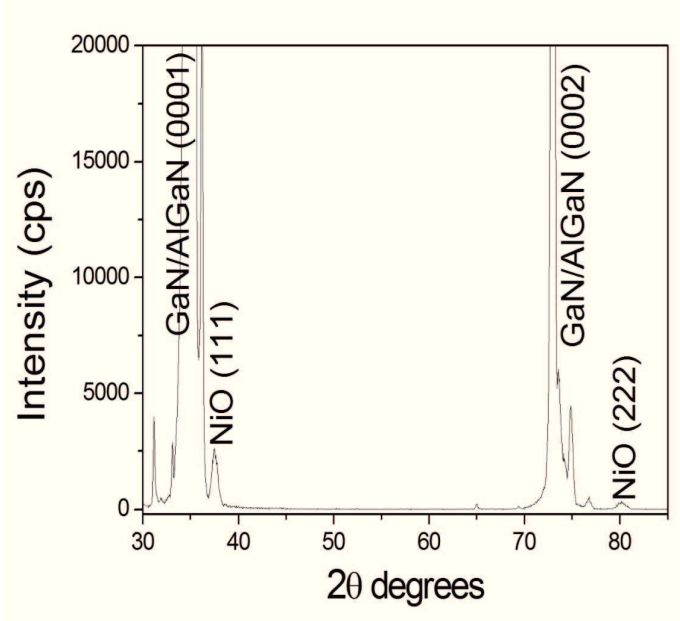

Fig. 6.1: *XRD patterns of the NiO film grown onto AlGaN/GaN heterostructure*

Fig. 6.2 shows a cross section TEM micrograph at low magnification, from which a thickness of the NiO layer of 15 nm has been estimated. High resolution TEM image (Fig. 1(b)) demonstrates the good quality of the interface, with the {111} NiO planes perfectly parallel to the {0001} planes of the GaN substrate. The epitaxial relationship has been confirmed by the fast Fourier transform (FFT) performed at the interface (see inset in Fig 1b). In fact, all the spots (the external ones related to the NiO and the internal to the AlGaN) are perfectly aligned. The occurrence of the epitaxial growth can be explained by evaluation of the NiO and AlGaN lattice structures. Nickel oxide belongs to the family of fcc oxides and possesses lattice parameters

a=b=c= 3.186 Å. The {111} planes of the fcc lattice show a hexagonal symmetry thus, it is possible to establish an epitaxial relationship between the hexagonal {0001} planes from the AlGaN substrate and the {111} planes of the NiO film. In particular, the overlap between the two hexagonal units from the NiO and AlGaN results in a lattice mismatch of about 5 %.

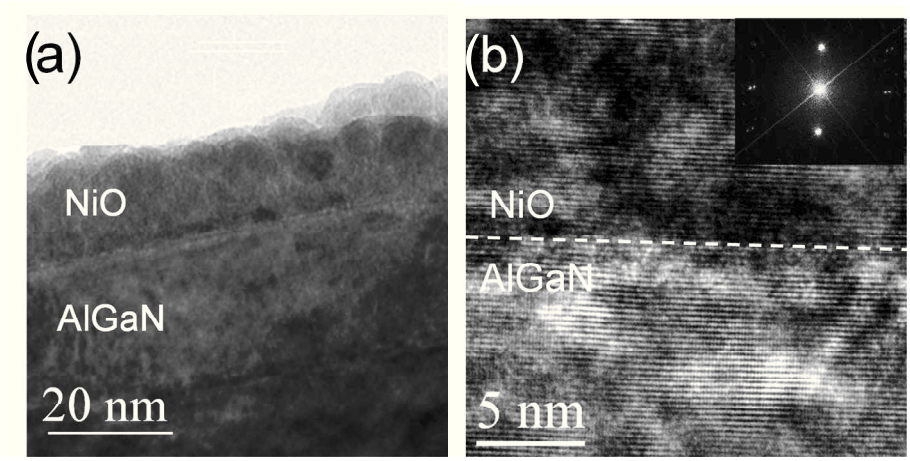

Fig. 6.2: *Cross section TEM micrographs of the NiO film grown onto AlGaN/GaN heterostructure: low magnification bright field contrast (a) and the NiO/AlGaN interfacial region acquired in the high resolution mode (b). The fast Fourier transform is shown in the insert.*

Additional morphological information on the NiO films has been obtained by atomic force microscopy (AFM). In particular, the AFM analysis (see *Fig. 6.3a*) show, for a scanned area of 5 μm^2 a root mean square (RMS) of 7 nm, comparable with the surface morphology of the underlying AlGaN (see *Fig. 6.3b*).

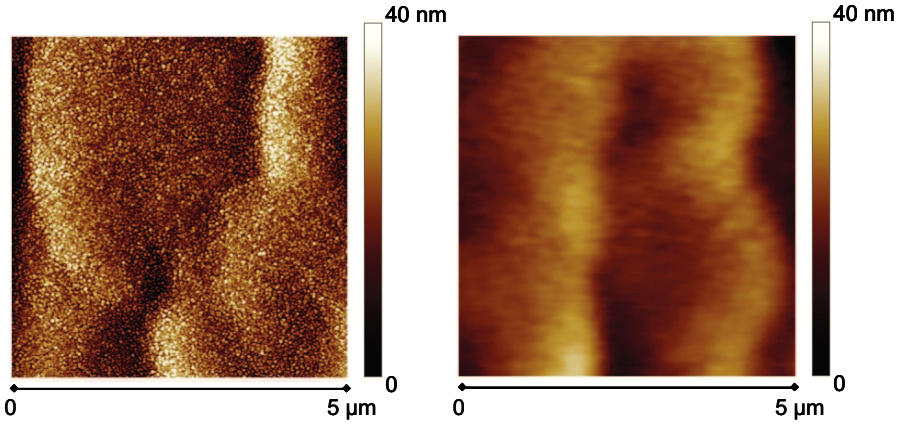

Fig. 6.3: *AFM images of the NiO surface growth on AlGaN/GaN heterostructures.*

Hence, it can be concluded that the selected deposition parameters provided uniform and smooth planar films. Furthermore, during the fabrication of the test patterns for the electrical characterization, the NiO film has been subjected to the thermal budget required by the Ohmic contact formation on source and drain regions (850°C). However, no appreciable change in both microstructure and morphology has been observed after this thermal treatment, thus proving a functional thermal stability of the film.

In order to investigate the effect of the NiO under the gate contact, the electrical characterization of the fabricated Schottky diodes was carried out. C-V measurements (showed in *Fig. 6.4a*) were carried out for the NiO/AlGaN/GaN MIS-Schottky diode and for the AlGaN/GaN reference diode. The measurements were performed at a frequency of 1 MHz, applying a small signal of 30 mV. Evidently, a decrease of the accumulation capacitance in the MIS diodes with respect of the reference diode occurs (from 1.95×10^{-7} F/cm^2 to 1.52×10^{-7} F/cm^2). Furthermore, in the MIS diode the transition from accumulation to depletion takes place at a more negative bias, as expected in a HEMT structure with an insulated gate. The decrease of the capacitance observed in the reference device at positive bias (i.e., above 0.75 V) is related to the increase of the forward current of the metal/AlGaN Schottky contact.

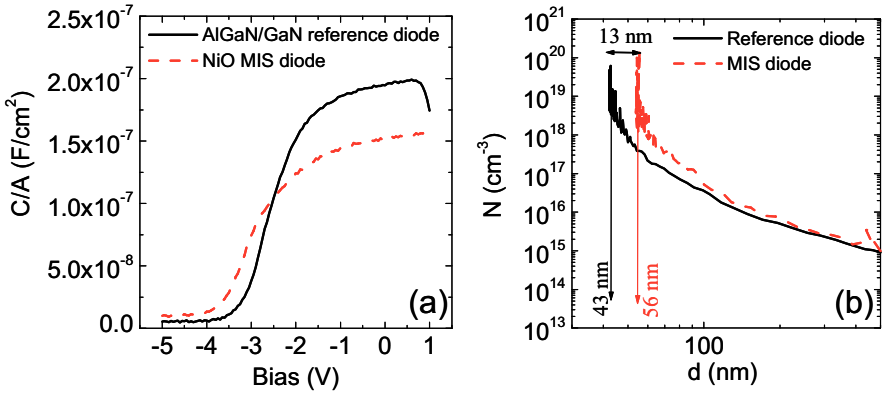

Fig. 6.4: *C-V characteristics of the NiO/AlGaN/GaN MIS diode and of the reference AlGaN/GaN Schottky diode(a)and the 2DEG concentration profiles N as a function of the depth d (b).*

By the C-V curves, according to the Eq. 2.31 was possible extract the dependence of the electron concentration *N* as a function of the depth *d*, both for the reference AlGaN/GaN diode and for the MIS diode. The *N(d)* profiles, showed in *Fig. 6.4b*, exhibit the peak at different depths, indicating the location of the 2DEG at 43 nm for the reference Schottky diode and at 56 nm for the MIS diode, respectively. Hence, the resulting thickness of the NiO insulating layer is 13 nm, in good agreement with the value measured by TEM analysis.

Moreover, from the C-V curves in the accumulation region, the measured capacitance in the MIS diode (C_{MIS}) can be considered as the series capacitance of the reference AlGaN barrier layer (C_{AlGaN}) and of the NiO insulating layer, i.e.,

$$\frac{1}{C_{MIS}} = \frac{1}{C_{AlGaN}} + \frac{1}{C_{NiO}} \qquad \text{(Eq. 6. 1)}$$

By applying the Eq. 6. 1 to the experimental data reported in *Fig. 6.4a*, the capacitance of the NiO layer (C_{NiO} = 6.89×10^{-7} F/cm^2) was estimated. Consequently, a NiO permittivity of 11.7 was calculated considering a NiO thickness of 15 nm (as determined by TEM). This value is in good

agreement with the NiO bulk permittivity [116] and properly higher than that of AlGaN alloys (~9.5). This latter aspect becomes quite relevant during high voltage operation, when the incorporation of NiO can induce the maximum electric field into the AlGaN/GaN region, in contrast to other gate insulators with a lower permittivity (Si_3N_4, SiO_2, Al_2O_3, Ga_2O_3) than AlGaN alloys. In this way, premature device breakdown in the gate dielectric can be prevented.

The impact of the NiO films on the electrical properties of AlGaN/GaN heterostructure has been further evaluated by I-V measurements. *Fig. 6.5* shows the current density-voltage (J-V) curves of the MIS-Schottky diodes using NiO as gate insulator, compared with those of the AlGaN/GaN reference Schottky diodes fabricated on the same sample. As can be seen, the introduction of a NiO layer as gate insulator leads to a shift of the forward characteristics towards higher bias values, which is accompanied by a reduction of the reverse leakage current. This behaviour is typical of a MIS Schottky contact and can be modelled using the classical description given by Card and Rhoderick [210]. Accordingly, the current density in the MIS Schottky diode can be expressed as [210]:

$$J_{MIS} = J_{Schottky} \exp\left(-\chi^{1/2}\delta\right) \qquad \text{(Eq. 6. 2)}$$

where $J_{Schottky}$ is the current density of the reference metal/semiconductor Schottky interface, χ (eV) and δ are the mean barrier height and the thickness of the gate insulating layer, respectively.

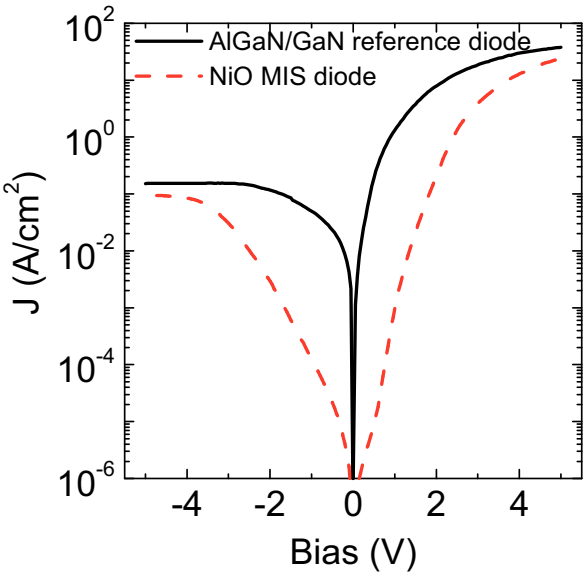

Fig. 6.5: *Current density – voltage (J-V) forward and reverse characteristics of the NiO/AlGaN/GaN MIS diode and of the reference AlGaN/GaN Schottky diode.*

Considering the predicted conduction band misalignment between NiO and AlGaN [116,211], i.e., a barrier of 1 eV, a decrease of the current density of a factor of 1.80×10^3 is expected at moderate bias when using a 15 nm NiO insulating layer onto AlGaN. As a matter of fact, under a forward bias of +1 V the reduction of the current observed experimentally is 1.44×10^3, close to the theoretical prediction. On the other hand, under reverse bias (-1 V) the current density in the MIS diode is reduced only by a factor of 1.44×10^2 . Hence, the MIS performances can be further improved by optimizing the quality of the deposited material and the device processing.

These preliminary results showed that NiO can lead to a reduction of the leakage current in the MIS Schottky diodes, close to the theoretical prediction. Moreover, the growth by MOCVD produced uniform films, free from voids and with a dielectric constant value close to that of the bulk

material. Hence, the MOCVD NiO thin films are promising as gate insulators for AlGaN/GaN HEMTs technology.

Obviously, more experimental and systematic work must be done in order to better understand the transport properties through the oxide and to which extent the electronic properties of this material can be tailored by changing the growth conditions.

Summary

After this travel in the world of the AlGaN/GaN heterostructures, understanding the advantages of using such system and the studying some issues related to device fabrication, it is not possible to draw some conclusion to this work of thesis. The conclusions of this work must represent not only the end point of this work of thesis, but rather a possible start for future research.

In this thesis, some surface and interface issues related to AlGaN/GaN heterostructures have been studied. In particular, a special attention was put on the physical problems connected to the fabrication of enhancement mode HEMTs.

Firstly, due to the specific characteristics of AlGaN/GaN heterostructures (like the thickness of the layer involved) a nanoscale approach has been used to investigate the local modification of the surface induced by some plasma or thermal processes. In particular, the effects of a fluorine plasma treatment of the surface of AlGaN or of a local thermal oxidation process under the gate regions were studied, both by means of C-AFM and macroscopic measurements on capacitors and diodes. These analyses demonstrated that the AlGaN/GaN heterostructure (and hence the 2DEG) are extremely sensitive to the above processes, which both caused a depletion of the 2DEG. In particular, despite the morphology of the surface resulted almost unchanged by these treatments, the C-AFM analysis showed an increase of the resistance in the channel below the treated region.

In the fluorine plasma treated sample, the C-V measurements clearly showed a shift towards less negative values of the threshold voltage, with respect to the untreated sample. The experimental results suggested that the electrical modifications occurring in the heterostructures are not only due to the introduction of negative fluorine ions, as already reported in the literature, but also due to the plasma-induced damage. .On the other hand, in the sample treated with a local oxidation process, a very thin surface oxide layer is formed, and its presence led to a more significant positive shift of the

threshold voltage (+4.95). However, a drastic reduction of the sheet carrier concentrations (6.87×10^{11} cm^{-2}) takes place. Even if this approach led to a reduction of the leakage current of the gate, the robustness of this thin thermal oxide layer may represent a concern under current or bias stress, thus making the process not yet reliable for practical devices.

Due to the severe limitations of these approaches, the use of a p-GaN cap layer onto an AlGaN/GaN heterostructure has been considered. In fact, this approach is probably the most elegant solution to achieve a normally-off behaviour with a stable threshold voltage. In this context, several physical issues related to the fabrication of p-GaN/AlGaN/GaN transistors have been investigated.

First of all, the use of a p-GaN gate requires the formation of a Ohmic contact onto p-GaN. Hence, the possibility to form low specific contact resistance Ohmic contact on p-GaN has been evaluated using a bilayer Au/Ni annealed in two different ambient condition, in Ar and in N_2/O_2 atmosphere. The electrical characterization showed that the sample annealed in an oxidizing ambient have a lower specific contact resistance, in the order of 10^{-3} $\Omega\cdot cm^2$ for an annealing at 600°C in a N_2/O_2 mixture. The electrical properties of the GaN (namely, its resistivity) were not significantly affected by these thermal treatments. A structural analysis of the metal layer after annealing demonstrated that the NiO phase formed after annealing is not present at the interface. Furthermore, a nanoscale electrical probing of the metal layer by C-AFM confirmed the low conductivity of the NiO phase, that can not be responsible of the reduction of the specific contact resistance (as sometimes reported by other authors). The study of the temperature dependence of the specific contact resistance enabled to establish the dominant carrier transport mechanism at the metal/GaN contact and to demonstrate the reduction of the Schottky barrier height from 1.07 eV, for the Ar annealed sample, to 0.71 eV for the N_2/O_2 annealed sample.

A lot of work was devoted to investigate the effect of a p-GaN layer as a gate contact onto an AlGaN/GaN heterostructure, in order to efficiently deplete the 2DEG and achieve a normally-off operation. For this purpose, HEMTs using p-GaN gate contact were first fabricated using different metal gate (Ti/Al/Ni/Au or Ni/Au) and compared with standard HEMTs (not including the p-GaN). C-V measurements showed a positive shift of the

threshold voltage from -3.9 V of the standard HEMTs to -1.1 V (Ti/Al/Ni/Au) and -1.8 V (Ni/Au) of the sample using p-GaN gate.. Since the complete depletion of the 2DEG failed in the first approach, and still a normally-on behaviour was observed, an optimization of the entire heterostructure was attempted. Here, computer simulations of the band structures in our system allowed to clarify that a reduced Al concentration and thickness of the AlGaN barrier can favour the complete depletion of the 2DEG in the absence of an applied bias. Hence, the electrical behaviour of new heterostructures, having an Al concentration of 20 % and an AlGaN thickness of 18 nm, has been studied. In this case, the C-V analysis on the test devices showed a normally-off behaviour with a threshold voltage of +1.4 V. Although this results is very promising, the quality of the used material was not optimal, as the I-V characteristic of the devices were affected by an excess of leakage current coming from the GaN buffer.

The problem of the leakage current arising when the gate bias exceeds the turn-on voltage of the p-GaN/AlGaN diode can occur in the normally-off technology with the p-GaN gate, but it is also common to almost all the proposed methods for normally-off HEMT. It can be overcome by the use of a gate dielectric below the metal gate. Due to the importance of this topic, in the last chapter of this work nickel oxide (NiO) was preliminary studied by structural and electrical analysis. NiO was chosen since, under appropriate conditions, it can be used itself as a material to induce the depletion of the 2DEG in normally-off HEMTs.

In particular, in this work it has been demonstrated that NiO thin films grown by MOCVD exhibit an atomically flat interface to AlGaN/Gan heterostructure, with the {111} NiO planes perfectly parallel to the {0001} planes of the GaN substrate. The electrical characterization on MIS diodes showed a dielectric behaviour close to the ideal one (ε_{NiO}= 11.9). Additionally, a significant reduction of the reverse leakage current with respect to a standard device without insulation in the gate was observed, thus making the material interesting for normally-on devices. Clearly, much more work is necessary to really understand the current transport through these thin oxide films, as well as to evaluate the possibility to tailor the electrical behaviour of NiO films making them suitable for normally-off operation.

In conclusion, basing on the experimental achievements presented in this thesis, it is clear that many aspects treated in this work deserve a further investigation and open new possibility of research.

First and foremost, it is clear that a reliable normally-off behaviour using a p-GaN gate onto an AlGaN/GaN heterostructure can be achieved only if the physics related to the heterostructure and the fabrication processes is well understood at a nanoscale level. In this context, the heterostructure can be still optimized to reduce the leakage current of the buffer and to further increase the threshold voltage towards the theoretical value. Preliminary simulations (not reported in this work) as well as literature data suggest that the use of a AlGaN back barrier behind a thin GaN buffer could give a better confinement of the 2DEG and a higher threshold voltage.

A critical concern that has not been mentioned in the work is the electrical activation of the Mg-dopant in the p-GaN cap. In fact, in the material used in this thesis, the Mg has been activated upon long-time thermal processes in-situ (in the reactor chamber after the growth of the heterostructure). However, such long processes can cause a diffusion of Mg towards the 2DEG, thus leading to a degradation of the overall electrical properties of the heterostructure (very low sheet carrier concentration, and low mobility). In this sense, a study on the mechanism of Mg activation through ex-situ rapid thermal annealing would be very useful to understand (and control) the final performance of the device.

Concerning the processing, as reminded several time in the text, one of the limitations of AlGaN/GaN HEMTs is the leakage current coming from the Schottky gate. In the specific case of a p-GaN gate approach, since the gate is fabricated before the Ohmic contacts, it will be subjected to the typical thermal budgets (around 800°C) for Ti/Al/Ni/Au source-drain contact formation. At such high temperatures, the metal gate (in our case Ti/Al has been used) can react with the p-GaN forming interfacial compounds and/or metallic spikes that can produce an excess of leakage current. In this sense, the study of a more stable metal gate (that does not interact with GaN, as for example a layer of TiN) could be useful for the improvement of the “gate-first” fabrication sequence. Another solution could be the reduction of the thermal budget necessary to obtain good Ohmic contacts on AlGaN/GaN heterostructures. To avoid high temperature annealing, a possible solution is in the use of Au free metal for Ohmic contacts. In fact, as an example, Ti-Al

based contact typically require lower temperatures to achieve Ohmic behaviour. Studying the physics of Au-free metallization for GaN HEMTs is practically an important issue since a Au-free technology is a key request to integrate GaN devices in the large scale Si fabs, where the use of Au is a source of contamination that must be avoided. In addition, it is known that the use of Au-free metal solution would lead to an improvement of the surface morphology of the contacts.

Finally, the use of a dielectric under the p-GaN gate contact must be considered for the further development of this family of enhancement mode HEMTs. In fact, the gate dielectric can both reduce the leakage current and increase the threshold voltage of the device. In this sense, the choice of the dielectric material for p-GaN, in terms of thickness and dielectric constant, will be the key issue in this research field for the final device performance.

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