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Analysis and Development of new strategies for solar energy conversion: New systems of integration, topologies and control

Vittorio Claudio Crisafulli

Coordinator of PhD

Prof. Alfio Consoli

Tutor

Prof. Alfio Consoli

a.a. 2007/2010

Scuola Superiore di Catania
Via San Nullo 101
CAP-95125 Catania
ITALY
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Preface

This work has been done in collaboration with the CePTIT (Unvirsity of Catania) and the System lab of STMicroelectronics. Acknowledgements are given to the Scuola Superiore of Catania and the above mentioned institutions for their financial support.

The research was carried out under the supervision of Professor Alfio Consoli from the Dipartimento di Ingegneria Elettrica, Elettronica e dei Sistem (DIEES) at Catania University. My deepest gratitude goes to my supervisor for his guidance and professional support during the elaboration of my PhD thesis.

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Vittorio Claudio Crisafulli December 2010; Catania

Abstract

In the recent past, energy and environment have played opposite roles in human progress. Energy has been as an engine for the development and the environment has been as the breaker of it.

Only after a more conscious and rigorous international policy on environment protection, not opposed to the development, energy and environmental matters have become unified behind a new sustainable model. This has determined new strategies in the energy sector. Hence, renewable sources have become a must in this new sustainable model.

The key role in the last decade has been played by the Distributed Power Generation Systems (DPGS) which present an efficient and economic way of generating electricity closer to the load(s). The DPGS can contribute to an efficient and renewable electricity future by potentially: increasing the use of renewable sources of energy; improving the efficiency of the electricity system by reducing transmission and distribution losses; improving the security of the electricity supply through increased diversity of supply and reduced vulnerability to simultaneous system failures. However, the new trend of using DPGS comes also with a suite of new challenges. One of the challenges is the interaction between the DPGS and the utility grid. As a consequence, grid interconnection requirements applied to the distributed generation are continuously updated in order to maintain the quality and the stability of the utility grid.

Consequently, the major tasks of this thesis were to analyze and to develop new strategies for solar energy conversion addressing efficiency and quality in order to allow the DPGS not only to deliver power with high efficiency to the utility grid but also to sustain it.

This thesis was divided into three main parts, as follows: “Small Photovoltaic System: AC module”, “Control of DPGS” and “New Topologies and Devices, technologies for multilevel inverter addressing grid connection”.

In the first part, the main focus was on topologies for module integration. Additionally, a new topology has been proposed and developed and successfully tested.

In the second part, the main focus was c on Control, PWM techniques and ancillary function as grid-connection algorithms.

In the third part, the main reported research was concentrated around the role of multilevel inverter in the next future of DPGS. Focusing on topologies and technologies device.

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Chapter 1
Introduction

This chapter presents the background and the motivation of the thesis, continuing with a short overview of grid-connected PV systems. Furthermore, it details the aims of the project, continuing with the outline of the thesis and finishing with a list of the main contributions

1.1 Background and motivation

Recently the energy global trend is unsustainable. Without decisive action, energy-related, emissions of CO_2 will more than double within 40/50 years and the oil demand will increase over the security of supplies. We can change our current path, but this will take an energy revolution and low-carbon energy technologies will have a crucial role to play. Energy efficiency, many types of renewable energy, carbon capture and storage (CCS), nuclear power and new transport technologies will all require widespread deployment if we are to reach our greenhouse gas emission goals.

Two renewable energy systems are the most dominant so far, which are wind and solar system. Wind is one of the most promising alternative energy technologies, while solar energy is the most abundant renewable energy resource on earth. The solar energy that hits the earth's surface in one hour is about the same as the amount consumed by all human activities in a year. Power electronics is the key technology to handle all this power and to adapt it in order to fit it in the grid.

In the last decade, photovoltaic (PV) penetration is coming out very rapidly due to dramatic cost reductions of the silicon wafer for producing PV cells. PV is a technology with a significant potential for long-term growth in nearly all world regions. Several solar PV roadmap vision said that PV is projected to provide 5% of global electricity consumption within 20 years, rising up to 10% in 2050. Achieving this target will require a strong and balanced policy effort in the next decade to allow for optimal technology progress, cost reduction and ramp-up of industrial manufacturing.

Solar PV, which generates electricity through the direct conversion of sunlight, is one of the three technologies available to use sunlight as an active source. Concentrating solar power systems (CSP) use concentrated solar radiation as a high temperature energy source to produce electrical power and drive chemical reactions. CSP is typically applied in relatively large scale plants under very clear skies and bright sun. The availability of thermal storage and fuel back-up allows CSP plants to mitigate the effects of sunlight variability. Solar heating and cooling (SHC) uses the thermal energy directly from the sun to heat or cool domestic water or building spaces. These three ways of harvesting sun energy are complementary, rather than directly competitive, and developers should carefully assess their needs and environment when choosing which solar technology to use.

The global PV market has experienced vibrant growth for more than a decade with an average annual growth rate of 60%. As of 2010, solar photovoltaics generates electricity in more than 100 countries and, while yet comprising a tiny fraction of the 4800 GW total global power-generating capacity from all sources, is the fastest growing power-generation technology in the world. Between 2004 and 2009, grid-connected PV capacity increased at an annual average rate of 60 percent, to some 21 GW

The large variety of PV applications allows for a range of different technologies to be present in the market, from low-cost, lower efficiency technologies to high-efficiency technologies at higher cost. Figure 1 gives an overview of the trend cost of PV module per watt in the last 3 years.

Almost completely, the requisites that make effective any reduction of energy consumption and CO2 emissions are based on Power Electronics. Stabilisation of the power grids with slow and constant integration of fluctuating renewable energies, effective and efficient injection of wind and solar energy into the grids, use of efficient controlled speed motor drives in industry and transportation, adoption of full electric or hybrid vehicles to allow energy efficient and low emission mobility, achievement of large scale energy savings in home appliance and lighting technologies, efficient energy recovery and energy management of storage systems, all such results can only be obtained through an extensive application of Power Electronics. The strategic and ambitious goals of the European Union for 2020 depend on the Europe's political choice and technical capability to provide a real adoption of the multidisciplinary techniques and components that are included in Power Electronics.

In a recent presentation of the ECPE (European Consortium on Power Electronics) Research Roadmap Team on "Power Grid Infrastructure & Renewable Energy Sources",

integration of different renewable energies has been indicated as one of the strategic tools to achieve the goal of having the Renewables (Wind and Solar) to contribute up to 30% to the global electricity energy production in 2030. By adding the contribution from hydro power, mainly produced in North-East Europe, the situation depicted in Fig. 1 is predicted, where Solar thermal and PhotoVoltaic (PV) power generation coming from South Mediterranean countries can contribute either with large scale PV installations and solar thermal plants either with distributed small scale PV plants. Integration to the grid of the renewable energies will occur via HVDC, energy lines with UHVAC and UHVDC, and in case of low voltage networks via distributed intelligent PV converters and advanced PLC. Intelligent Super Grid and Smart Grids interconnected as in Fig. 1 and Fig. 2 within are foreseen as the future energy systems.

In this scenario, while Power Electronics will have to face important challenges such as those of supplying high power Voltage Source Control technology, DC-circuit breakers for meshed HVDC overlay grids, improved DC-grids, and MV DC/DC converters with or without galvanic isolation, power converters for low-power PV generation systems will also cover an increasing important role as they appear the only tool to effectively establish large scale distributed energy, generated by the sun and connected to the grid. In fact, even in the future distributed generation systems exploiting sun energy will continue to be based on a conversion process where power converters, advanced Pulse Width Modulation (PWM) techniques and microcontroller based control systems are associated to achieve high conversion efficiency, high power factor, and low current harmonic THD [1][2].

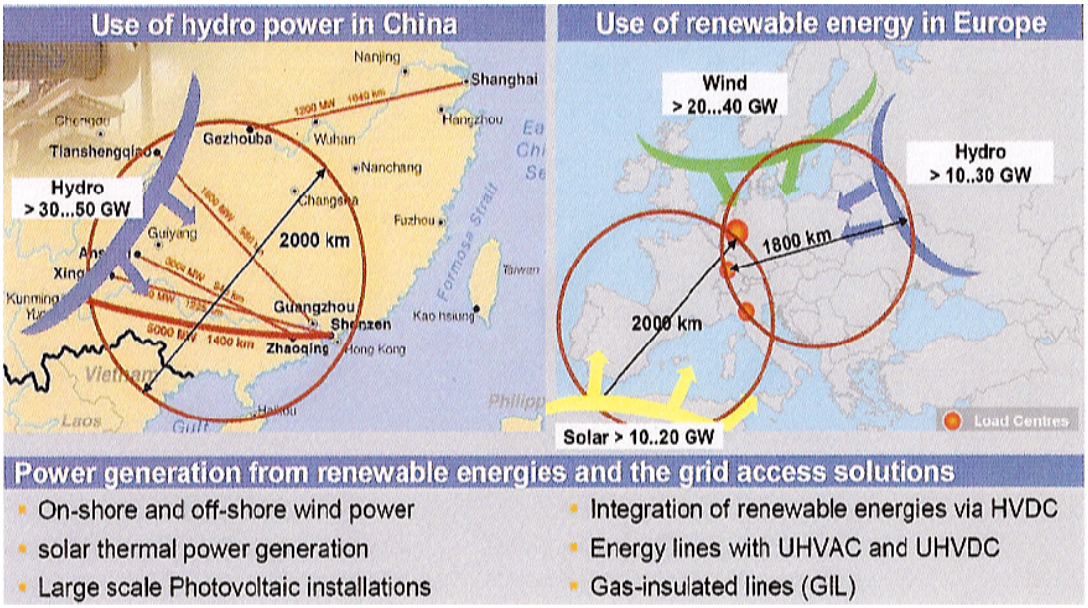


Fig. 1 Grid access for large-scale renewable (Source: Siemens AG).

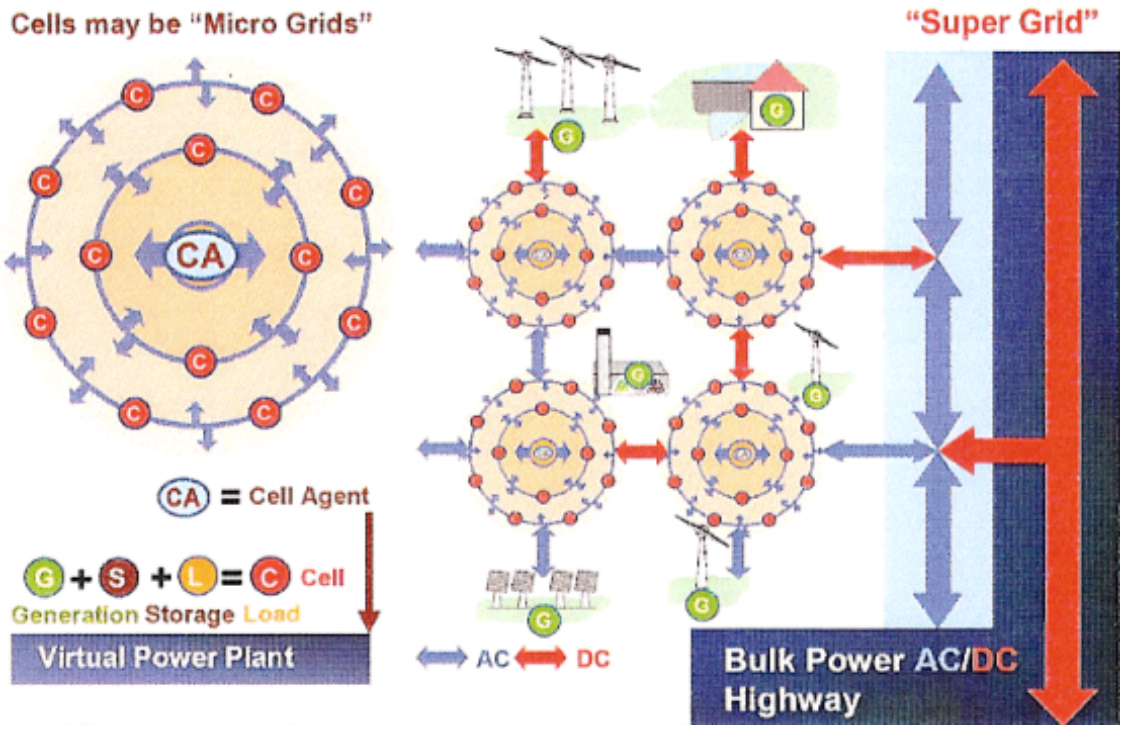


Fig. 2. Future energy system will be formed by intelligent Super Grid and Smart Grids (Source: Siemens AG).

Nowadays, technical improvements and advances in the circuit design of the converters, and integration of the required control and protection functions into the converter control circuit have allowed to introduce into the market advanced PV converter systems that also provide sufficient control and protection functions such as maximum power tracking, inverter current control, and power factor control. Within the range of power till 10 kW several DC/AC converter configurations have been proposed from single stage to double or multi-stage topologies according to the number of cascaded power stages, with or without a low or high frequency power transformer. Single-stage single-phase or three-phase inverters are the traditional solution adopted to interface a large number of PV modules to the grid as the modules are connected in series to create strings with a suitable high value of the output voltage and the strings are connected in parallel through interconnection diodes to obtain the desired power level. The presence of the low-frequency transformer and the poor efficiency of the centralized inverter associated to the poor performance of the Maximum Power Point Tracker (MPPT), have moved to "string conversion" solutions, which basically consist in a double stage power converter for each string of the PV plant. Using an input stage in boost configuration allows one to connect fewer panels in series to create the DC voltage, while increasing the overall efficiency of the power conversion, as the blocking diodes are not requested and the MPPT algorithm is applied to only one string with limited number of panels. String conversion configurations based on several DC/DC converters connected to a

high voltage DC bus and linked to a single DC/AC converter in principle appear as more complex solutions but offer higher efficiency due to single string MPPT control and modularity of the PV plant. Finally, for very low-power applications it is recognized that the solution based on AC modules is the best one to solve such issues as input power optimization, plant modularity, and system reliability. With this architecture every single PV panel is directly connected to the grid through MICroinverters (MIC) having the same power of the panel and installed on its back-side.

1.2 Photovoltaic Systems

1.2.1 Problem formulation

The cumulative PV installations reached by the end of 2009 more than 20 GW worldwide experiencing an important growth despite the financial crisis. This shows that the need for renewable energy is a strategic issue due to climatic impact, sustainability and high development rates in China and India.

The large penetration of PV inverters especially in low voltage networks related to residential/commercial PV plants stability issues are becoming challenging. New, more stringent grid requirements are expected to emerge following the path of wind power with global goal of turning renewable energy power plants in "virtual" power plants. As PV penetration is growing, the impact on grid stability is becoming important. New demands like voltage ride-through, voltage regulation, island operation, are emerging.

Photovoltaic energy generation is becoming increasingly significant in providing sustainable energy for the ever-increasing needs of the society, and it will play a key role in the world energy scenario.

Mass penetration of PV generation requires not only that the entire PV installation meets performances, but prerequisites new solutions to improve yield, availability, stability and robustness for seamless integration into the electricity network. The efficiency of commercial PV panels is around 15-20%. Therefore, it is very important that the power produced by these panels is not wasted, by using inefficient power electronics systems. The efficiency and quality of both single-phase and three phase PV inverter systems will be improved using new topologies, new controls and ancillary function.

1.2.2 Objectives

The aim of this project is to analyze and develop new topology, exhibit a high efficiency will be proposed, as well as new advanced control algorithms for the PV Power systems. All these functions can be implemented in the current platforms of the PV inverters on the market and turn them in so-called Smart PV Inverters with more market value and increased grid integration potential.

The main societal objective of this project is to facilitate the mass penetration of PV generation therefore contributing to a greener future.

1.3 Main contributions

A short list of contributions is included in the order they appear in the thesis.

- Review and simulation of Module Integrated Converter (or ACModule) topologies A comprehensive review is presented by modelling several structures: DC/DC and DC/AC topologies, focusing on efficiency and cost. It has been shown that the topology proposed is one of the best compromises in cost, efficiency and high voltage gain. It is also emphasized that where isolation is needed the best topology is a classic boost interleaved with isolation and regenerative active clamp (presented in the bidirectional DC/DC converter for HEV).
- Review and comparison of a control algorithm for grid synchronization In this thesis, the most popular grid synchronization algorithms were thoroughly reviewed and compared. The comparison was carried out by using simulations tools Matlab/Symulink and Dspace platform. The system was then tested using a real setup. All the algorithms were tested and compared under several distortion conditions (reference)
- PWM techniques comparison The effect of different PWM techniques applied to the PV inverter were analysed while taking the Total Harmonic Distortion factor and efficiency into account. The standard unipolar and bipolar techniques and the mixing frequency technique were incorporated in the analysis. This analysis has shown the potentiality of the mixing frequency techniques compared to the standard techniques.
- New topology In the near future there will be many significant changes in the grid-cod addressing the PV inverter. At the moment PV inverters only feed the active power to the grid using a power factor equal to 1. However, the high penetration of PV inverters in the last few years has caused some problems, because the power injected at the distribution

level has been increased by the DGPS without any update. In fact, when there are many inverters injecting active power at the same time, the voltage at the Point of Common Coupling (PCC) might rise over the limits stated in the standards and trigger the safety of the inverters leading to disconnection or limit the power production below the available power. In order to overcome the mentioned disadvantages, the future standard system will impose to add a new control for the power curtain or for reactive power injection world-wide. This injection will change the structure of the new inverter. Modified Neutral Pont Clamped inverter with new technologies POWER devices has been presented in this thesis. The structures with these new power devices were compared with the standard under different conditions of load and power factor.

1.4 Outline of the thesis

The continuous increase in power demands makes decentralized renewable energy production more and more the only way to supply the energy needs next in the future. Decentralized energy production using solar energy could be a solution for balancing the continuously-increasing power demands. This continuously increasing consumption overloads the distribution grids as well as the power stations, therefore having a negative impact on power availability, security and quality.

It is the goal of this thesis to analyze and model and to introduce new strategies for harvesting high efficiency and high quality in term of energy conversion from photovoltaic systems. The focus of this thesis is to introduce new topology and additional control method.

Chapter 1 of this thesis details the application and motivations of this work while Chapter 2 covers the principles of module integrated converter and its operation. Chapter 3 focuses on a comparison of new topology and the state of the art concerning MIC, Chapter 4 presents hardware setup and experimental results. Chapter 5 present control structure for single phase inverter, focus on PLL. Chapter 6 cover the multilevel issue in renewable energy with conclusion and future work covered in Chapter 7 of this thesis.

This thesis goes into detail on the design considerations for every aspect of this system. This includes modeling, simulation, hardware implementation, control algo- rithms and experimental testing

1.5 Scientific production

List of Publications

I. "*A New Resonant Active Clamping Technique for Bi-directional Converters in HEVs*" N.Abbate, M. Cacciato, A. Consoli V. Crisafulli, G. Vitale; Accepted to be published in ECCE2010, Atlanta Georgia, September 2010

II. "*Digital Controlled Bidirectional DC/DC Converter for Electrical and Hybrid Vehicles*", N.Abbate, M. Cacciato, A. Consoli V. Crisafulli, G. Vitale; Accepted to be published in EPE-PEMC 2010 Ohrid, Republic of Macedonia, Settembre 2010

III. "*A High Voltage Gain DC/DC Converter for Energy Harvesting in Single Module Photovoltaic Applications*", M. Cacciato, A. Consoli, V. Crisafulli; Accepted to be published in ISIE2010, Bari, July 2010

IV. "*Robustness evaluation of phase-locked loop algorithms for single-phase distributed generation systems*", M. Cacciato, A. Consoli, V. Crisafulli, G. Scarcella, G. Scelba; SPEEDAM 2010, Pisa

V. "*Latest ST MOSFET and IGBT technologies for the best efficiency in solar inverters*", L. Abbatelli, S. Buonomo, M. Cacciato, A.Consoli, V. Crisafulli, R. Scollo; PCIM Europe 2010, Norimberga

VI. "*Power Converters dor Photovoltaic Generation Systems in Smart Grid Applications*" A. Consoli, M.Cacciato, V. Crisafulli; Revista da associacão brasileira de eletronica de potencia – SOBRAEP vol. 14, no 4, novembro de 2009

VII. "*Power Converters dor Photovoltaic Generation Systems in Smart Grid Applications*" A. Consoli, M.Cacciato, V. Crisafulli; The 10th Brazilian Power Electronics Conference COBEP 2009

VIII. "*Tecnica PWM a Basse Perdite per Sistemi di Generazione Monofase Connessi alla Rete*", A. Consoli , M. Cacciato, V. Crisafulli, G. Frascadore; Convegno Nazionale AEIT 2009 Catania

IX. "*Convertitori DC/AC per pannello Fotovoltaico*", A. Consoli , M. Cacciato, V. Crisafulli; Convegno Nazionale AEIT 2009 Catania

X. "*ESBT Technology in industrial converters: The best way to cut your losses*" S. Buonomo, V. Crisafulli, G. VItale, M. Nania, R. Scollo; PCIM Europe 2008

XI. *"ESBT® Power Switch in High Efficiency DC-DC Converte*r" S. Buonomo, V. Crisaflilli, V. Enea, M. Nania, A. Raciti, C. Ronsisvalle, R. Scollo; IECON 2007. 33rd Annual Conference of the IEEE

XII. *"Experimental Investigation of Monolithic Cascode Devices in Inverter Leg Applications*", F Chimento, V. Crisafulli, S. Musumeci, A. Raciti, S. Buonomo, R Scollo; 42nd IAS Annual Meeting

Part I
AC Module

Chapter 2
AC Module Concept

The interest toward the application of MIC converter is increasing in the last years mainly due to the possibility of highly efficient decentralized clean energy generation. The output voltage of a single panel is in the range of 24-36V, generally below 50 V. Consequently, low-power applications with high output voltage require a high gain for proper operation. Several solutions were so far proposed in the literature, ranging from the use of high-frequency transformers to capacitive multipliers. In this chapter an evaluation of different topology is proposed. Finally a prototype of the best topology came from the comparison is presented and tested. This chapter presents the basic concept of photovoltaic generation, continuing with a short overview of grid-connected PV systems and finally presents the MICroinverter or ACModule concept.

2.1 PV cell

In 1839, Becquerel discovered the ability of certain materials to convert sunlight to electricity, when he discovered the photogalvanic effect. The first solar cell has been producted in 1954 by Chapin, Fuller, and Pearson. This cell had a conversion efficiency of 6%. Within 4 years, solar cells were used on the Vanguard I orbiting satellite. The high cost of boosting a payload into space readily justified the use of these cells, even though they were quite expensive.

The most popular materials for direct conversion of sunlight to electricity have been crystalline silicon (Si), amorphous silicon (a-SiH), copper indium diselenide (CIS), cadmium telluride (CdTe), and gallium arsenide (GaAs). All of these semiconductor materials have band-gap energies between 1 and 2 eV.

The band gap of a semiconductor is the energy required to excite an electron from the valence band to the conduction band of the semiconductor. Transferring the negative electron to the conduction band creates a positive hole in the valence band. Both charge carriers are then available for electrical conduction.

Sunlight is a very convenient source of energy for creation of these electron–hole pairs (EHPs), since most of the energy in the solar spectrum is at levels higher than the band-gap energies of PV materials. Once the EHP has been produced by an incident photon, the electron and hole must flow in opposite directions. Separation of electron and hole can be achieved by using a pn -junction. A pn-junction is composed of material that is rich in electrons on one side (the n-side) and rich in holes on the other side (the p-side). The pn-junction produces a built-in electric field, directed from the n-side to the p-side, that separates the photon-generated EHPs. The electrons are forced to the n-side and the holes are forced to the p-side by the junction electric field as long as the EHP is produced within or close to the pn-junction. If the EHP is generated too far from the junction, the electron and hole will recombine before they can be separated by the junction electric field.

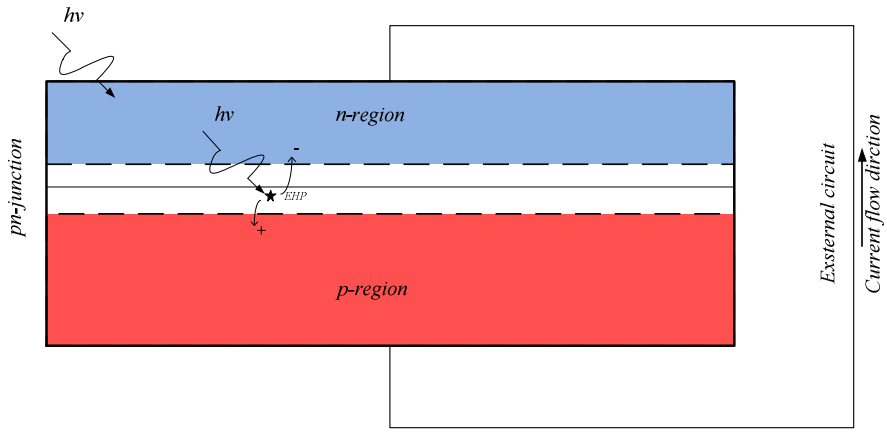


Fig. 1 Solar Cell

Figure 1 shows photons (hv) entering a typical PV cell. Some of the photons will create EHPs close to the surface, some will create EHPs near or within the junction region, and some will penetrate beyond the junction. Generally, the highest-energy photons produce EHPs close to the surface, whereas the lowest-energy photons penetrate the deepest. This process of liberating an EHP results in the conversion of part of the energy of the incident photon to electricity. Any leftover energy is converted to heat. If the EHP is produced near or within the pn-junction, the electron is swept into the n-region and the hole is swept into the p-region. The electrons (−) then diffuse toward the top of the cell and the holes (+) diffuse toward the bottom of the cell. As the electrons reach the top surface, where there is a contact to an external circuit, they continue to flow into the external circuit. As the holes reach the bottom surface, where there is another contact to the external circuit, they recombine with electrons flowing in from the external circuit. For each electron that leaves the top, another enters the

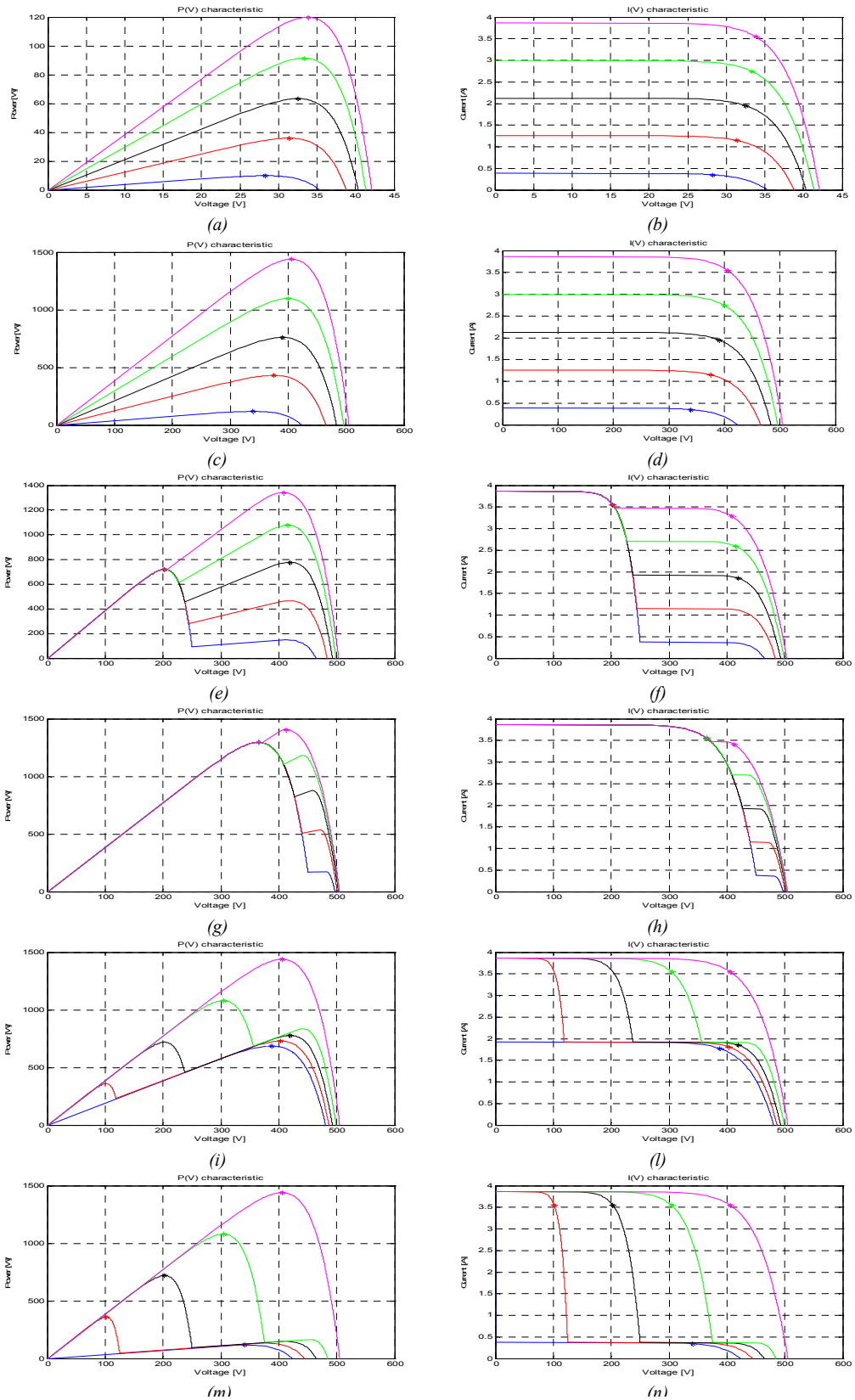


Fig. 2 *(a)* V-I single PV-panel 120 W; *(b)* P-V single PV-panel 120 W; *(c)* V-I 12 PV-panels 100% irradiance; *(d)* P-V 12 PV-panels 100% irradiance; *(e)* V-I 12 PV-panels 100% irradiance with 50% effect shadow level; *(f)* 12 PV-panels 100% irradiance with 50% effect shadow level; *(g)* V-I 12 PV-panels 100% irradiance with 10% effect shadow level; *(h)* P-V 12 PV-panels 100% irradiance with 10% effect shadow level; *(i)* V-I 12 PV-panels 100% irradiance with 10% effect shadow area; *(l)* P-V 12 PV-panels 100% irradiance with 10% effect shadow area; *(m)*, V-I 12 PV-panels 100% irradiance with 50% effect shadow area; *(n)* P-V 12 PV-panels 100% irradiance with 50% effect shadow area;

bottom. This completes the circuit, with electron flow in the external circuit and the flow of both electrons and holes within the PV cell. The challenge in the design of the PV cell is to absorb all incident photons close enough to the pn-junction so all electrons and holes generated will be collected. A further challenge in cell design is to minimize conversion of sunlight to heat and maximize conversion to electricity. Because of the pn-junction, a voltage appears between the bottom and the top of the cell. This voltage is what forces the current through the external circuit. Depending upon the cell material, the voltage developed by the cell may range from very small up to about 1 V. Thus, to produce higher voltages, the cells must be connected in series. When cells are connected together, normally they are incorporated into PV modules, which often combine as many as 40 cells in series to produce voltages in the range of 20 V and currents of several amperes. When voltages and currents beyond the capability of an individual module are desired, the modules can be connected into arrays that will produce higher voltages and higher currents. Although most cells produce only a few watts, and most modules produce 10 to 300 W, most arrays produce a few thousand watts. A few very large systems have been deployed that produce power in the megawatt range.

An important feature of all modern PV cells is that, over their lifetimes, they can produce up to ten times as much energy as was used in their fabrication and deployment.

The ideal solar cell operates as a diode when in the dark, and operates almost as an ideal current source when operated under short-circuit conditions. The short-circuit current of the cell is close to directly proportional to the intensity of the sunlight incident on the cell. The current source nature of the cell means that if cells are connected in series to increase their overall voltage, the cells must be closely matched so each cell produces identical current

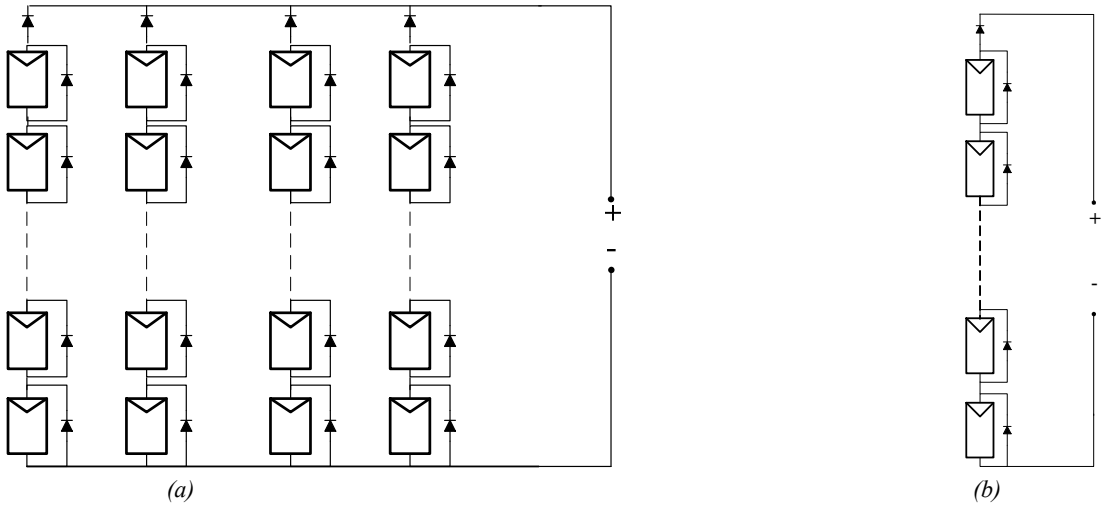


Fig. 3 *(a)* multistring system; *(b)* single string system

under identical illumination conditions. If this is not the case, the voltage of the series combination will not be optimized. The I–V relationship for the ideal PV cell is given by Eq.1

$$I = I_L - I_0 \cdot \left\{ e^{\frac{k \cdot t}{q \cdot v}} - 1 \right\} \qquad \textbf{Eq. 1}$$

where I_L is the photon-generated current component, I_0 is the cell reverse saturation current, and k*T/q=25.7 mV at a temperature of 25°C. More specifically, the photocurrent is related to sunlight intensity by the relationship: Where G is the sunlight intensity in W/m ^{2} and G_o= 1000 W/m ^{2}.

Figure 2 shows the different behaviour of the PV module under normal condition and shadow condition. Fig. 2 (a) and (b) (a) show the I–V and P-V characteristics as a function of incident sunlight for a single PV panel. Fig. 2 (c) and (d) show the I–V and P-V characteristics as a function of incident sunlight for an array of 12 PV-panels (as shown in Fig. 3). The other plots in Fig. 2(x) show the same characteristics under different condition of shadow area and shadow level of the PV array. It is evident the degradation of the P-V and I-V characteristic under abnormal condition. Note that as the temperature rises, the open circuit voltage of the PV-cell, V_{OC}, decreases. For Si cells, the rate of decrease is 2.3 mV/°C for each cell. Thus, a 36-cell module (as shown in Fig. 4) operating 25°C above ambient temperature, will lose 36 ×2.3×25= 2070 mV = 2.07 V. This is nearly a 10% loss in output voltage, which, when coupled with approximately temperature-independent current, results in a 10% power loss. The departure of the I–V characteristic of a real cell from that of a perfect cell is measured by the fill factor (FF) of the cell. The assumption is that a perfect cell would have a rectangular characteristic, with constant current up to the maximum cell voltage, and then constant voltage. The constant current would be the short-circuit current and the constant voltage would be the open-circuit voltage. Since the current produced by a cell depends upon the total power incident of the cell, if a cell is shaded even partially, it will not produce the same current as unshaded cells. At a certain point of shading, the polarity of the cell voltage reverses to enable the cell to carry the current generated by the unshaded cells in the module. When this happens, the cell dissipates power, and can overheat to the point of cell degradation.

To protect the module against cell degradation, bypass diodes are normally incorporated into the module design to shunt current away from shaded cells, as shown in Fig. 3.

If the voltage of a module drops below the voltage of other modules connected in parallel, it is possible for the current produced by the higher-voltage modules to flow in the reverse

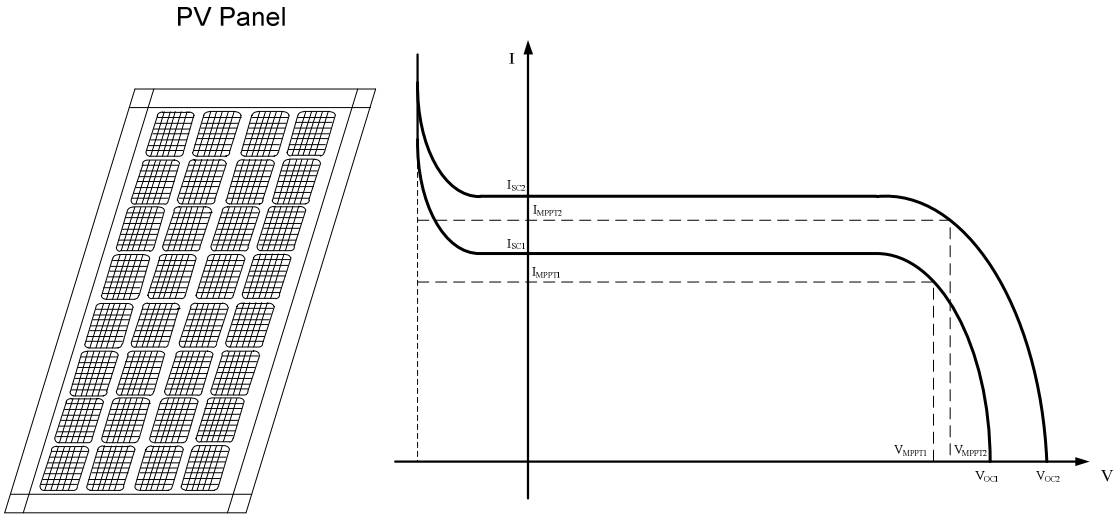


Fig. 4 PV-Cell and V-I characteristic

direction of the lower voltage module. To prevent reverse flow of current through a module, a blocking diode is sometimes used in series with the module, as shown in Fig. 3.

2.2 ACmodule Concept

Solar power production is affected by various factors such as module mismatch, obstruction shading, inter-row shading, and obstacles such as dust or debris. In addition, non-uniform changes in temperature, irradiance, and shading create complex current-voltage curves, further affecting energy harvest. This is due to the fact that in traditional systems the performance of the entire system is dictated by the performance of the weakest module.

Inverter R&D has focused on two areas. The first is incremental changes in the existing string/central inverter, and most of these changes are geared toward higher efficiency and larger capacity. These changes have led to bigger, more centralized inverters, for example, SMA's new 500kW 500U PV inverter.

The second recent inverter development is a move toward decentralized architectures, including partial solutions such as DC-to-DC optimizers, consisting of add-on electronics designed to augment a central inverter, and complete inverter solutions such as microinverters [3].

Recently, the development of a new energy conversion solution in low power Photo-Voltaic (PV) generation systems has started. It consists in the integration of a small converter inside the junction box of PV panels used for solar energy harvesting. Such a converter, called AC Module (ACM), shows AC output characteristics with grid-connection capability without external DC connector. ACMs should achieve similar costs of the produced kWh as those

obtained with standard systems. Therefore, in developing a new ACM system the main issues regard the converter efficiency and cost.

Although the characteristics of the ACM may change according to panel specifications, its structure is composed by the cascade connection of two stages, a DC/DC and a DC/AC. The DC/DC stage is used to boost the output voltage of the PV module up to a value suitable for connecting the module to the grid with standard single-phase inverter. The DC/DC converter is also responsible for implementing the Maximum Power Point Tracking (MPPT). Therefore, high efficiency and elevated voltage gain are the most important performance required in this application to the DC/DC converter. In particular, high voltage gain can be obtained through charge-pump systems or high-frequency transformers that remain the only solution in case a galvanic isolation is required.

At the moment one of the main issues in “Solar Conversion” is to obtain the maximum power available from the field in all weather conditions. In order to get the Maximum Power a lot of specific control algorithms, such as MPPT (Maximum Power Point Tracking), have been done. Conventional system modules linked together in series may perform differently, simply because of dirt or accidental shadowing. Under these conditions, the MPPT is unable to function properly and adapts all modules to the worst performance and penalizes such all. In order to solve this problem a new topology has been used, which is adopted by many manufacturers: one inverter circuit is combined with multiple independent MPPT's that divide the plant. However, an inverter of several kilowatts, even in case of multi-string, requires a high voltage input. In this case, the shading problem continues to persist. Figure 1 shows in the left side the model of a string converter, while in the right side different configuration for string converter.

When the PV series string is operating under non-uniform conditions of radiation, as it is often the case in PV array, a problem arises. All the cells in the system share the same current, and when a cell or group of cells is shaded one of two scenarios may occur:

- The group of shaded cells will try to drive the unshaded ones into operating at a lower current level. In this case the system output power is limited by the current produced by the cell or panel generating the lowest output current.
- The unshaded cells will try to drive the shaded ones into operating at a higher current level. The only way a PV cell can operate at a higher current than its short circuit current, which is directly proportional to irradiance, is by moving into the negative voltage region of the cell’s I-V curve where it becomes reverse biased as shown in Fig. 1. At this point the panel’s backplane diode(s) becomes forward biased and it conducts the string current. The down side is that now the group of shaded cells is en-

tirely bypassed, contributing zero power to the system, and the string voltage is also affected.

It is apparent that due to widely varying voltage levels of the series string, another dc-dc converter is needed to regulate the dc input voltage to the inverter. The Maximum Power Point Tracker within the inverter decides which of the two situations described above takes place. This central converter must be able to operate at high voltages and currents and withstand large voltage swings. Such a component may increase the complexity of the controls of the system, but more importantly, it will add significant cost and losses to the PV installation.

In order to address and try to mitigate the series string problem, a concept called the Module Integrated Converter (MIC) was developed. It solves the series string problem by adding dc-dc converters at the output of each panel. The overall tolerance of the system against irradiance mismatches is improved because now each panel is not affected by the operating conditions of its neighbours.

The concept of the AC photovoltaic module or Module Integrated Converter, a photovoltaic module with an integrated DC/AC, has been proposed several years ago at Caltech's Jet Propulsion Laboratory, but is only now reaching commercial realization.

The AC Module concept has many advantages over central inverter systems, the main ones being a low minimum system size and the ability to site individual modules without concern for shading and orientation.

A module integrated converter approach whether DC/DC or DC/AC has many advantages:

- AC Module systems improve system reliability because of distributed hardware (redundancy), testability (via communications links) and simplicity (no high voltage DC components or wiring)
- Better Utilization (MPPT) per module basis: Each module can independently control and so optimise the power flow to or from its source. In a solar power application, each module can independently perform maximum power point tracking (MPPT) for its PV-panel. This allows panels to be given different orientations opening up new possibilities in architectural applications. Greater tolerance of localised shading is now also possible. These reasons taken together are the most important advantage of per-panel distributed modules.
- Mixing of different sources becomes possible: Independent and intelligent power flow control can decouple each source from the others in the string. Batteries could be replaced individually as required since old and new batteries can now be mixed.

Existing PV module strings could be extended with new higher output panels without compromising overall string reliability or performance.

- Better protection of module power sources: Intelligent protection can be applied on a per source basis. A single shaded PV module can deliver its power rather than being bypassed by a diode for its own protection.
- Redundancy of both power converters and modules: An intelligent module can bypass a failed source or indeed a failed converter if appropriately designed, allowing the complete installation to continue operation at slightly reduced capacity.
- Greater safety during installation and maintenance: Depending on design, each module may be able to isolate its connected power source, so the wiring of series or parallel connections of modules can be performed safely. The module, power source connection is a safe low voltage connection.
- System design and installation costs are reduced via product standardization
- The minimum array increment of one AC module and the elimination of balance-of-system equipment allows for maximum flexibility in initial sizing and simple future array expansion
- AC arrays are exposed to damage from nearby lightning strikes.

Inverter technology has always had a significant impact on energy harvest. The serial nature of module installation results in the "Christmas light effect," i.e., any impact (dust, debris, shade) on module performance will also affect the other modules in the string. Distributed inverter architectures mitigate this effect as each module becomes an independent power producer. Per-module MPPT enables increased energy harvest.

There are of course some disadvantages. The main one is that for systems over about 50 kW total, a central inverter can be made very cheaply - it is likely that large systems "behind the utility fence" will not be AC module devices.

Possible disadvantages of AC-modules are the following:

- Increased zero-load dissipation compared to conventional PV-systems.
- Increased thermal stress on the inverter, because the inverter is mounted on the back of the module.
- New residential scale PhotoVoltaic (PV) arrays are commonly connected to the grid by a single DC-AC inverter connected to a series string of PV modules, or many small DC-AC inverters which connect one or two modules directly to the AC grid.
- ACMs must operate in a very harsh thermal environment which affects their component lifetime;

- ACMs interaction can be an issue in large PV plants;
- high efficiency is difficult to be obtained in small power converters;
- system costs.

2.3 Series vs. parallel string of module-integrated converters.

The present grid connected module integrated converters that convert directly to 240Vac can lay claim to these advantages. However, this approach of direct grid connection has the disadvantage of a large difference in voltage from input (low) to output (high). This requires a transformer based converter, which requires more mass and volume, is more expensive, and is less efficient than a simple DC-DC converter [4][5][6].

A series rather than parallel connection of converters allows the input-output voltage ratio to be close to unity, which leads to the highest switch utilisation, and removes the need for a transformer. Efficiencies of close to 100% are possible, and converters can be small, light and low cost.

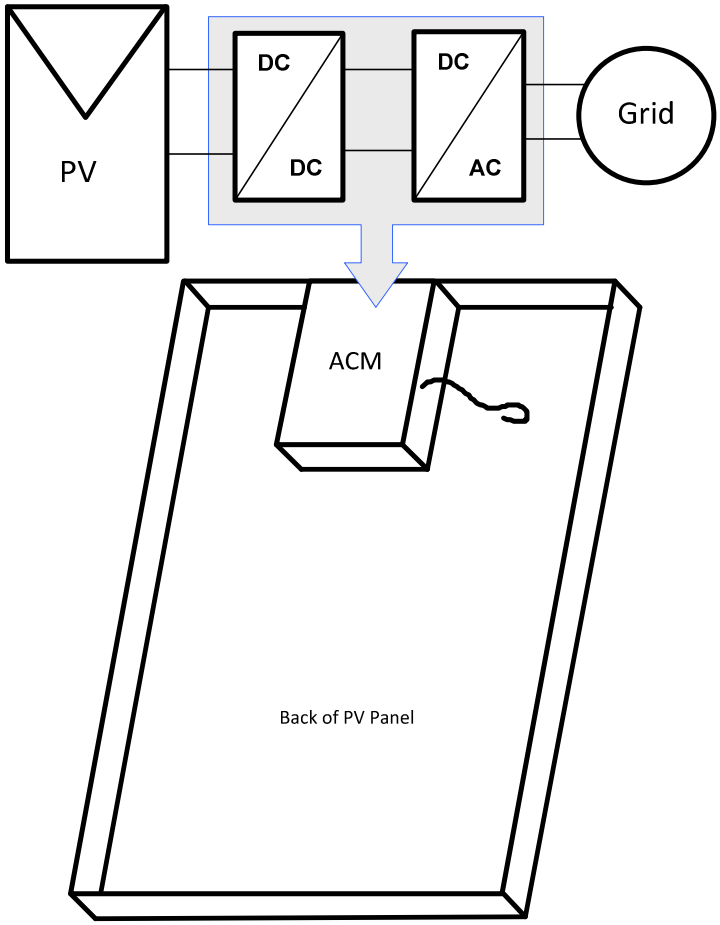


Fig. 5: Basic topology of an ACModule

A series connection utilises low voltage MOSFETs, Schottky diodes, inductors and capacitors that have been developed for low voltage DC-DC converters. A parallel connected converter requires high voltage fast recovery diodes and MOSFETs, which are at a performance vs. cost disadvantage.

2.3.1 Central Inverter

In the Photovoltaic scenario the most common system layout is the centralized inverter, or plant-oriented, topology, which consists of series connected PV modules (also called PV strings) all connected in parallel in order to fit voltage and power constraints, as shown in Fig. 6,has led this structure to be widely used in large grid-connected installations. . The PV modules were divided into series connections (called a string), each generating a sufficiently high voltage to avoid further amplification. These series connections were then connected in parallel, through string diodes, in order to reach high power levels. These series connections were then connected in parallel, through string diodes, in order to reach high power levels. The benefits of this topology are the low specific converter cost and simple maintenance.. This centralized inverter includes some severe limitations, such as high-voltage dc cables between the PV modules and the inverter, power losses due to a centralized MPPT, mismatch losses between the PV modules, losses in the string diodes, and a non flexible design where the benefits of mass production could not be reached. The grid-connected stage was usually line commutated by means of thyristors, involving many current harmonics and poor power quality. The large amount of harmonics was the occasion of new inverter topologies and system layouts, in order to cope with the emerging standards which also covered power quality.

Centralized PV inverters perform two major functions: power conversion from DC to AC; and Maximum Power Point Tracking (MPPT):

- Power Conversion

Traditional solar energy central and string inverters convert current by ‘chopping’ the 200 to 480 volt DC voltage from the source solar strings, typically using local controls and a power conversion bridge. By filtering and tuning the frequency of the supply, the inverter ensures the current is in phase with the grid to ensure the current is grid-compliant and can be used for standard residential or commercial loads or sold back to the utility.

- Maximum Power Point Tracking (MPPT)

The goal of the MPPT algorithm is to extract the greatest power available from the solar array. The better the MPPT algorithm, the greater the power output. With a central inverter, the MPPT is performed on the solar array as an aggregate. However, changes in temperature,

irradiance, and shading create complex current-voltage curves, thereby making it difficult or impossible for the MPPT algorithm to find a power point that is optimal for all modules. This results in a compromise in operating conditions and results in less than optimal energy harvest.

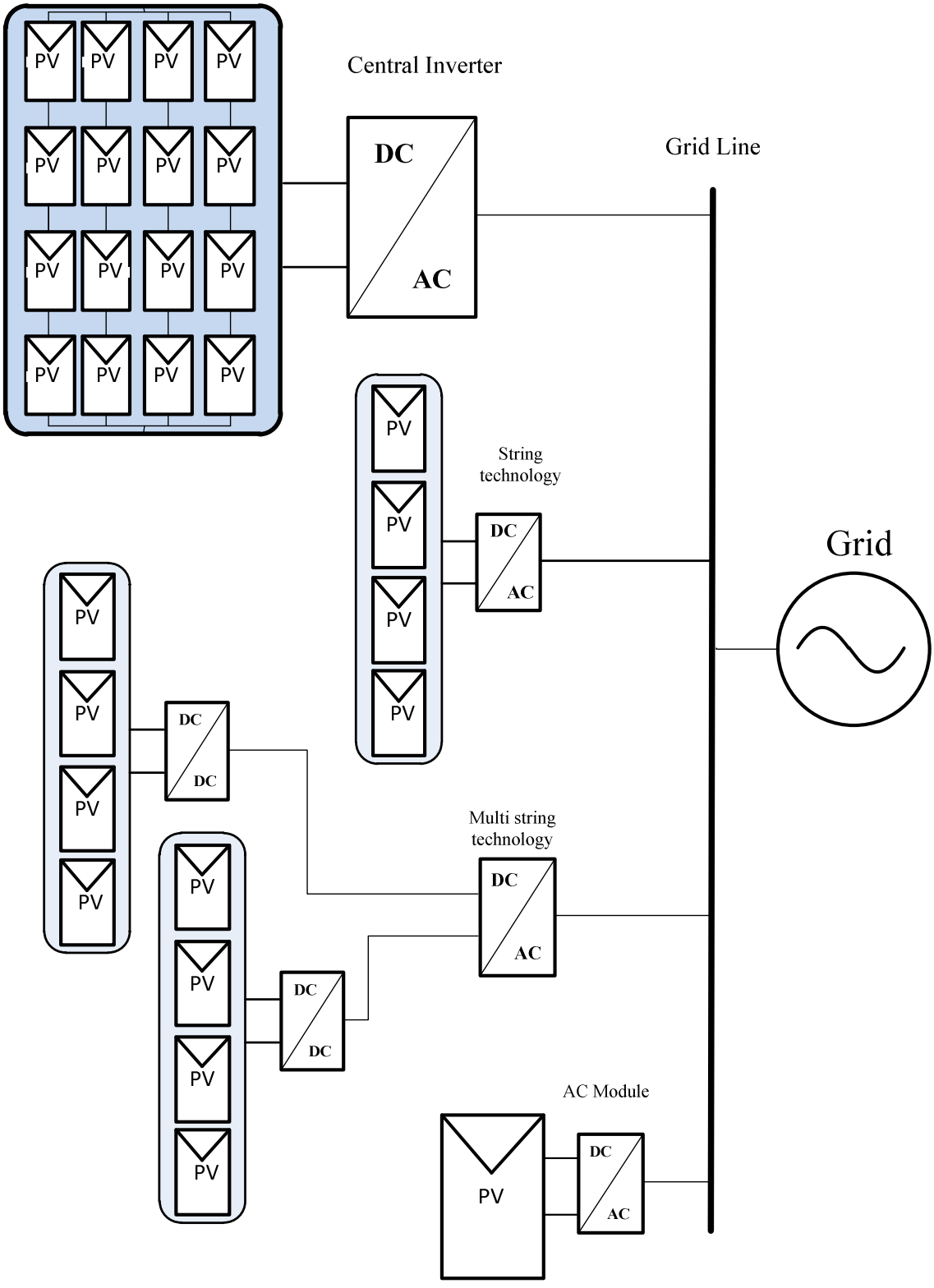


Fig. 6: PV topology; central inverter, string converter, multi string converter and ACModule.

In addition, varying roof orientations, and module mismatch (often resulting from typical manufacturing tolerances) can also have an impact on energy harvest. Other challenges associated with centralized inverters include the space required to locate the device, as well as heat dissipation requirements. Large central inverters are typically actively cooled. These cooling fans can make a tremendous amount of noise , so location of the inverter relative to offices and occupied areas must be considered.

2.3.2 String Inverter

Recently, in photovoltaic installation, the string inverter have been preferred compare the central inverter strategy. The string inverter, shown in Fig. 6, is a reduced version of the centralized inverter, where a single string of PV modules is connected to the inverter. String inverters prevents mismatch losses between strings and lets each string operate at its maximum power point. Furthermore, string diodes are removed which reduces energy losses. Yet, the extra inverters not only add power conversion losses but also elevate the cost of the PV system. That is one of the reasons why large plants usually favor centralized configurations.

In terms of continuity of service, it is very unlikely that all string inverters are down simultaneously, which ensures at least a minimal photovoltaic production on the grid. String inverters are also future proof, in the sense that the capacity of a module oriented installation can be upgraded easily, if the grid connection allows additional capacity flow. An additional innovation to this topology is the team concept which aims to improve power conversion efficiency during low solar irradiance. By using dc switches which cross-connect strings together, as shown in Fig. 6, the strings may be combined (as in the centralized topology) in order to accept a larger solar irradiance PV production range and enhance conversion efficiency by using only one inverter

The input voltage may be high enough to avoid voltage amplification. This requires roughly 16 PV modules in series for European systems. The total open-circuit voltage for 16 PV modules may reach as much as 720 V, which calls for a 1000-V MOSFET/IGBT in order to allow for a 75% voltage de-rating of the semiconductors. The normal operation voltage is, however, as low as 450-510 V. The possibility of using fewer PV modules in series also exists, if a dc–dc converter or line-frequency transformer is used for voltage amplification. There are no losses associated with string diodes and separate MPPTs can be applied to each string. This increases the overall efficiency compared to the centralized inverter, and reduces the price, due to mass production.

2.3.3 Multi String Inverter

The multi-string inverter depicted in Fig. 6, is the further development of the string inverter combines the two previous topologies by introducing a dc-dc converter with MPPT control strategies for each string of the PV array. Several strings are interfaced with their own dc–dc converter to a common dc–ac inverter. This is beneficial, compared with the centralized system, since every string can be controlled individually. The dc-dc string converters are also used to elevate PV string voltage to a high voltage dc bus while using a MPPT strategy. The introduction of a dc bus reduces inverter functionalities, for example the MPPT is transferred to the DC/DC converters and also eases heterogeneous PV module integration. Indeed, modules used from one string to another, may differ in age, size, technology, or even nominal power values Thus, the operator may start his/her own PV power plant with a few modules. Further enlargements are easily achieved since a new string with dc–dc converter can be plugged into the existing plat- form. A flexible design with high efficiency is hereby achieved. Finally, the ac cell inverter system is the case where one large PV cell is connected to a dc–ac inverter. The main challenge for the designers is to develop an inverter that can amplify the very low voltage, up to an appropriate level for the grid, and at the same time reach a high efficiency. For the same reason, entirely new converter concepts are required.

2.3.4 MIC or AC Module

The ac module depicted in Fig. 3 is the integration of the inverter and PV module into one electrical device. It removes the mismatch losses between PV modules since there is only one PV module, as well as supports optimal adjustment between the PV module and the inverter and, hence, the individual MPPT. It includes the possibility of an easy enlarging of the system, due to the modular structure. The opportunity to become a “plug- and-play” device, which can be used by persons without any knowledge of electrical installations, is also an inherent feature. On the other hand, the necessary high voltage-amplification may reduce the overall efficiency and increase the price per watt, because of more complex circuit topologies. On the other hand, the ac module is intended to be mass produced, which leads to low manufacturing cost and low retail prices.

The present solutions use self-commutated dc–ac inverters, by means of IGBTs or MOSFETs, involving high power quality in compliance with the standards.

2.4 What is String converter?

MIC is a new concept, concerning renewable energy. Photovoltaic cells produce direct current (dc) power. The utility wiring and appliances within the home use alternating current (ac) power with voltages in the range of 110 Vrms (USA) and 220 Vrms (Europe). Therefore all grid connected PV installations require an inverter to convert power from dc to ac. The input dc voltage to the inverter must be large in order to most efficiently convert to the ac-line voltage. The standard solution for achieving this is by connecting several PV panel in series in order to build up the system's output voltage.

In a dc-dc converter, power is converted from dc to ac by periodic switching of the transistor. The ac power signal, also referred to as indirect power, is then rectified again through the diode and converted back to dc. The key to obtaining high efficiency in this application is the minimization of indirect power at the nominal operating point. This implies generating the least amount of ac power possible by minimizing switching and processing of the input dc signal. This is achieved by use of a converter having a buck-boost characteristic, designed to have a voltage conversion ratio of unity at the nominal operating point. The circuit can operate in a mode called "pass-through" which achieves maximum efficiency by directly connecting input and output ports of the converter. Neighbouring operating points in the buck or boost mode also exhibit (MPPT) DC/DC converter (MPPT) very high efficiency, and hence the insertion loss for this approach is very low. This architecture allows for maximum flexibility and improved tolerance in a system under mismatched conditions.

The MPPT block of this system operates independently from changes in the string current, which allows the converters to exhibit output characteristics of a constant power source. This means that the string current and voltage are adjustable, and it is possible to regulate the string voltage by tuning the string current. With a fixed string voltage the string becomes modular and it is possible to easily add more strings in parallel or connect the system to a battery bank. Additionally, the central dc-dc converter becomes redundant and unnecessary, greatly improving the total power output of the PV installation at a minimum added cost.

In 2001 Shimizu introduced a Generation Control Circuit capable of "shuffling" power between adjacent PV modules. This concept was further improved two years later by Walker, who proposed non-isolated, inverting, bidirectional dc-dc converters for the same purpose. This proposal is intended for series connected PV strings that are evenly lit, and therefore the efficiency of the converters is optimized for their quiescent state. Each MIC processes only the power difference between adjacent modules, allowing them to operate at different currents

as long as the shuffling converters support this current difference. This way a power stage with smaller rating and higher efficiency can be implemented.

However, the author notes that in the worst case scenario where two adjacent modules are shaded, the converters connected to these panels must operate in deep buck mode in order to supply the full string current of the array. Therefore the MIC must be rated after all, for the same current, voltage and power as the panel they support. Another converter is necessary at the string level in order to interface the top and bottom modules. A bidirectional Flyback is suggested for the central dc-dc converter. The efficiency of the flyback converter, generally notorious for being low, is not included in the author's simulation of the system.

It is also important to note that these converters implement a passive form of MPPT, by simply operating at a fixed panel voltage, close to the maximum power point voltage. The main assumption being that changes in irradiance and temperature will be low enough that the voltage at the maximum power point will only vary slightly. Active maximum power point tracking is performed by the array's dc-ac inverter.

Four different converter topologies for PV module integration have been investigated by Walker and Sernia in 2002. Efficiency vs. input power for each of these was predicted via simulation for a 60 W module using synchronous rectifiers. The authors concluded that the boost converter is not capable of always delivering the full amount of output power from a series connected string under shading conditions. The buck converter can deliver any amount of power, but the string will require many more panels. If the buck or boost converters reach a minimum or maximum duty cycle boundary, the string output voltage will be limited. The dc-dc converter at the string level is still necessary to ensure proper regulation of the dc input to the inverter. The authors concluded that the buck-boost and Chuk converters were too expensive and inefficient to be deemed practical.

2.5 Summary

The PV cell was introduced in this chapter. The mode of operation under normal and abnormal condition was also presented. The partial shadow is also treated in many papers. The case of partial shadow is included in the chapter in order to show the problems associated with it. Thus, even a small amount of partial shadow may result in severe power losses, and the risk of delamination, and a very irregularly voltage-power characteristic. The irregularly characteristic is a problem for most Maximum Power Point Trackers (MPPT). This is regarded as a problem, which must be dealt with.

Finally, the MICroinverter concept has been presented with a short review of its history and types of technologies.

Chapter 3
MIC for Photovoltaic modules

The interest toward the application of MIC converter is increasing in the last years mainly due to the possibility of highly efficient decentralized clean energy generation. The output voltage of a single panel is in the range of 24-36V, generally below 50 V. Consequently, low-power applications with high output voltage require a high gain for proper operation. Several solutions were so far proposed in the literature, ranging from the use of high-frequency transformers to capacitive multipliers. In this chapter an evaluation of different topology is proposed. Finally a prototype of the best topology came from the comparison is presented and tested..

3.1 Strengths of ACModule

Although the design techniques of converters for PV panels may change according to the panel specifications, efficiency and voltage gain are the two most important performances required to such architectures. In particular, a high voltage gain of the DC/DC converter is requested and this can be obtained through charge-pump systems or high-frequency transformers, which remain the best choice in case galvanic isolation is required.

Although the classic boost converter is theoretically capable of reaching a high voltage gain, in practice, the gain declines as the duty cycle approaches unity due to parasitic components. In addition, the control stability at operation with very high duty-cycle values is severely affected.

One alternative would be associating in cascade either conventional boost converters or interleaved variants or employing a modified cascaded boost in order to achieve the required gain. A major disadvantage here is the poor efficiency level due to losses in the two successive power processing stages.

To surpass such limitations, several topologies proposed in the literature can achieve high voltage gain without requiring high values of duty cycles or multiple cascaded stages. A common important feature is also the reduced voltage stress across the active semiconductors.

Such features can be achieved by one of the following techniques, as will be discussed in the succeeding sections: isolated magnetic means, non isolated magnetic means, and finally, capacitive means.

In addition, higher levels of efficiency are, in general, not attainable due to the association of several power processing stages. An alternative to the previous circuits is the use of the high frequency transformer as an energy storage inductor, like in variants of the isolated dc–dc forward or push–pull converter. Such solutions are nevertheless normally limited to lower power levels and also attain reduced efficiency, with the rise of problems like high voltage stress, large switching losses, and electromagnetic interference problems, mainly due to the negative effect of the leakage inductance and winding capacitance of the transformer. In order to bypass such drawbacks and reach a higher level of efficiency, the circuit proposed in [20] modifies the basic current-fed push–pull converter to employ a current doubler stage that reduces conduction losses in the input stage and a zero-current-switching voltage multiplier in the output with no losses due to reverse recovery.

High gain is also achieved here through the turns-ratio relation, although, now, non-isolated structures like coupled inductors or magnetically coupled non-isolated converters are considered. One first example of such approach would be a boost converter where two magnetically coupled windings are placed before and after the switch so that not only is the gain increased but also the voltage stress across the switch is reduced. In order to deal with the problem related to the leakage inductance, several clamping circuits as proposed in in literature. When compared with the galvanic isolated topology circuits, the circuits in this section are capable of achieving a higher level of efficiency as only a single stage is present. In addition, reduction of the voltage stress across the semiconductors is possible in most circuits, which allows further reduction of the losses and costs.

3.2 Topologies under comparison

There are several design strategies for converters panel. The most serious problem is related to the high voltage gain that is required of the stage DC / DC converter. For good performance, this value of gain can be obtained by using charge-pump systems or through the use of high frequency transformers. In countries that require galvanic isolation is better to use the second strategy, if the use of a high frequency transformer is considered sufficient.

In this thesis several solutions have been investigated. In Fig. 7 it is shown an interleaved

boost insulated classic. This converter shows a very high gain achieved through the use of a transformer with a secondary center-tapped. The control strategy of the devices is a classic PWM interleaved between the two channels to reduce input ripple current. In fact, the transistors Q1 and Q2 are made to switch at the same frequency and with the same duty cycle but 180 ° out of phase signals to each other. High gain is achieved here through the turn-ratio of a high frequency transformer that provides galvanic isolation between the source and the grid and also normally allows the use of low voltage-rated active switches in the input side. The high-frequency waveform in the input of the transformer can be generated by a voltage-fed or current-fed full bridge inverter, whereas the last one attains reduced semiconductor conduction losses since both legs are connected in parallel during the short-circuit interval. The output is then rectified by a conventional diode bridge. Two inherent disadvantages of such circuits are the high amount of switching losses, as higher frequencies are normally employed to reduce the size of the transformer, and the higher conduction losses due to the sum of inverter and rectifying stages. In order to deal with the first disadvantage, the use of a soft-switching technique can be employed, although a common drawback is the increased complexity in the operation and construction. The switch control strategy is a standard interleaved Pulse Width Modulation (PWM) between the two channels, able to reduce the ripple of the input current, as the two transistors have the same switching frequency and duty-cycle and a phase shift of 180°.

A possible solution for the second disadvantage is to substitute the diode bridge with a high-frequency active voltage doubler leg that provides reduced conduction losses with additional gain. As a conclusion regarding the circuits discussed so far in this section, the use of a high-frequency galvanic isolation is more appropriate when very high gains are required or at medium power levels.

Fig. 8 shows a dual interleaved isolated boost converter. The high gain is obtained through the two center-tapped transformers that load the output capability. The control strategy is slightly different from the previously stated but easy to implement. There are two interleaved phases, each with two transistors. The devices at each stage Q1-Q2 and Q3-Q4 are controlled by signals out of phase with each other by 180 ° and slightly overlapping, as shown in Fig. 9.

The dual boost-interleaved converter uses two high-frequency transformers to charge the output capacities and again ensure the high voltage gain. In this case two interleaved phases are introduced with two transistors each, which are driven according to the shown strategy

where a small overlapping is inserted in the 180° phase shift. According to table 3 the two isolated boost converters have in high voltage gains and low voltage stress on the transistors their best performance, while especially the dual boost is penalized by the number of devices and voltage and current stress. Efficiency of dual boost (90%) is also lower than that shown by the classic boost-interleaved (95%).

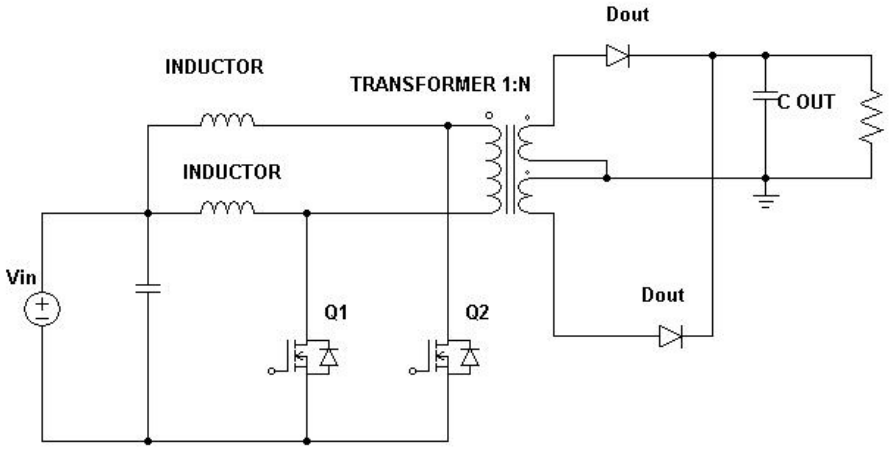


Fig. 7 Boost-Interleaved Converter with HF Transformer.

Fig. 10 shows a variant of the converter presented previously. An alternative interleaved isolated boost converter is the l-type half-bridge shown in fig. 9 [8][9]. In this case the two transformers have no central connection in the secondary winding but they still allow one to shift of 180° the secondary voltages according to the shown configuration and, most important, through the circuits obtained with the four diodes the charge of both output capacitors is contributed by both transformers. The control strategy is the same. The main difference is the use of two transformers without center tap in the secondary. With the connection shown in Figure you can get the secondary voltage 180 ° out of phase. The main difference compared to the previous case is that, through the circuit formed by diodes D_1-D_2-D_3-D_4, each secondary transformer contributes to the position of both output capacitors. Efficiency is in between the two previous converters but number of switches and diodes, and stress is the worst as always in this class of converters.

In Fig. 11 is presented the Multi-Stage converter. The basic structure is always a two-phase interleaved boost, but with the peculiarity to use in place of an inductor per phase, a single inductor and a transformer with two primary and one secondary. The two primary voltages are fed out of phase with each other by 180 ° to decrease the current ripple and make the current equal in the two phases. The secondary is used to load a voltage doubler, which is connected

in series with the output capacity of the interleaved boost.

Fig. 12 shows a multicell converter. It too is based on an interleaved boost with coupled inductors to reduce input current ripple, but with the addition of a charge pump (diode-capacity) over the two transistors.

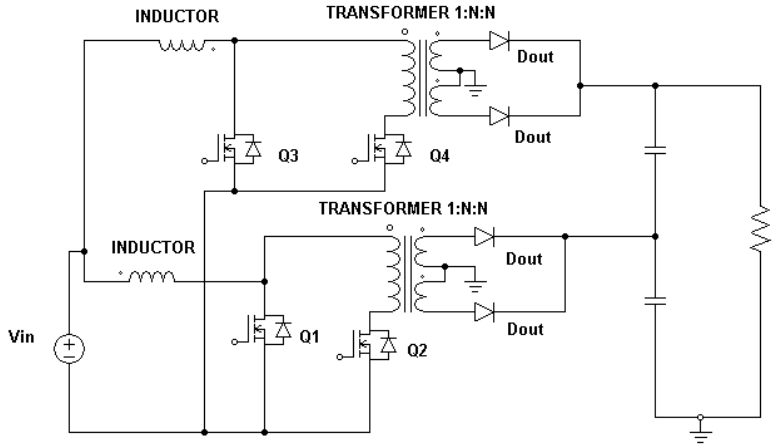


Fig. 8 Dual Boost-Interleaved converter with HF Transformers

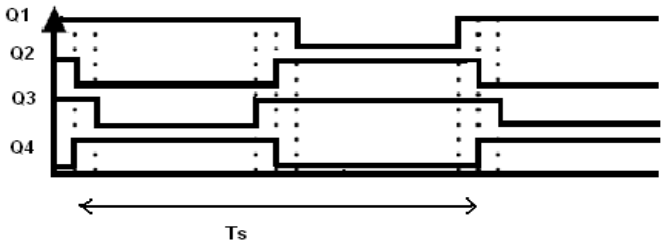


Fig. 9. PWM signal for the dual boost-interleaved converter with HF Transformers

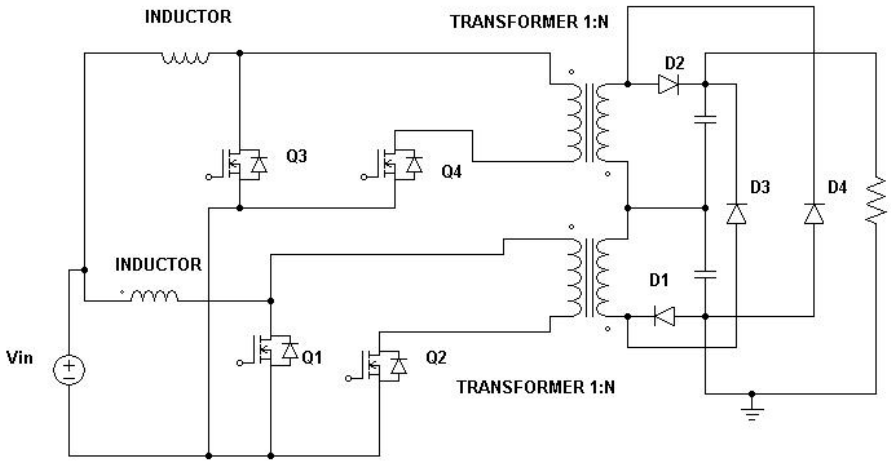


Fig. 10: L-type Half-Bridge Interleaved Isolated Boost converter.

As it has been proved by the simulation comparison, in order to increase the converter efficiency Multi-stage or Multi-cell configurations have to be adopted. The Multi-stage converter of Fig. 10 is still an interleaved two-phase boost with the peculiar characteristic of using a single inductor and a transformer with two primaries and a secondary winding. The two transformer primaries are fed by 180°-shifted voltages in order to reduce the current ripple and make equal the phase currents. The secondary winding charges a voltage doubler, which is connected to the positive terminal of the output capacitor of the interleaved boost.

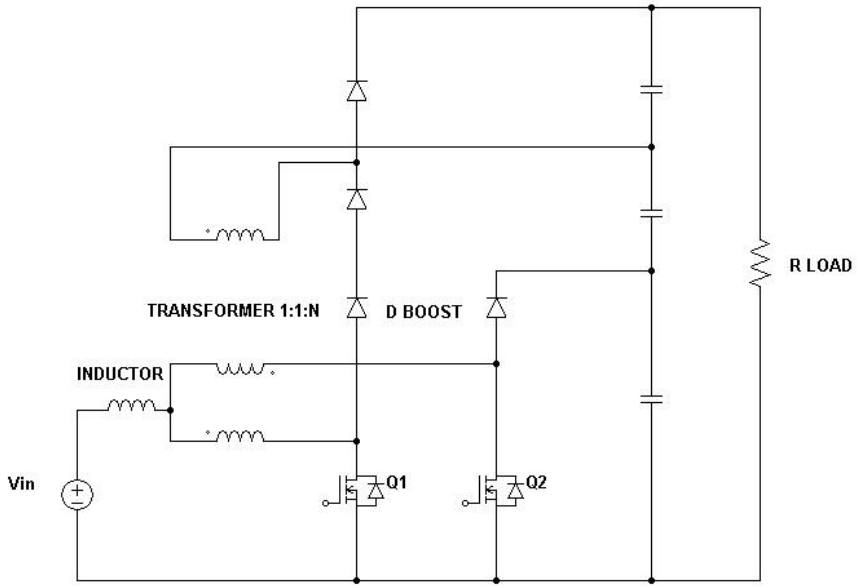


Fig. 11: Multi-stage converter.

The Multi-cell converter of Fig. 11 is also based on an interleaved boost with coupled inductors to reduce the ripple of the input current. However, in this case a charge-pump system including diodes and capacitors is added to the two transistors. This converter is highly penalized by the number of diodes although each one of them experiences a voltage stress eight times less than the other topologies and a voltage stress on the transistors that is half of the dual boost and L-type boost.

As it shows the higher efficiency and best performance at low and high loads, the Multi-cell converter seems the best candidate to cover a worldwide market request of MICs including bus multi-voltage feature for European (230 V) or North America (110 V) requirements. In Fig. 13 the efficiency curve calculated at different loads on an experimental prototype confirms the simulation predictions-

3.3 Evaluation of the ACModule

A detailed study of each afore-mentioned converter was performed in order to understand the advantages and the disadvantage of each of them. Each converter has been analyzed using well known software, like PSpice and PSIM. In Table 1 are reported the results of performance comparison of the five DC/DC converters, afore mentioned, chosen among the most adopted solutions concerning MIC. Several aspects have been taken in to account for this comparison. Efficiency of each configuration has been calculated through application of the "Californian Ponderation" expression (shown in Eq. 3):

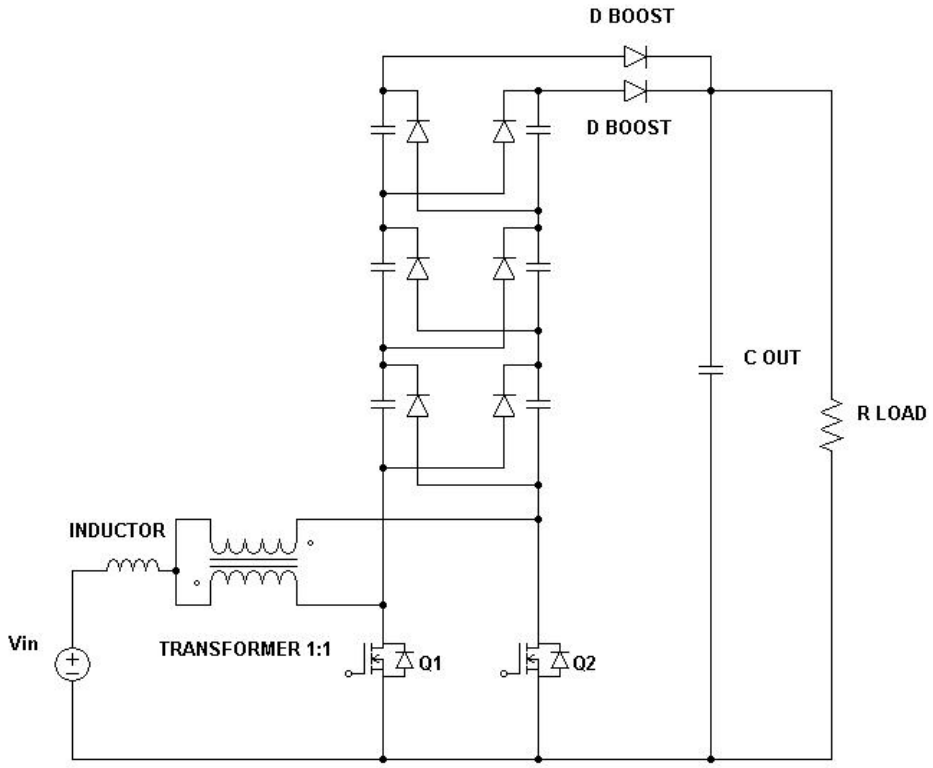


Fig. 12: 3-Stades Multi-cell converter**.**

$$\eta_{CEC} = 0{,}04 \cdot \eta_{10\%} + 0{,}05 \cdot \eta_{20\%} + 0{,}12 \cdot \eta_{30\%} + 0{,}21 \cdot \eta_{50\%} + 0{,}53 \cdot \eta_{75\%} + 0{,}05 \cdot \eta_{100\%} \quad \text{Eq- 2}$$

that more precisely takes into account the operating conditions of PV systems in hot temperature regions. Common simulation tools have been used such as PSIM and SPICE and it has been assumed that the same type of transistor is used in all converters.

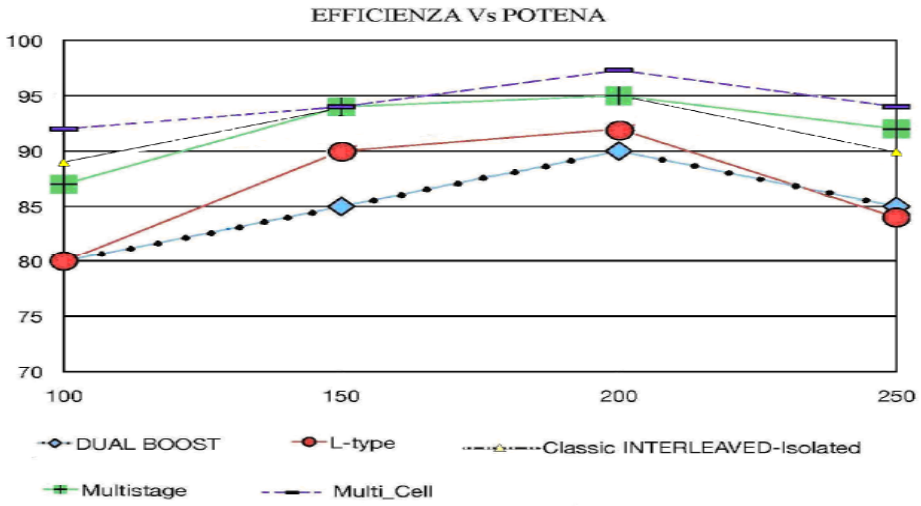


Fig. 13: Efficiency versus output power

Table 1

CRITERI	**1° Multiplier Cell**	**2° Multi Stage**	**3° Boost with transfromers**	**4° Boost transformers**	**5° Boost transformers**
Efficiency	97%	95%	90%	90%	95,4%
# switch	2	2	4	4	2
MAX Stress Voltage Switch	$V_{out}/4$	$V_{out}/4$	$V_{out}/2$	$V_{out}/2$	V_{out}/n
MAX Stress Current Switch	3In/4	3In/4	In/2	In/2	In/2
N° Diode	10	4	2	2	2
Stress Voltage Diode	$V_{out}/4$	$V_{out}/4$	2 V_{out}	2 V_{out}	2 V_{out}
Stress Current Diode	3In/4	3In/4	3In/4	3In/4	In/2n
Capacitor out	220 µF	220 µF	220 µF	220 µF	220 µF
L inducton	250 µH	250 µH	250 µH	250 µH	250 µH*2
Transformers	Yes	Yes+NS	Yes	Yes	Yes
Snubber	Yes	Yes	NO	NO	NO

The best topology has been selected after carefully investigation, taking into account several aspects. A standard Photovoltaic module is in the range of power 200W. In some country the standard asks galvanic isolation for grid-connected system. Efficiency, space, number of component, cost and life-time play a very important role in power electronics system.

All converters have been investigated in simulation, using the same transistor model for each of them. Fig. 13 shows the simulation result concerning efficiency versus output power. The classic interleaved shows quiet good performance in efficiency: the peak efficiency is around 95% for the nominal power, while for low level of load it is above 90%. The del Dual Boost efficiency is reported in the above figure #. It is easy to understand that the peak of efficiency is around 90 % for 200W load, while for low load condition the efficiency is quiet low, close to 80% of efficiency. The key points of the Dual Boost are: low voltage stress on the power devices and very high static gain. The L-type shows a better efficiency profile compared to the Dual boost for nominal power condition, while for low load condition the profile is very close to the dual boost. The Multi-Stage shows peak efficiency close to 95%. This converter presents very high static gain and low voltage stress on the power devices. The Multi-cell converter presents peak efficiency around the nominal power equal to 97%. The minimum efficiency is above 90%. The key points of this converter are: low voltage stress on the power devices, very high static gain and very high efficiency.

3.4 Prototype realization

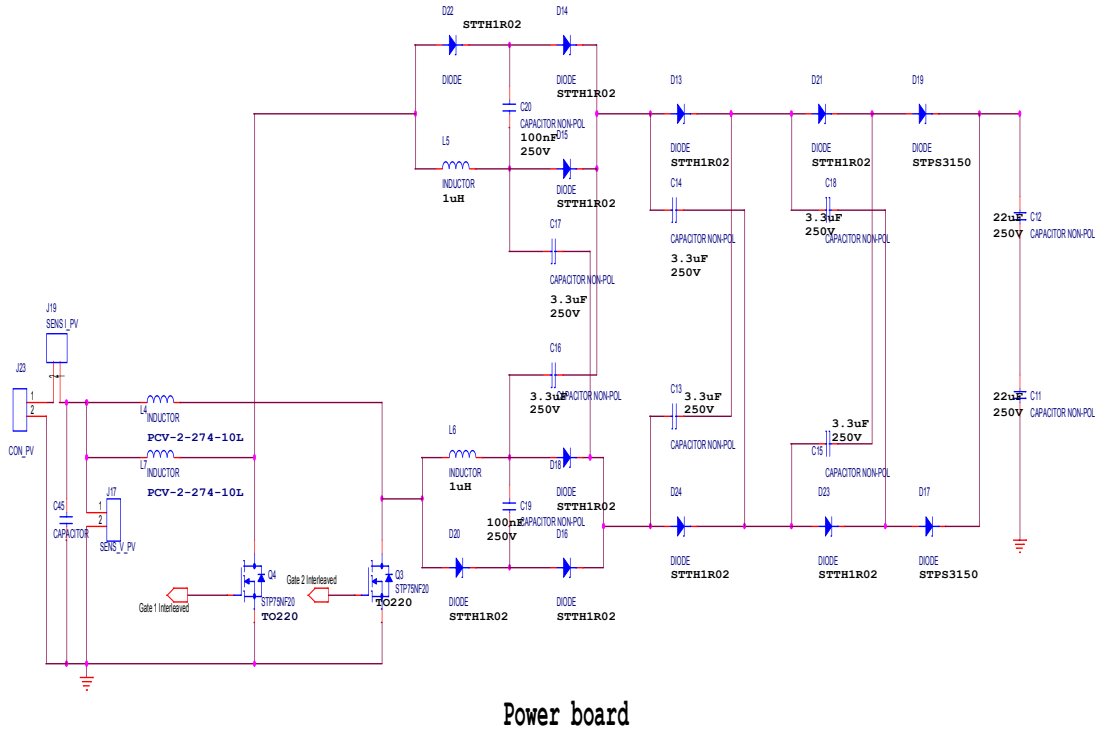
After deep consideration based on the simulation results a prototype of the best topology has been built. The Multi-Cell Converter whit three-and two stadiums has been chosen, which has shown very high performance for all the conditions, low load and full load, compared to other converters. The prototypes of converters have been design taking into account the same standard of the simulations. It has been tested at two different output voltage equal to 200 and 400 V. This choice is determined by the feasibility of a MIC for different markets, in fact, the bus voltage of 200 V is used to obtain the value of AC voltage of 110 V, normally used in the distribution plan, the bus voltage 400 to get that V AC to 230 V European markets. The load tests were performed at 10% 20% 30% 50% 75% and 100% of the maximum power of 250W. The test campaign has confirmed through SPICE simulations as shown in Figure 11.

Figures 12 and 13 and Table 2 shows the experimental results obtained. With regard to the European performance η_{CEC} the maximum value is 96.07% while the peak value is equal to

97.1% with three-stage multiplier, input voltage of 36 V and output voltage of 400V.

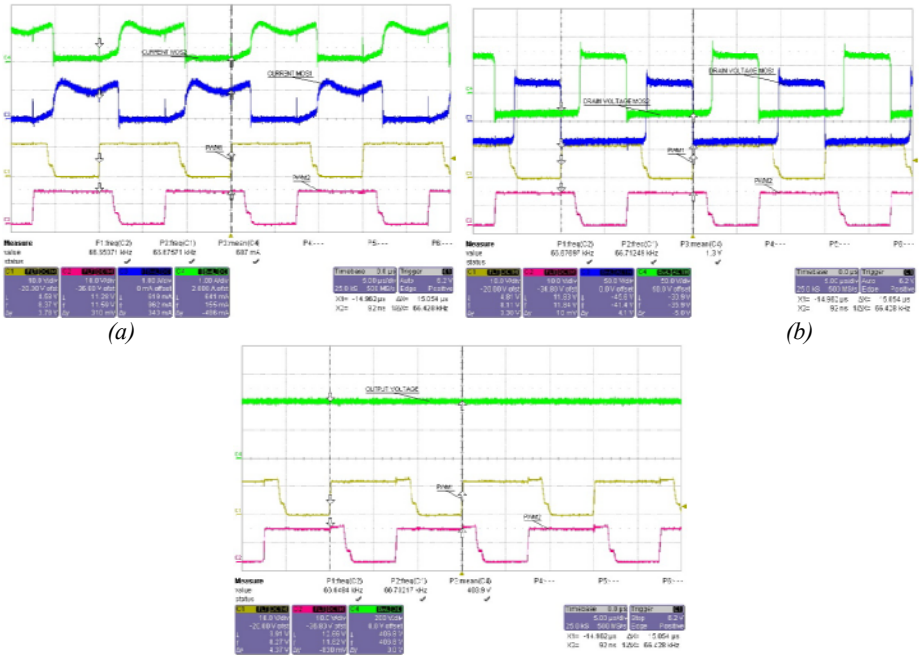
Table 2

Voltage Conversion	$M = \frac{V_{Out}}{V_{In}} = \frac{k+1}{1-D}$
Capacitor multiplier stage voltage	$V_{C\_MS} = \frac{V_{Out}}{k+1}$
Rect. Diodes multiplier stage Voltage	$V_{D\_MS} = \frac{2 \cdot V_{Out}}{k+1}$
Mosfet DS Voltage	$V_{M\_MS} = \frac{V_{Out}}{k+1}$
Boost diode Voltage	$V_{BD\_MS} = \frac{V_{Out}}{k+1}$



Power board

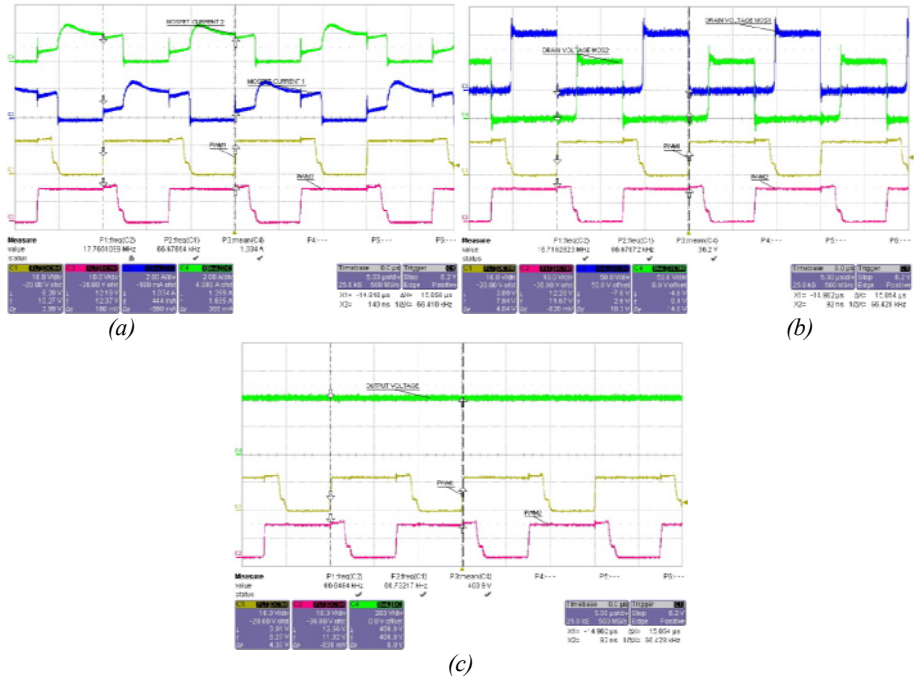
Fig. 14: PSpice Schematic ot the Multi-Cell Power Bord



(a) *(b)*

(c)

Fig. 15 Output power=50W; Output Voltage=350V; Switching Frequency= 50 kHz; Input Voltage=36V; *(a)* Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source current; Ch4 (Green): S2 drain-source current-*(b)* Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source Voltage; Ch4 (Green): S2 drain-source voltage-(c) Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch4 (Green): Output voltage.



(a) *(b)*

(c)

Fig. 16 OutputPower= 125W; Output Voltage=350V; Switching Frequency= 50 kHz; Input Voltage=36V; *(a)* Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source current; Ch4 (Green): S2 drain-source current-*(b)* Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source Voltage; Ch4 (Green): S2 drain-source voltage-(c) Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch4 (Green): Output voltage.

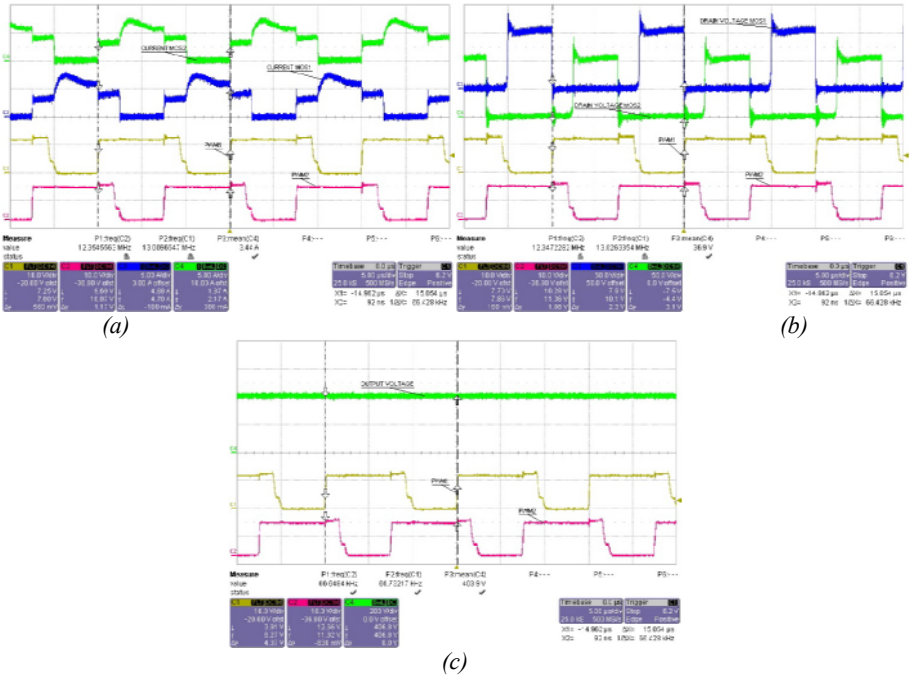


Fig. 17 Output power=250W; Output Voltage=350V; Switching Frequency= 50 kHz; Input Voltage=36V; (a) Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source current; Ch4 (Green): S2 drain-source current-*(b)* Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source Voltage; Ch4 (Green): S2 drain-source voltage-(c) Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch4 (Green): Output voltage.

Fig. 14 shows the power board realized. While Fig. 15, Fig. 16 and Fig. 17 show some waveforms of the prototype , respectively , for low load condition (50 W output power), medium load condition (125 W output power), and high load condition (250 W output power).

Table 3

Number of Cell / Vin / Vout	Peack Efficiency	CEC Efficiency
2 cells 24 Vin 400 Vout	94%	93%
2 cells 36 Vin 400 Vout	95%	93,8%
2 cells 24 Vin 200 Vout	95,9%	93%
2 cells 36 Vin 200 Vout	95,1%	94%
3cells 24 Vin 400 Vout	94,4%	93,6%
3 cells 36 Vin 400 Vout	97,1%	96,07%
3 cells 24 Vin 200 Vout	95,4%	92,2%
3 cells 36 Vin 200 Vout	96,63%	96,06%

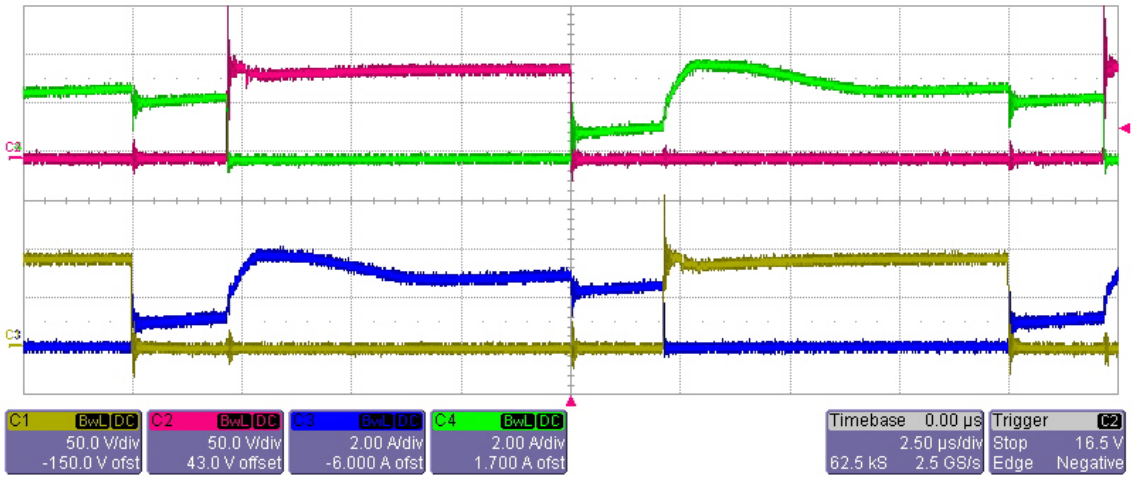


Fig. 18 Experimental results. Ch1 (Yellow): S1 Drain-Suorce Voltage; Ch2 (Red): S2 Drain-Suorce Voltage; Ch3 (Blue): S1 drain-source current; Ch4 (Green): S2 source current.

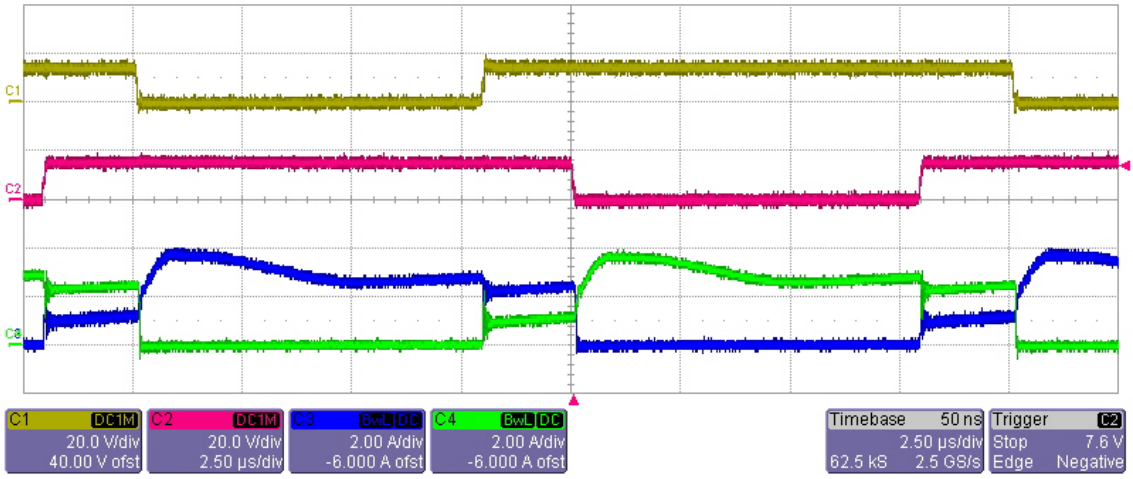


Fig. 19: Experimental results. Ch1 (Yellow): S2 gate-voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source current; Ch4 (Green): S2 source current.

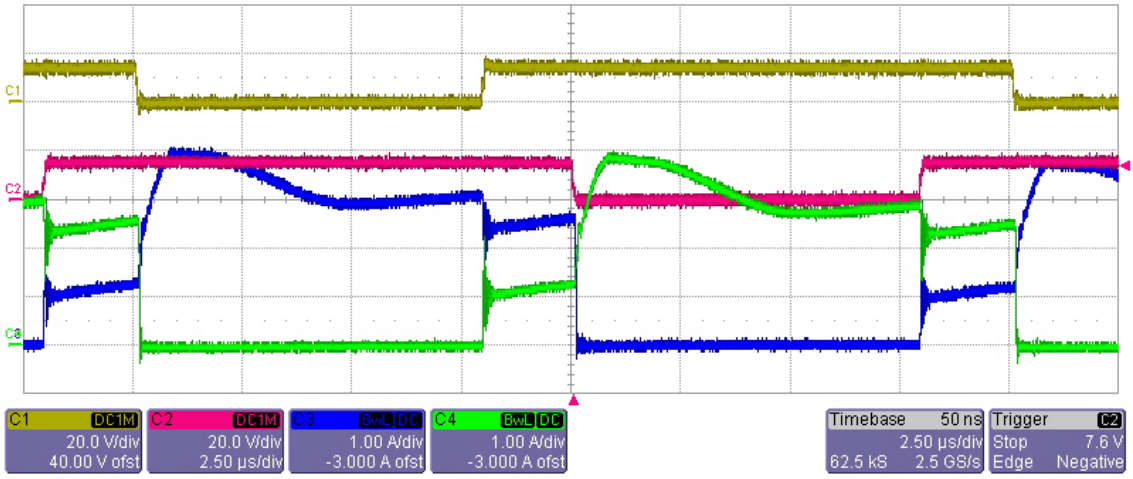


Fig. 20: Experimental results. Ch1 (Yellow): S2 gate-voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source current; Ch4 (Green): S2 source current.

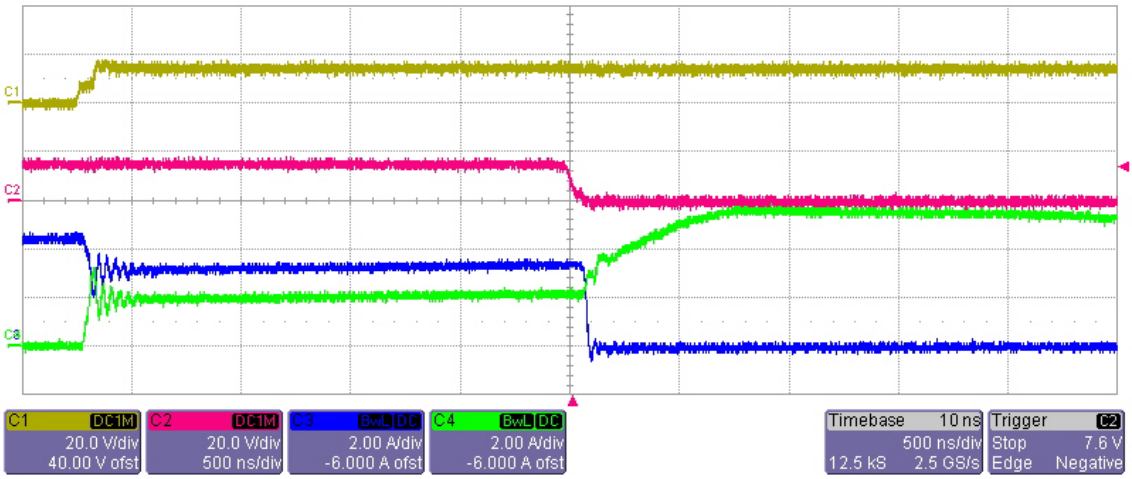


Fig. 21: Experimental results. Ch1 (Yellow): S2 gate-voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source current; Ch4 (Green): S2 source current.

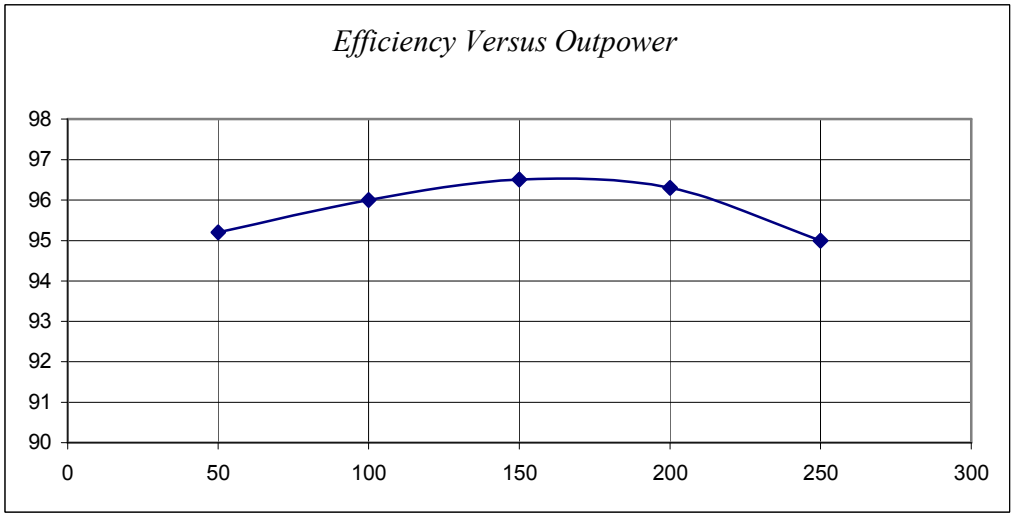


Fig. 22: Effciency versus Power for 3 stage and 24 V input voltage and 200 V output voltage

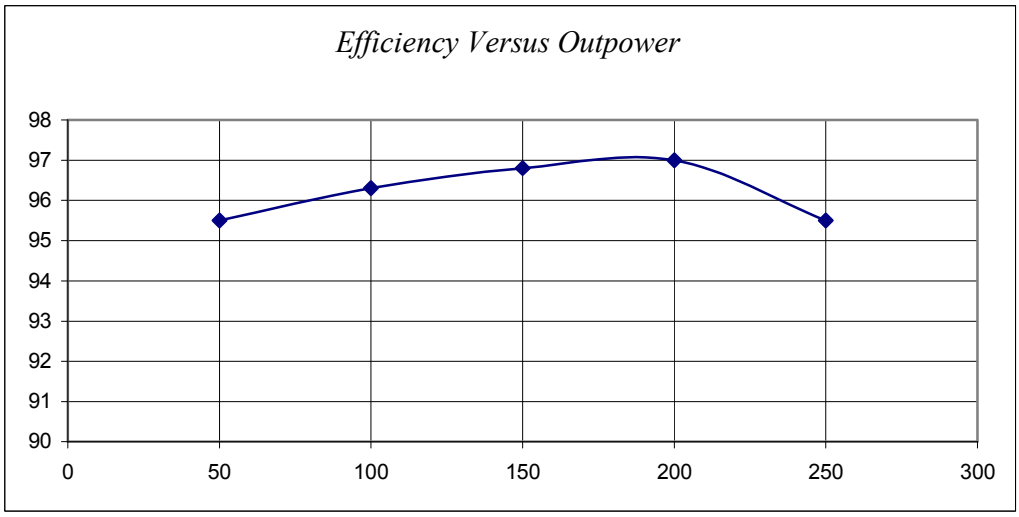


Fig. 23: Effciency versus Power for 3 stage and 36 V input voltage and 400 V output voltage

In Table 3 the peak efficiency and the CEC efficiency has shown. It is evident that the best efficiency is get for 36 V as a input voltage and 400 V as output voltage. Fig. 18, Fig. 19, Fig. 20 and Fig. 21 show some waveforms of the main parameters of the prototype. Fig. 22 and Fig. 23 shows the Efficiency versus output power , respectively, for the Prototype with 3 cells at 24V input voltage and 200 V output voltage and the same prototype at 36 V as input voltage and 400V as output voltage

3.5 Summary

In the field of grid-connected photovoltaic applications of power less than a few kW, is establishing a new solution for converting energy from direct current to alternating. This technique is to use single DC / AC power equal to that of the photovoltaic panel and installed directly on the back of it. In this article were discussed advantages and disadvantages of doing so. In particular, several circuit solutions have been reviewed by the panel for these converters. The topologies considered were analyzed in the simulation, draw up a list of potential performance and structural complexity.

From the simulation results the best topology has been selected and built. The experimental tests on the prototype have confirmed the validity of the solution.

Chapter 4

String Converter for Photovoltaic modules

This chapter proposes a new high gain converter tailored for low-power photovoltaic (PV) systems. First, a comparison between the most suitable high gain converter and a new topology is presented.

This new structure is based on an improved interleaved boost converter. Here, an additional winding is added to the autotransformer to provide not only the required high gain but also to significantly reduce the voltage stress across the active switches. A prototype for the verification of the circuit was built for a 30–45-V input-voltage range, 400-V output voltage, and 250-W output power. The operation is evaluated, and the experimental waveforms and efficiency curves are presented

4.1 High voltage gain DC/DC converter topology

Considering that efficiency maximization and high voltage gain are the two most important issues in ACM applications, many solutions have been proposed in the past addressing both problems. As for the high voltage gain, it can be obtained through topologies using High Frequency (HF) transformers or charge-pump circuits. If galvanic isolation is not requested, the second solution is more attractive as it avoids the transformer losses.

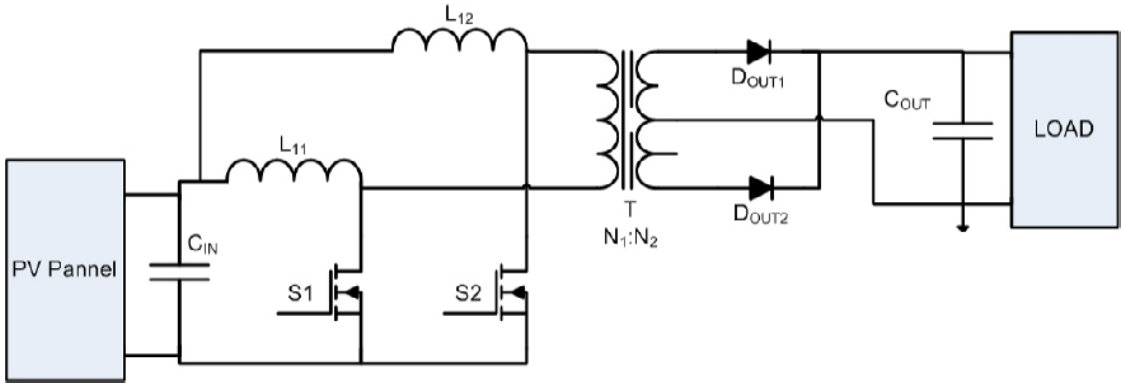


Fig. 24: Scheme of interleaved boost converter with HF transformer

In the literature, many topologies have been presented [10][11][12][13][14]. Following, a new solution, suitable for such system, is presented and compared with the existing ones according to the number of power devices, rated power and weighted conversion efficiency. A detailed description of the inverter is presented in the following sections. First, the power electronic topology is introduced.

4.1.1 Interleaved Boost with HF Transformers

In Fig. 24 is shown the scheme of a two-channels interleaved boost converter with HF transformer. The transistors S_1 and S_2 are switched at the same frequency with the same duty cycle but their gate signals are shifted by 180°. Usually, a snubber must be added in order to reduce the overvoltage at the switch turn-off, but it negatively affects the efficiency. To solve such a problem, some solutions have been presented in the literature, as the active clamp circuit presented in literature, such as the active clamp circuit.

4.1.2 Multi-Stage Converter

In Fig. 25 is shown the scheme of the Multi-Stage converter. The basic structure is similar to the classical interleaved boost, but an autotransformer is used between the two phases. The high gain is obtained using an auxiliary winding coupled with the autotransformer to equalize the voltage across the output filter capacitors [15][16][17].

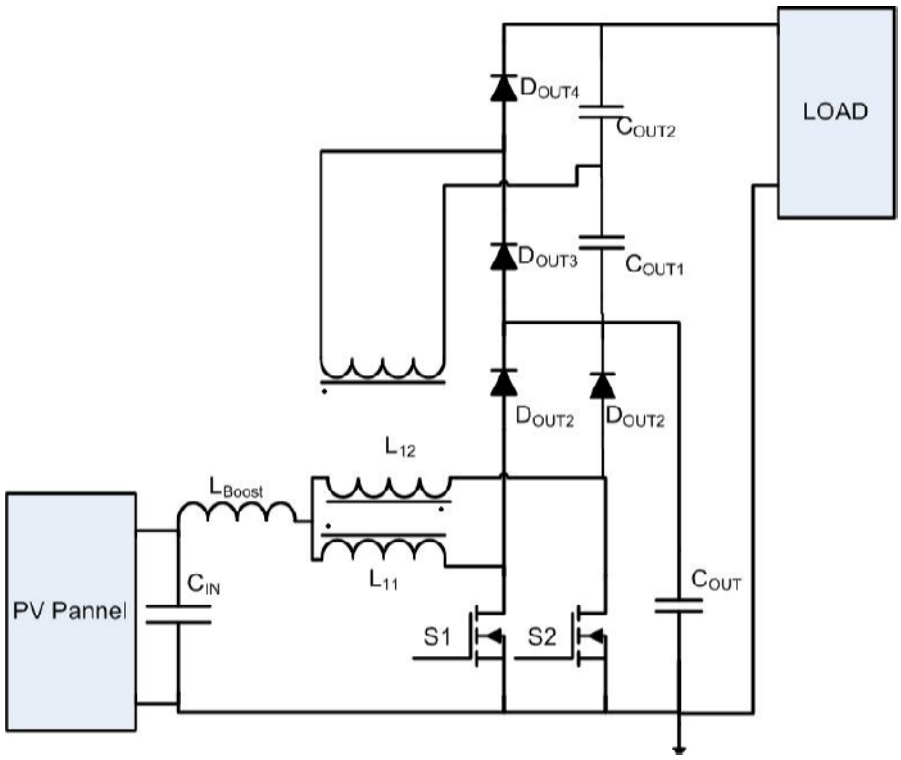


Fig. 25: Scheme of Multi-Stage converter.

4.1.3 Multi-Cell Converter

A topology based on the interleaved boost converter using a Multi-Cell structure is shown in Fig. 26. The number of interleaved stages can be increased, providing the advantage of reducing conduction losses in the power devices (e.g. switches and diodes). As a remark, a snubber circuit may be required in order to decrease the turn-on losses of switches S_1 and S_2 caused by the amount of the reverse recovery currents of the output and the multi-cell diodes [18][19][20].

4.1.4 Interleaved Charge-Pump Converter

The scheme of the proposed converter is shown in Fig: 27. It is based on a two channel interleaved boost topology where the input inductance is connected in series with the coupled inductors of the two channels. The main switches are connected to the common point of each coupled inductors and the ground.

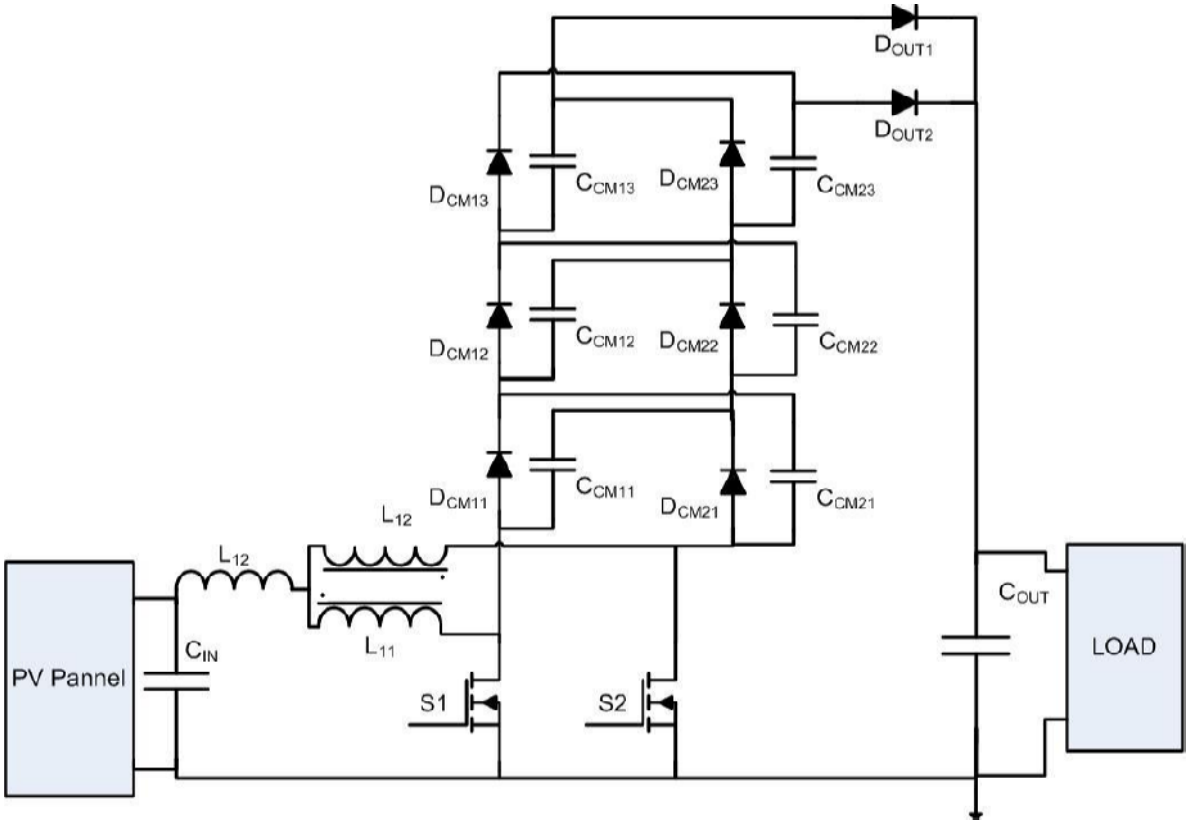


Fig. 26: Scheme of Multi-Cell converter

The proposed converter consists of two active switches (S_1 andS_2), two inductors (L_{11} and L_{21}) that have the same level of inductance, one boost inductance L and other two inductors

(L_{22} and L_{12}) magnetic coupled with L_{11} and L_{21} and a charge pump structure. The inductor L_{11} of the first channel is coupled with L_{12}, which is in series with C1 and connected to the other phase by the diode D_2. Such a circuit is a charge pump stage. S_1 and S_2 are controlled simultaneously by using one interleaved PWM control signal.

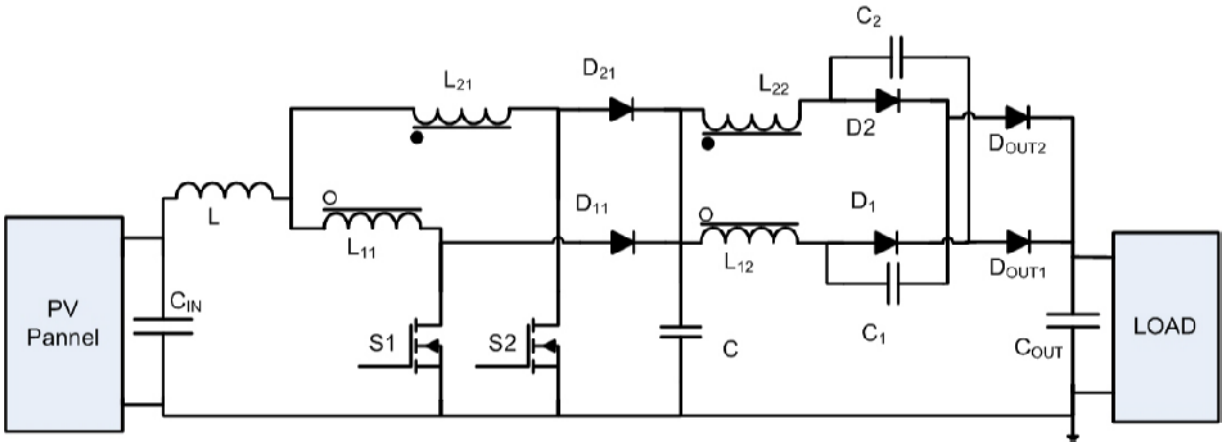


Fig: 27 Scheme of the proposed converter

4.1.5 Analysis of the ACModule

A comparison of the characteristics of the considered converters is reported in Table 4. The efficiency is evaluated following the California Energy Commission (CEC) index, shown in equation (e). This index is more accurate than the European (EU) one for PV systems installed in hot temperature regions.

$$\eta_{CEC} = 0{,}04 \cdot \eta_{10\%} + 0{,}05 \cdot \eta_{20\%} + 0{,}12 \cdot \eta_{30\%} + 0{,}21 \cdot \eta_{50\%} + 0{,}53 \cdot \eta_{75\%} + 0{,}05 \cdot \eta_{100\%} \quad \text{Eq. 3}$$

CEC efficiency has been calculated by simulations performed with PSIM and SPICE. The same power devices have been used for each topology under analysis. It can be noted that, for the proposed solution, the voltage-stress applied on the power devices is lower compared to that shown by the other topologies.

Consequently, very low breakdown voltage power devices can be used, allowing large power losses reduction both in switching and conduction states.

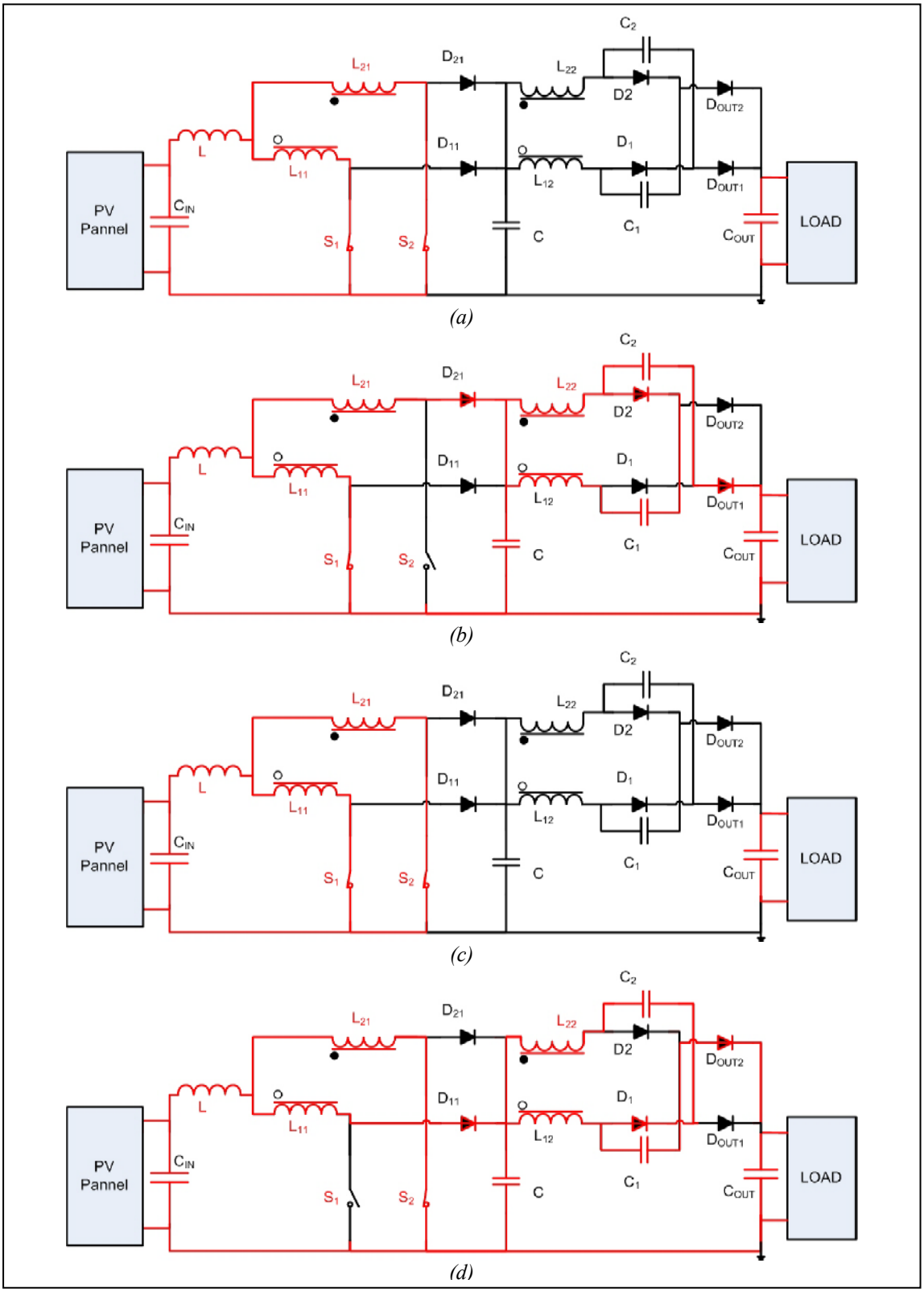


Fig. 28: Operation analysis of the proposed converter.

Table 4

	Main characteristics of DC/DC converters			
	Interleaved	Multi-Stage	Multi-Cell	Interleaved Charge-Pump
Switches Voltage	Vout/2N	Vout/4	Vout/4	Vout/(N+M)
Switches Current	In/2	In/2	In/2	In/2
# of Power Devices	4	6	10	8
Magnetic Component	2 inductor	1 trafo and 2 inductor	2 coupled inductor	2 coupled inductor
Efficiency (CEC)	94%	95%	96%	96,3%

4.2 Operation analysis of the proposed converter

In order to explain the converter operation, a steady state analysis has been performed through simulation. According to the simulated voltages and currents shown in Fig. 29, a switching period can be divided in four time intervals corresponding to the different configurations shown in Fig. 28. The operating principles and steady state analysis are presented in detail as follows:

a) First Interval [t_0 ~t_1] (Fig. 28 (a)): Before t_0, only the switch S_2 is in ON state. At t_0 the switch S_1 is turned-on. The energy is stored in the inductor $L+(L_{11}//L_{21})$. There is no current flowing through L_{11} and L_{21}. The load is supplied by the output capacitor, according to Fig. 28 (a). Such a period stops when S_2 is turned-off.
b) Second Interval [t_1 ~t_2] (Fig. 28 (b)): At t_1 the switch S_2 is turned-off, while S_1 remains on. The magnetizing inductance $L+L_{11}$ is charged by the source. The capacitor C is supplied through the inductor L_{21}. The diode D_{12} is forward biased. The capacitor C_1 is supplied through L_{22} (coupled with L_{21}). During this interval C_2 feeds the load trough the diode D_{out2}.
c) Third Interval [t_2 ~t_3] (Fig. 28 (c)): during this interval the converter behaviour is similar to that of the first one, where S_1 remains on and S_2 is turned on. The energy is stored in the inductance $L+(L_{11}//L_{21})$. The load is supplied only by the output capacitor.
d) Fourth Interval [t_3 ~t_4] (Fig. 28 (d)): starting at t_3, the switch S_1 is turned-off, while S_2 remains on. The magnetizing inductance $L+L_{22}$ is charged by the source. The capacitor C is supplied through the inductor L_{11}. The diode D_{11} is forward biased. The capacitor C_2 is

supplied through L_{12} (coupled with L11). C_1 transfers energy to the load trough the output diode D_{out1}.

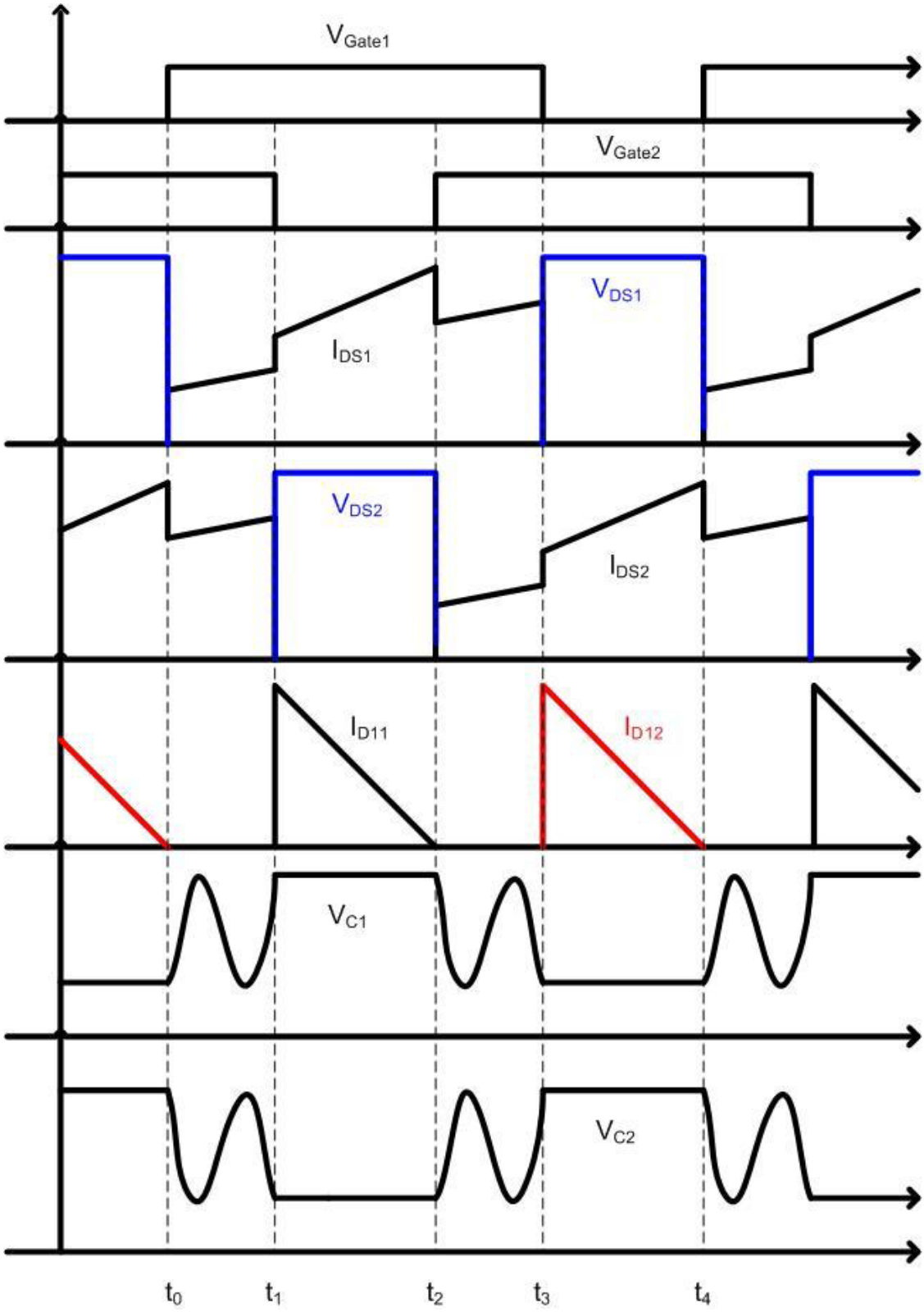


Fig. 29: Wave forms of the proposed converter.

4.2.1 Theoretical analysis

The static gain of the proposed converter operating in continuous conduction mode is shown in equation (2). This equation is also valid for operation with δ>0.5:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{(1 + N \cdot \delta + M)}{(1 - \delta)} \quad \text{Eq. 4}$$

where M is the number of multi-cell stages; δ is the duty cycle and N is the turn ratio of the coupled inductor. According to the equation (4), the gain obtained by the proposed converter can be expressed as a function of the duty cycle and turn ratio, respectively, with one with one Fig. 30 (a), two Fig. 30 (b), or three Fig. 30 (c), multi-cell stages.

The maximum voltages applied to the power switches (S_1 and S_2) and the output diodes (D_{OUTl} and D_{OUT2}) are equal to the multiplier capacitor voltage. The maximum voltage of such components is equal to:

$$V_{DSMax} = \frac{V_{IN}}{(1 - D)} \quad \text{Eq.5}$$

The maximum voltage applied to the multiplier diodes is twice the multiplier capacitor voltage, even if configurations with more than one multiplier stage (M>1) are considered.

$$V_D = \frac{V_{IN}}{(1 - D)} \cdot 2 \quad \text{Eq.6}$$

As for the rated power P_O and the converter efficiency, the input current is calculated in equation (7), while the rms current value of the switches is given by equation (8), where P is the number of the stages connected in parallel [20]:

$$I_{IN} = \frac{P_o}{(V_{IN} \cdot \eta)} \quad \text{Eq.7}$$

$$I_{S_{rms}} = \frac{I_{IN}}{P} \cdot \sqrt{\frac{5 - D}{4}} \quad \text{Eq. 8}$$

The RMS switch current is calculated by the equation 8, considering the operation with D>0.5 and two parallel stages.

The average current in each diode is reduced by the number of parallel (P) and series stages, as it can be seen in equation 9:

$$I_D = \frac{I_{IN} \cdot (1 - D)}{P \cdot (M + 1)} \qquad \text{Eq. 9}$$

the diode average current is reduced with the increment of the parallel stages (P) and with the number of multiplier stages (M). Therefore, the increment of the number of diodes 'does not increase the diode conduction losses because the average current of each diode is proportionally reduced [21][22][23][24][25].

4.3 Experimental Result

In order to experimentally evaluate the performance of the proposed converter a prototype has been built considering the following specifications:

Table 5

Parameters Design	
Vin	20~36V
Pout	200W
Vout	400V
fs	100kHz

Inductances have been calculated through equation 10 by fixing the current ripple on the boost inductors equal to ΔI=10%•IinMAX and, according to the voltages required by the application, the turn ratio n has been chosen equal to one.

$$L_{11} = \frac{V_{IN}}{N_S \cdot \Delta I_L \cdot f_s} \approx 100\mu H \qquad \text{Eq. 10}$$

The values of the capacitors C1 and C2 can be calculated from equation 11, considering a voltage ripple equal to 10V and the minimum duty cycle equal to 0,5 [21].

$$C_1 = C_2 = \frac{I_{IN} \cdot (1 - D)}{N_S \cdot (M + 1) \cdot \Delta V_C \cdot f_s} \approx 2\mu F \qquad \text{Eq. 11}$$

In Table 6 are reported the main characteristics of the adopted power devices.

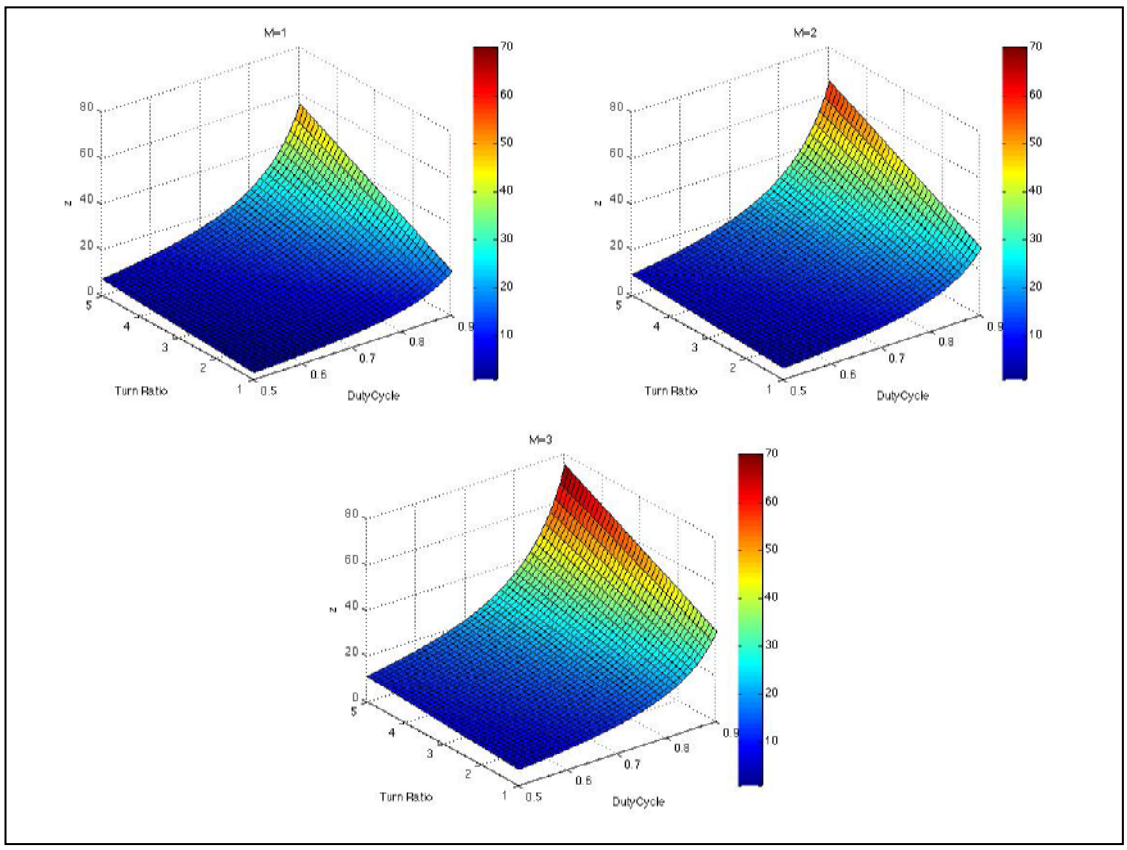


Fig. 30.: Voltage gain of the proposed converter as a function of duty cycle and turn ratio obtained with 1 (a), 2 (b) and 3 (c) Multi-cell stages.

Table 6

Characteristics of power devices	
D1 D2	Ultra Fast Diode 3A 200V
D11 ,D12	SiC Diode 4A 600V
Dout1, Dout2	Power Schottky Diode 3A 150V
S1 S2	PowerMOSFET 40A 200V

The experimental results obtained using the developed prototype are reported in Fig. 31 - Fig. 38, showing the correct behaviour of the prototype Fig. 31 shows the boost inductor current and the drain-source current for each power devices (S_1 and S_2). Fig. 32 shows drain-source current for each power devices (S_1 and S_2), gate-source voltage of S_1, and the drain-

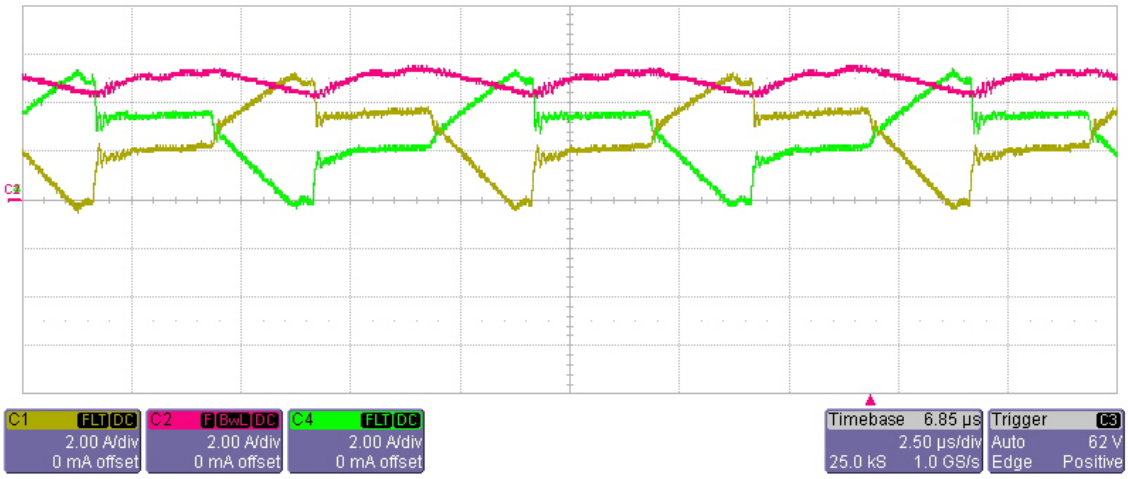


Fig. 31: Experimental results. Ch1 (Yellow): S2 source current; Ch2 (Red): L boost current; Ch4 (Green): S1 source current.

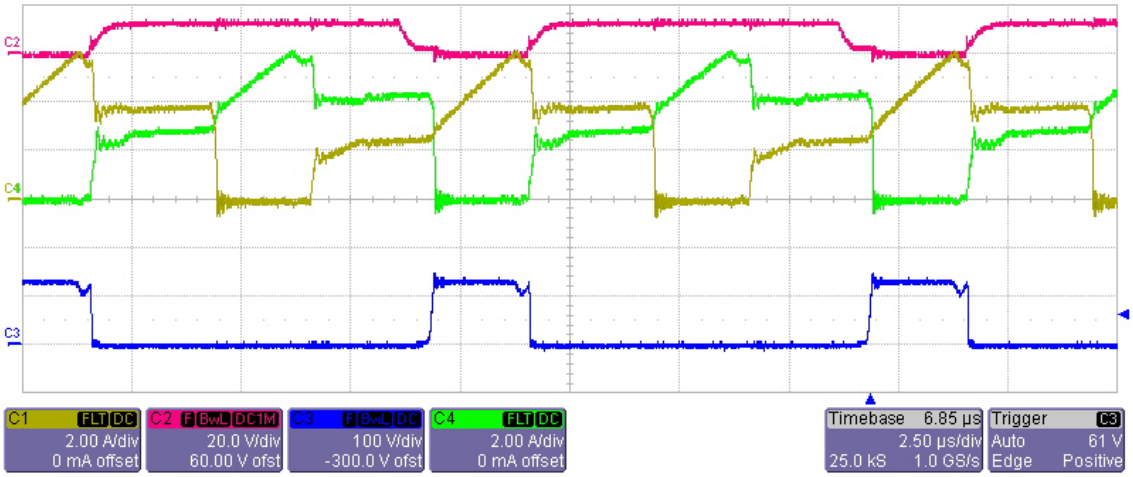


Fig. 32: Experimental results. Ch1 (Yellow): S2 source current; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source voltage; Ch4 (Green): S1 source current.

source voltage of S_1. Fig. 34 and Fig. 34 show gate-source voltage of S_2, gate-source voltage of S_1, drain-source voltage of S_1 and drain-source current of S1 and its zoom. Fig. 35 shows the behaviour of the diode-boost (D_{11} and D_{21}) current and the drain-source voltage on the power devices (S_1 and S_2).

It was observed by simulation and in the practical implementation that the current and voltage sharing in the switches and diodes are dependent only of the symmetry of the switch duty-cycle. Asymmetries of intrinsic parameters of the circuit as inductance, does not change the current or voltage sharing.

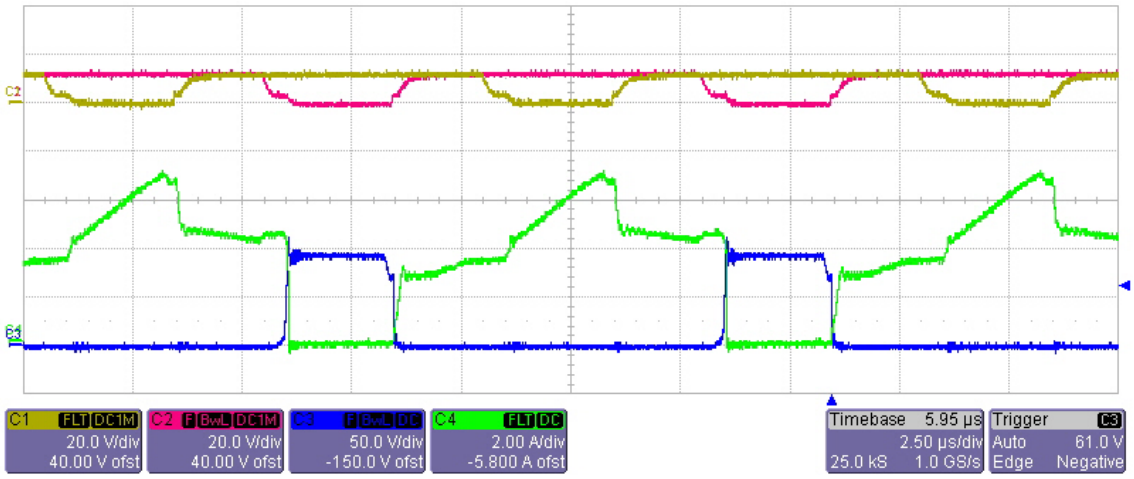


Fig. 33: Experimental results. Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source voltage; Ch4 (Green): S1 source current.

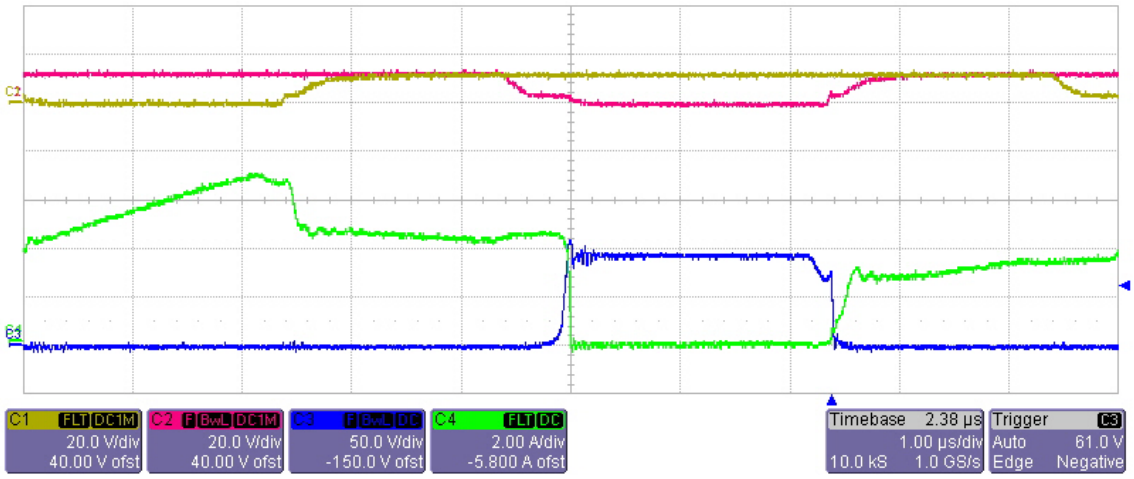


Fig. 34: Experimental results. Ch1 (Yellow): S2 gate-source voltage; Ch2 (Red): S1 gate-source voltage; Ch3 (Blue): S1 drain-source voltage; Ch4 (Green): S1 source current.

In order to test the impact of SiC diodes on the converter efficiency, the diodes D_{11} and D_{21} of the prototype has been replaced with SiC type. The time sketches are shown in Fig. 36 and Fig. 37. Comparing the negative current area, proportional to the diode reverse recovery charge Q_{rr}, it is evident that the higher is the switching frequency the bigger are the switching losses. In particular, for the proposed converter SiC diodes show a reduction of the total losses equal to 0,4W compared with standard “ultra-fast”. In Fig. 38, the voltages on capacitors C_1 and C_2 are shown.

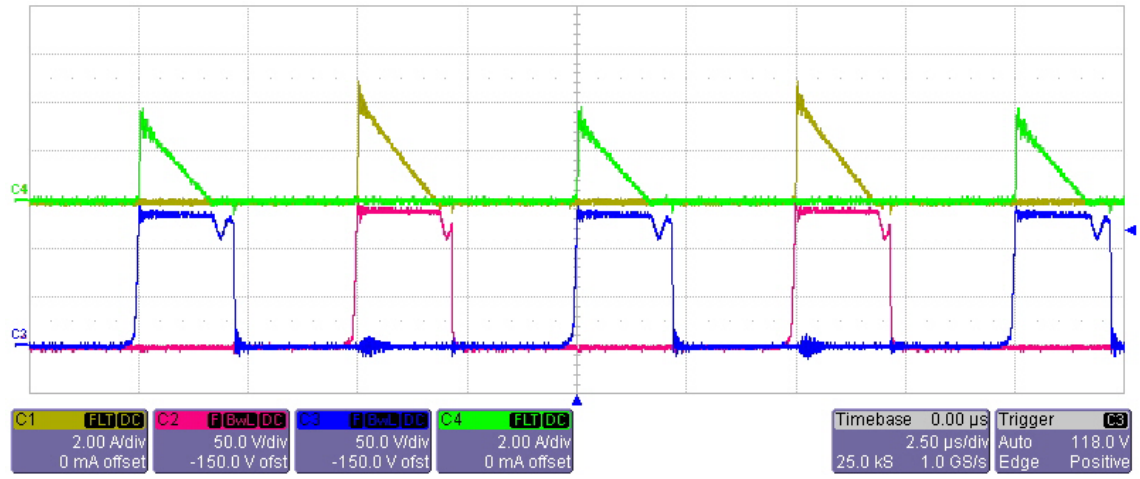


Fig. 35: Experimental results using Fast-Diode: Ch1 (Yellow) Diode current (D_{21}). Ch2 (Red) S_2 drain-source voltage; Ch3 (Blue) S_1 drain-source voltage; Ch4 (Green) Diode current (D_{11}).

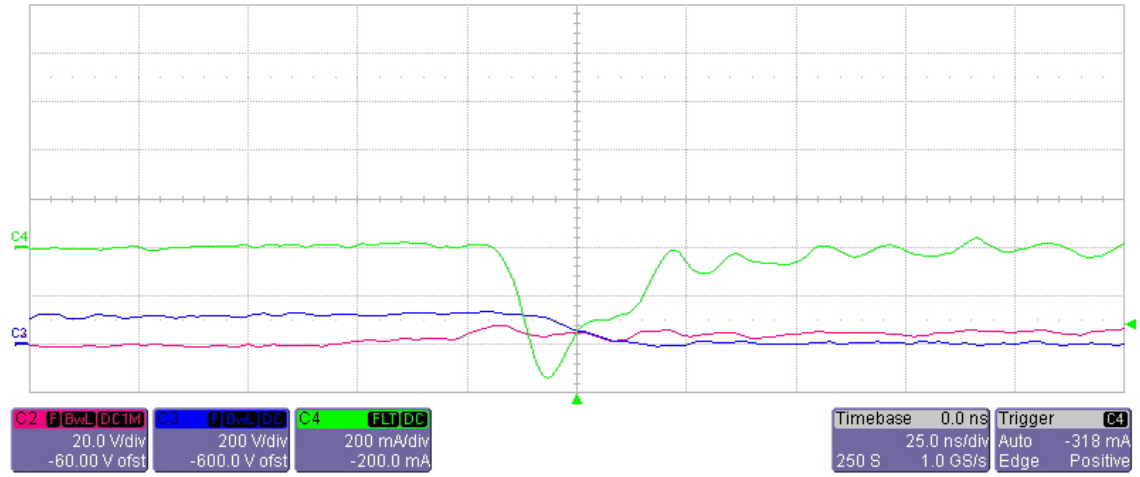


Fig. 36: Experimental results using Fast-Diode: Ch2 (Red) S_1 gate-source voltage; Ch3 (Blue) S_1 drain-source voltage; Ch4 (Green) Diode current (D_{11}).

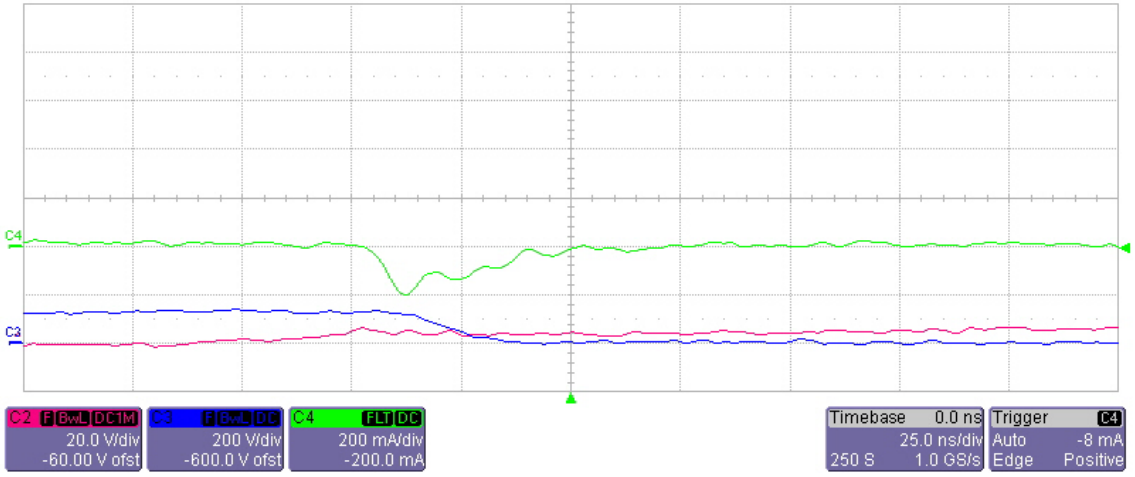


Fig. 37: Experimental results using SiC-Diode: Ch2 (Red) S_1 gate-source voltage; Ch3 (Blue) S_1 drain-source voltage; Ch4 (Green) Diode current (D_{11})**.**

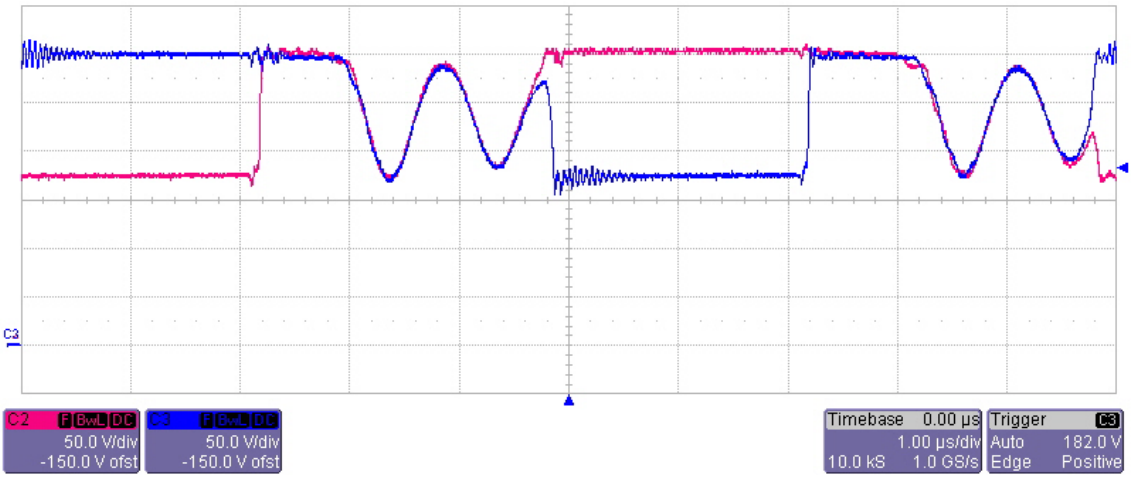


Fig. 38: Experimental results: Ch3 (Red) C_1voltage; Ch4 (Blue) C_2 voltage

Table 7 *Measured efficiency*

Input Voltage	Output Voltage	$\eta_{MAX\%}$	$\eta_{CEC\%}$
20	200	95,0	95,5
25	200	95,4	94,8
30	400	97,0	96,2
36	400	96,0	95,0

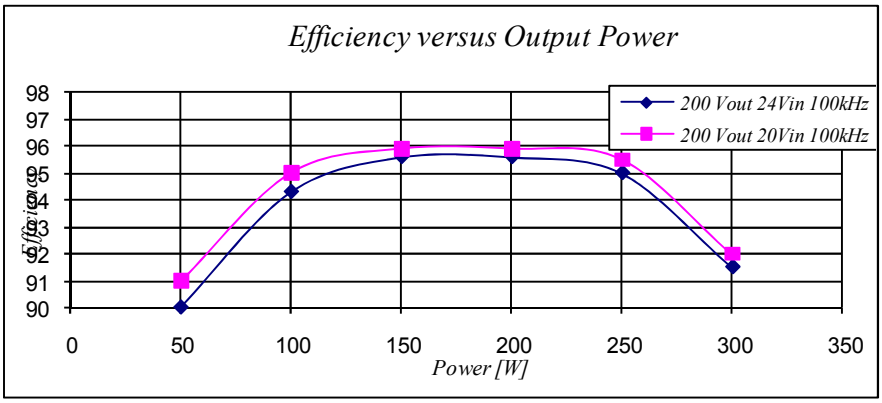


Fig. 39: Efficiency at 200V output. Input 24V (red), 20V (blue).

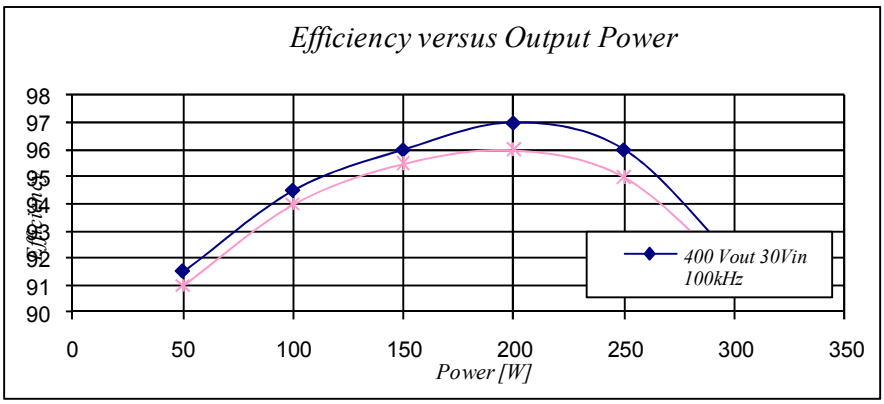


Fig. 40: Efficiency at 400V output. Input 30V (blue), 36V (red).

The figures of merit of the converter are shown in Fig. 39 and Fig. 40, while in Table 7 are reported the measured maximum and ECE efficiency. Such measurements have been performed considering the European and US grid standards, as well as different PV modules. The experimental results of the prototype confirm that the proposed converter is a very good alternative to the standard high gain converter. . The obtained efficiency is quite high in a wide range of input voltage and output power with a maximum up to 96%.

Fig. 40 shows the efficiency curve of the circuit presented in Fig: 27 for two different input voltage: 30V and 36V. The efficiency reached at the nominal load for a input voltage of 30 V and 36V is equal to 97% and 96% respectively.

4.4 Summary

In this chapter, a review of high voltage gain DC/DC converters has been presented focusing on single module photovoltaic application. Then, a novel topology has been introduced and the converters performances have been compared trough simulations and design considerations. The proposed solution shows the highest efficiency and lowest voltage stress on the active devices.

The proposed converter is a suitable choice for renewable energy applications, and it also can be extended to other power conversion systems where a high DC bus voltage is needed.

The proposed structure allows to operate with large step-up conversions ratio, without a transformer and also maintain low voltage and current stress in the switches and diodes. The proposed converter presents high efficiency (97%) due to low voltage and current stress and low commutation losses. The modularity of the structure allows the increment of the current,

voltage and power levels, using the same range of components and maintaining high efficiency, only increasing the number of series stages or increasing the ration of the coupling inductors. The experimental results confirm the basic operation of the converter and theoretical analysis developed

Part II

Control of Single-Phase DPGS

Chapter 5
Control of Single Phase Inverter for grid connection

In this chapter the issue of control strategies for single-stage photovoltaic (PV) inverter is addressed. A short overview of control system is presented with focus on the main elements of the grid-connected system: maximum power point tracker (MPPT), synchronization method, power control, anti-islanding detection.

5.1 Introduction

A controller is a subsystem or a process assembled for the purpose of controlling the output of a system such as a switching mode converter. The control strategy applied to the grid-connected converter, basically, is composed by four blocks:

- MPPT
- Grid angle estimation
- Anti-Islanding
- Power Management

5.2 Maximum Power Point Tracking

The power delivered by the PV module depends on the irradiance, temperature, and shadowing conditions. It is well known that PV generators have non linear P-V and I-V characteristics that depend on the condition of the PV array. So, as it is aforementioned in chapter 2, the output characteristics of a photovoltaic array with solar irradiation and cell's temperature show that different levels of power and current can be achieved from a particular

unit. The power has a Maximum Power Point (MPP) at a certain working point, with coordinates V_{MPP} voltage and I_{MPP} current. Since the MPP depends on solar irradiation and cell temperature, it is never constant over time; thereby Maximum Power Point Tracking (MPPT) should be used to track its changes. At every instant, each PV field shows its own maximum power that can be delivered to the load or the grid. Such an operating condition is indicated as the Maximum Power Point (MPP) of the PV generator. Because the MPP changes time by time during the day and through the year, a suitable power harvesting action must be performed continuously by the power electronic converter that interfaces the PV generator to the load, setting its operating point in a manner that allows the modules to produce all the power they are capable of. Then, a control tracking algorithm must be developed able to follow the MPP of the PV field, that is the Maximum Power Point Tracking (MPPT) algorithm [27][28][29].

5.2.1 Maximum Power Point Tracking Algorithms overview

In recent years, to extract maximum power a large number of techniques have been proposed and reported in literature. Fractional open-circuit voltage and short-circuit current strategies provide a simple and effective way to acquire the maximum power. They are based on the approximately linear relation existing under varying irradiance and temperature levels, respectively between the voltage of the PV generator at the MPP and its open-circuit voltage, and between the current of the PV generator at the MPP and its short-circuit current. The proportional constant depends on several parameters such as the fabrication technology, solar cells technology, fill factor, and atmospheric conditions. Although simple, these methods require periodical disconnection or short-circuit of the PV modules to measure the open-circuit voltage or the short-circuit current for reference, resulting in more loss of power. In addition, the number of components and cost are increased as in the power converter an additional switch is usually adopted to short the PV array periodically and measure the short-circuit current through a current sensor. Perturb and observe (P&O) and hill climbing methods

Table 8

MPPT	MPP reaching	Analog or Digital	Implementation Complexity	Sensed Parameters	Convergence Speed	Cost
Hill Climbing and P&O	yes	both	low	Voltage and Current	Varies	Medium
Incremental Conductance	yes	Digital	medium	Voltage and Current	Varies	Higher

Constant Voltage	yes	both	low	Voltage	Varies	Low
RCC	yes	Analog	low	Voltage and Current	Fast	Medium
Current sweep	yes	Digital	high	Voltage and Current	Slow	Medium
dP/dV Feedback control	yes	Digital	medium	Voltage and Current	Fast	Medium
Fractional Voc / Isc	no	both	low/medium	Voltage / Current	Medium	Medium

are widely applied in MPPT controllers due to their simplicity and easy implementation. P&O method involves a perturbation in the operating voltage of the PV array, while hill climbing strategy introduces a perturbation in the duty ratio of the power converter and is more attractive due to the simplified control structure. Incremental Conductance (InC) method, which is based on the fact that the slope of the curve of the PV array power vs. voltage is zero at the MPP, has been proposed to improve the tracking accuracy and dynamic performance under rapidly varying conditions. However, steady state oscillations still exist and the algorithm is a little more complicated compared to P&O/hill climbing strategies. P&O and hill climbing MPPT methods are the most commonly employed in practice. Their performance have been evaluated and compared through theoretical analysis and digital simulation showing that the P&O method exhibits fast dynamic performance and well regulated PV output voltage, which is more suitable than hill climbing method for grid-connected PV systems. The (Constant Voltage) CV method is based on the fact that generally the ratio V_{MPP}/VO_{0C} is equal to 0,76. A comparison of the several MPPT methods most commonly adopted is shown in Table 8.

In Fig. 41, is graphically shown how the methods act in order to reach the MPP set point: the P&O climbs the power curve until the system remains cycling in operating points across the MPP, while the InC algorithm acts incrementing or decrementing the operating point of the system according to the sign of the derivative of the power curve until its slope is zero.

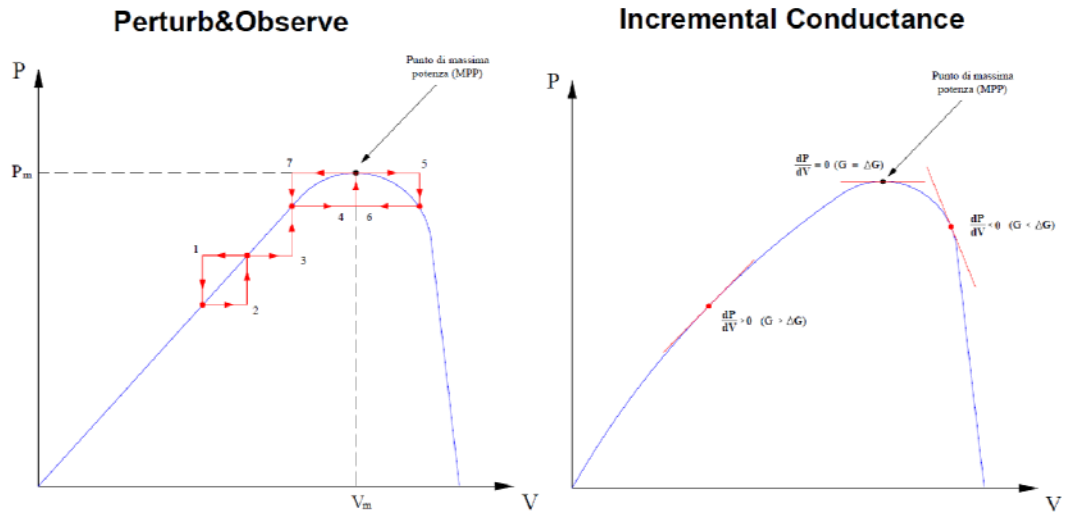


Fig. 41: Operation of two MPPT algorithms.

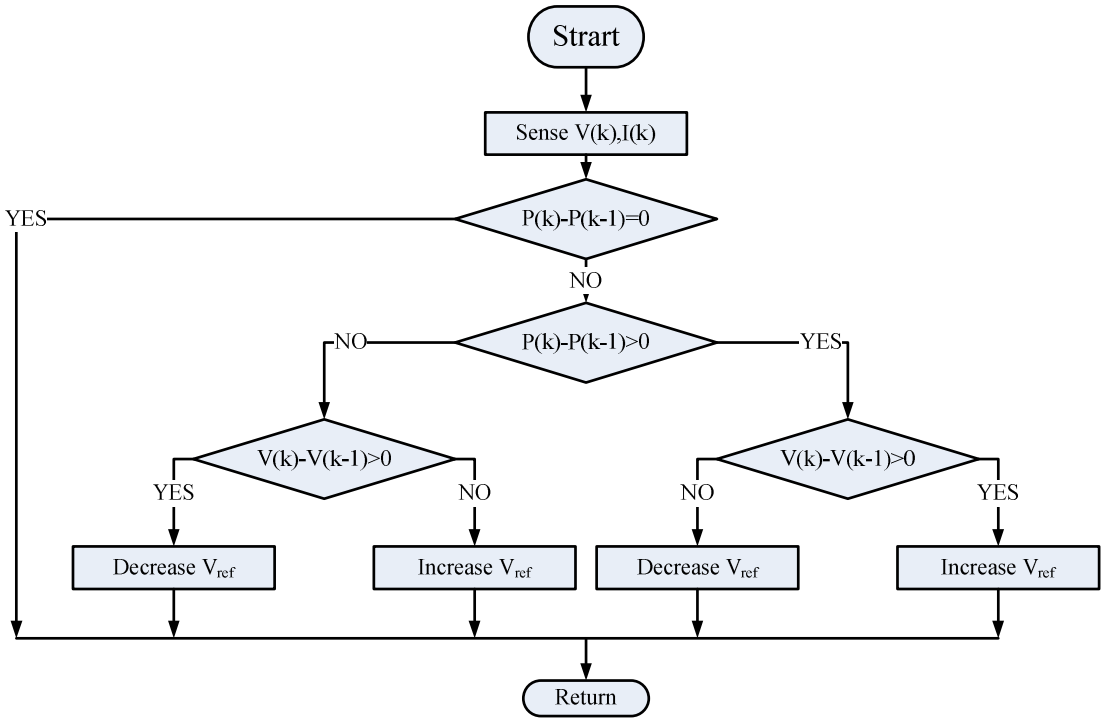


Fig. 42: Flow chart of P&O MPPT algorithm

The P&O method is easy to implement but there are always oscillations of the working point that, on the contrary, are avoided by the InC method. Unfortunately, the InC technique requires more computation resources.

The InC method uses the PV array's incremental conductance ΔI/ΔV to compute the sign of the ΔP/ΔV. The MPP condition is achieved when ΔP/ΔV=0 and ΔI/ΔV=0 then the system is not perturbed anymore. If such conditions are not satisfied, the system will be perturbed using the relationship between ΔI/ΔV and I/V. The InC is able to track the fast variations of

irradiance conditions with higher dynamics than P&O. However, because of noise and errors due to measurement and quantization, this method also can produce oscillations around the MPP. Moreover it can fail in rapidly changing atmospheric conditions. Another disadvantage of this algorithm is the increased complexity when compared to P&O method.

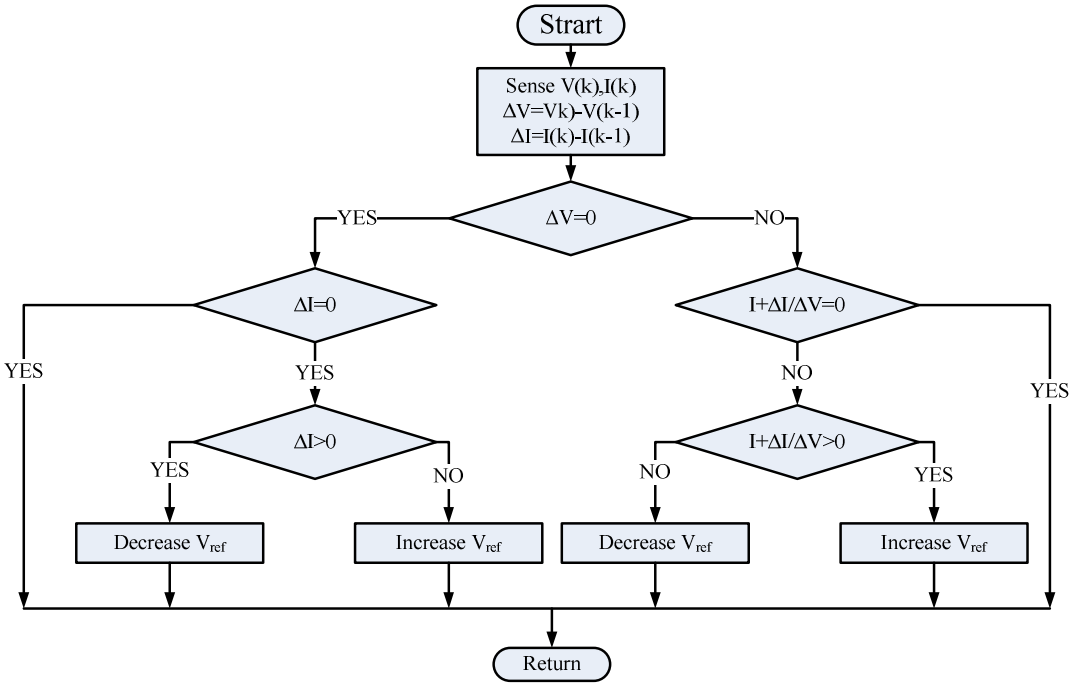


Fig. 43 Flow chart of InC MPPT algorithm.

The CV method algorithm is based on the fact that MPP voltage slightly varies with solar irradiance and the ratio of VMPP/VOC depends only on the solar cell parameters. In many implementations, a commonly used value for the VMPP/VOC ratio is 76%. Periodically, the CV algorithm sets the PV array current to zero to measure the array's open circuit voltage, then, the system operating point is set in correspondence of 76% of the VOC measured value. After a fixed period, the cycle is repeated. The main problem related with such an algorithm is that some energy is wasted when the PV array is disconnected. Moreover, the MPP is not always located at 76% of the array's open circuit voltage.

5.3 Grid Synchronization Control

Phase angle, frequency and amplitude of the utility voltage vector are the main/most important parameters of such system. This algorithm is responsible for the initialization of the system. In this section, a DC/AC control system based on “dq” axes theory is presented.

Phase angle detection method in three-phase system can be easily obtained by synchronous reference frame PLL. However, in case of Single-Phase system, the phase angle is detected by synchronous reference frame using a virtual phase V_β.

Usually the initialization of a standard grid-connected converter consists of a start-up procedure that monitors the input DC voltage value and, if this is inside the correct range. Once the DC bus voltage has reached the reference value, the inverter PWM modulation is enabled by the microcontroller unit to generate a sinusoidal output voltage in phase with the grid voltage. During the start-up phase, a fixed reference value for I_q is used to force the output voltage to increase. When the waveform produced by the inverter is with the same amplitude and in phase with the grid, the algorithm will connect the inverter to the grid and the closed loop power management starts.

5.3.1 Grid angle estimation

In the following paragraph is given a brief overview of some techniques that can be exploited to perform synchronization of the PV converter output voltage with the grid voltage source. This process requires calculation of the grid angle θ_e which defines the position of the phasor representing the grid voltage in the stationary reference frame and is used for reference frame transformations.

5.3.1.1 Zero Crossing Based Techniques

Fig. 44 and Fig. 45 show the zero crossing detection method and its flow chart. Usually the estimated angle θ^* is obtained by integrating the estimated frequency ω^*, which is estimated by controlling the angle difference to zero in the PI controller. In Fig. 44 ω_{set} is the initial frequency. Usually, this method requires minimum resources in terms of computational efforts and hardware, since it needs only the detection of the zero crossing point of the voltage grid source. The main disadvantage of this implementation is the low dynamic response, as the voltage grid phase is updated every half cycle.

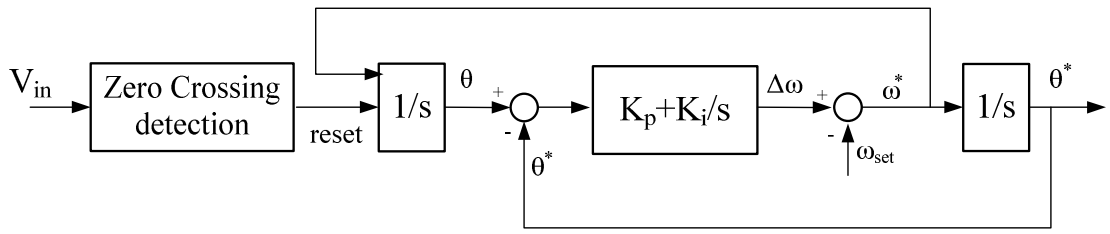


Fig. 44: Zero-Cross-Detection Method

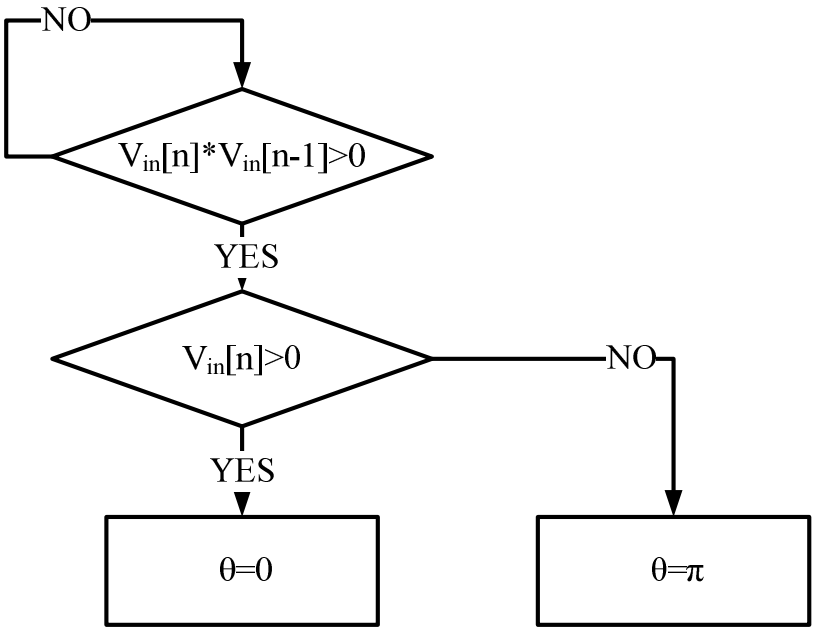


Fig. 45: Flowchart of zero-cross-detection method

5.3.1.2 Techniques Based on Stationary Reference Frame Transformation

Exploiting the projections of the single phase grid voltage signal in a suitable orthogonal stationary reference frame, a considerable improvement of the dynamic performances can be obtained. In particular, the grid voltage V_{Grid} is delayed of 90° degrees in order to obtain the two projections of V_{Grid} in an orthogonal stationary reference frame indicated with α-β, as it is shown in Fig. 46. After filtering the two signals, calculation of the amplitude $|V_{Grid}|$ and phase θ_e of V_{Grid} is performed through equations 12 and 13.

$$\left|V_{Grid}\right| = \left|V_{\alpha,\beta}\right| = \sqrt{v_{\alpha filt.}^2 + v_{\beta filt.}^2} \qquad \text{Eq. 12}$$

$$\theta_e = \text{Atan}\left(\frac{v_{\alpha filt.}}{\left|V_{\alpha,\beta}\right|}, \frac{v_{\beta filt.}}{\left|V_{\alpha,\beta}\right|}\right) \qquad \text{Eq. 13}$$

The filtering process plays an important role in the computation of equations 12 and 13; in fact, the delay introduced by the filters must be compensated in order to reach satisfactory results. Different methods have been proposed in the past in order to minimize such a delay among V_α and V_β. A valid solution is constituted by the use of resonant filters.

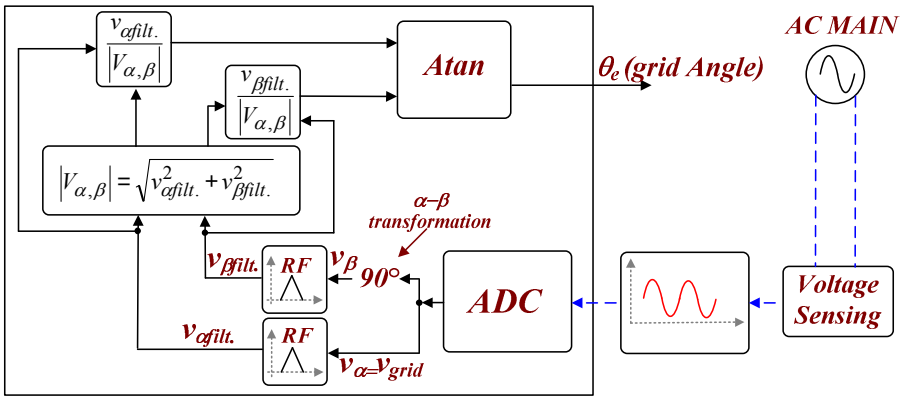


Fig. 46: PLL Block diagram of technique based on Stationary Reference Frame Transformation

5.3.1.3 Techniques Based on Synchronous Reference Frame Transformation

In this approach the two components of V_{Grid} are transformed in a reference frame synchronous with the grid voltage as displayed in Fig. 47. The main advantage of this operation is related to the filtering process, which requires less computational efforts in order to obtain clear signals, since the two transformed quantities V_q and V_d should be constants. Among the several filtering techniques proposed in literature, the Delay Signal Cancellation (DSC) method can be adopted.

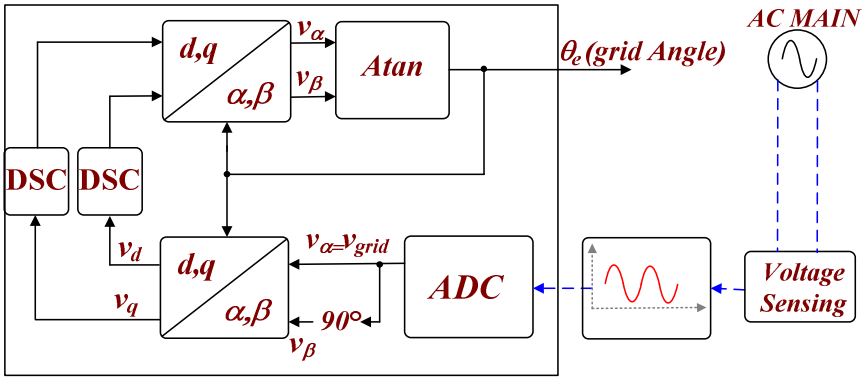


Fig. 47: Block diagram of technique based on Synchronous Reference Frame Transformation.

5.3.1.4 Techniques Based on dq-PLL

The main features of this technique are the decoupled control of active and reactive power and the possibility of using standard PI controllers in the control loop with further advantages in terms of easy implementation and zero error at steady state.

According to Fig. 48, the dq-PLL requires the transformation of the controlled variables, i.e. inverter output current and voltage, from a stationary reference frame (αβ) into a rotating reference frame "dq". If the rotating frequency of the "dq" reference frame is equal to the

frequency of the grid voltage, the transformed quantities are constants and can be controlled with standard PI regulators. It is then clear that correct estimation of the grid frequency is a basic requirement for this type of control. By integrating the grid frequency, the information about the grid angle can be extracted and then used in the equations performing the reference frame change.

While for three-phase inverters phase angle and voltage detection methods can be easily obtained by synchronous reference frame PLLs, for single phase inverters this technique is not so obvious. In fact, to perform the reference frame transformation at least two voltage phases are needed. For this reason a virtual voltage phase, generally called V_β, is generated starting from the available information about the grid voltage. More specifically, the virtual voltage, which is 90 degrees phase shifted with respect to the real one, is generated by sampling the grid voltage and by delaying the acquired samples of a quarter of a period via firmware.

Besides the grid voltage frequency, in current controlled grid-connected inverters, the grid voltage rms value must be constantly monitored in order to ensure the correct operation of the system and avoid hazardous events.

With this control scheme, the voltage component of the d axis is controlled to zero which means that the active power can be adjusted by acting on the q component of the current.

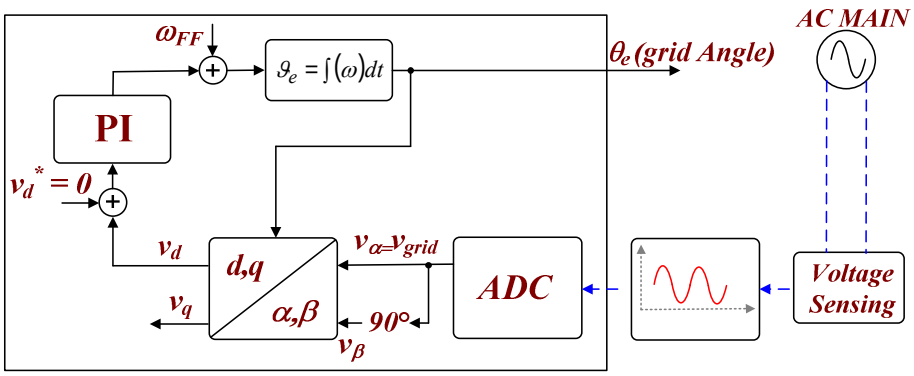


Fig. 48: dq-PLL structure

5.4 Anti Islanding monitoring

Islanding operation could be a interesting solution, for the near future, but at the moment, there are some drawbacks working in islanding. Some of them are as follows:

- Line worker safety can be threatened by DG sources feeding a system after primary sources have been opened and tagged out.
- The voltage and frequency may not be maintained within a standard permissible level.
- The islanded system may be inadequately grounded by the DG interconnection.
- Instantaneous re-closing could result in out of phase re-closing of DG. As a result of which large mechanical torques and currents are created that can damage the generators or prime movers. Also, transients are created, which are potentially damaging to utility and other customer equipment. Out of phase reclosing, if occurs at a voltage peak, will generate a very severe capacitive switching transient and in a lightly damped system, the crest over-voltage can approach three times rated voltage .

Due to these reasons, it is very important to detect the islanding quickly and accurately. Another big issue concerning islanding are the standard compliance. Among the technical requirements for grid connection, such as harmonics and DC current injection limits, the anti-islanding protection is also a big remark in it. Islanding can happen as a result of one or more of the following conditions:

- A fault that is detected by the utility, and which results in opening a disconnecting device, but which is not detected by the PV inverter or protection devices;
- Accidental opening of the normal utility supply by equipment failure;
- Utility switching of the distribution system and loads;
- Intentional disconnect for servicing either at a point on the utility or at the service entrance;
- Human error or malicious mischief; or,
- An act of nature

The main philosophy of detecting an islanding situation is to monitor the DG output parameters and/or system parameters and decide whether or not an islanding situation has occurred from change in these parameters. Islanding detection techniques can be divided into remote and local techniques and local techniques can further be divided into passive, active and hybrid techniques as shown in Figure 1

5.4.1 Islanding detection methods

Islanding detection methods may be divided into five categories: passive inverter- resident methods, active inverter-resident methods, active methods not resident in the inverter, and the use of communications between the utility and PV inverter.

- Passive inverter-resident methods rely on the detection of abnormal values of the voltage at the point of common coupling (PCC) between the PV inverter and the utility.
- Active inverter-resident methods use a variety of methods to attempt to cause an abnormal condition in the PCC voltage that can be detected to prevent islanding.
- Active methods not resident in the inverter also actively attempt to create an abnormal PCC voltage when the utility is disconnected, but the action is taken on the utility side of the PCC. Communications-based methods involve a transmission of data between the inverter or system and utility systems, and the data is used by the PV system to determine when to cease or continue operation.
- Passive Methods not resident in the inverter, such as utility-grade protection hardware for Over/under Frequency and Over/under Voltage protection relaying, are the utility fall-back normally used to assure that loads are not damaged if voltage or frequency are out of specification. Application of such a method may be required for very large PV installations.
- Hybrid method: Hybrid methods employ both the active and passive detection techniques. The active technique is implemented only when the islanding is suspected by the passive technique.

Passive methods for detecting an islanding condition are based on monitoring selected parameters such as voltage and frequency and/or their characteristics and force the inverter to cease converting power when normal specified conditions are abandoned. On the contrary, active methods for detecting the island contain an active circuit to introduce deliberate changes or disturbances to the connected circuit and then monitor the response to determine if the utility grid with its stable frequency, voltage and impedance is still connected.

Among the active methods such as:

- o Detection of Impedance at a Specific Frequency
- o Slip-mode Frequency Shift
- o Frequency Bias
- o Sandia Frequency Shift

- Sandia Voltage Shift
- Frequency Jump

and the passive islanding detection methods such as:

- Under/over Voltage
- Under/over Frequency
- Voltage Phase Jump
- Detection of Voltage Harmonics
- Detection of Current Harmonics

5.4.1.1 Voltage Phase Jump Detection

Phase Jump Detection (PJD) involves monitoring the phase difference between the inverter terminal voltage and its output current for a sudden "jump". Under normal operation and for current-source inverters, the inverter output current waveform will be synchronized to the utility voltage by detecting the rising (or falling) zero crossings of the voltage at node “PCC” in Fig. 49. This is generally accomplished using an analog or digital PLL.

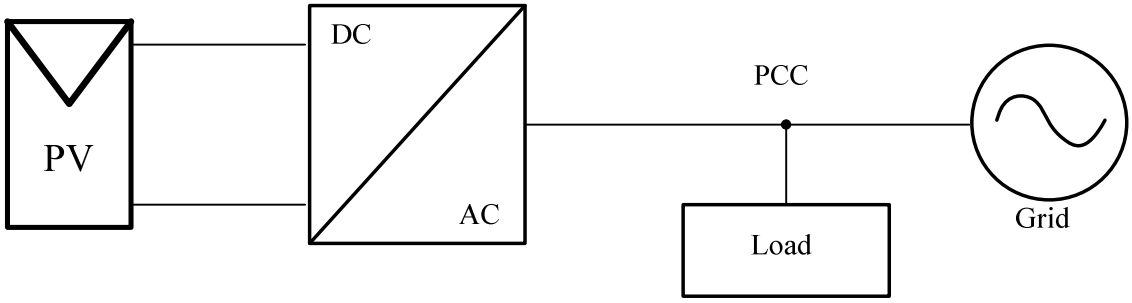


Fig. 49: Block scheme of PV generator connection with the grid

For current-source inverters, when the utility is disconnected, the voltage at the node A is no longer rigidly fixed by the utility voltage source. However, the inverter output current is fixed, since it is still following the waveform template provided by the PLL in the inverter. This happens because the synchronization between voltage and current occurs only at the zero crossings of V_{PCC}. Between zero crossings, the inverter is essentially operating in open-loop mode. Therefore, suddenly it is the PV inverter output current that becomes the fixed phase reference. Since the frequency has not changed yet, the phase angle of the load must be the same as before the utility disconnected, and therefore V_{PCC} must "jump" to this new phase. At the next zero crossing of V_{PCC}, the resulting phase error between the "new" voltage and the inverter output current can be used to detect islanding. If this phase error is greater than some threshold value, the controller can de-energize or shut down the inverter (Fig. 50).

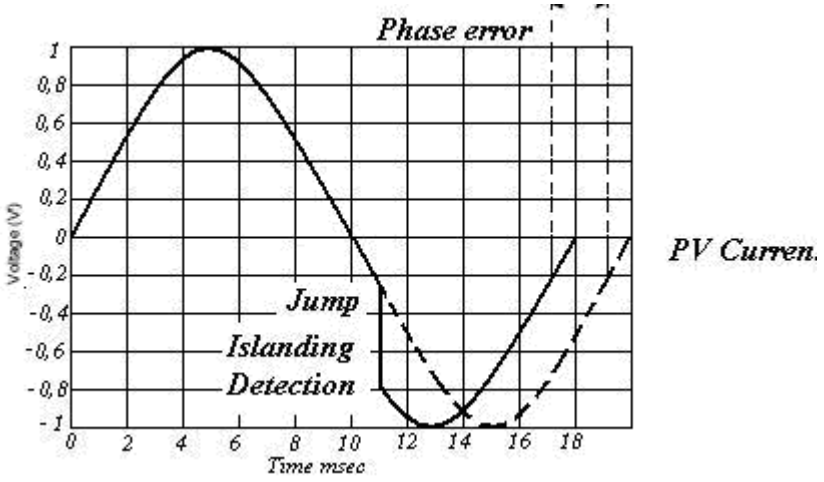


Fig. 50: Waveforms of islanding detection with voltage phase jump detection method

5.4.1.2 Detection of Voltage Harmonics

This method monitors the total harmonic distortion (THD) of the node "PCC" voltage V_{PCC} and shuts down if this THD exceeds some threshold. Under normal operation, the utility, being a "stiff" voltage source, forces a low-distortion sinusoidal voltage (THD ≈ 0) across the load terminals, causing the (linear) load to draw an undistorted sinusoidal current. Summing at node a, when the utility is connected the harmonic currents produced by the inverter will flow out into the low- impedance grid. Because these harmonic currents are kept small and the impedance of the utility is generally low, these harmonic currents interact with the very small utility impedance to produce only a very small amount of distortion in the node "PCC" voltage. Typically, when the inverter is connected to the utility grid, the THD of the voltage V_{PCC} is below the detection point.

When an island occurs, the harmonics of V_{PCC} increase. This happens because the PV inverter will produce some current harmonics in its AC output current, as all switching power converters do. A typical requirement for a grid-connected PV inverter is that it produce no more than 5% THD of its full rated current. When the utility disconnects, the harmonic currents produced by the inverter will flow into the load, which in general has much higher impedance than the utility. The harmonic currents interacting with the larger load impedance will produce larger harmonics in V_{PCC}. These voltage harmonics, or the change in the level of voltage harmonics, can be detected by the inverter, which can then assume that the PV inverter is islanding and discontinue operation.

5.4.1.3 Detection of Impedance at Specific Frequency

This method is a special case of the Harmonic Detection method. The difference, and the reason that this method is considered active rather than passive, is that this method injects a current harmonic of a specific frequency intentionally into node “PCC” via the PV inverter. One variant of the Harmonic Detection method relies on those current harmonics that are unintentionally injected into node “PCC”. When the utility is connected, if the utility impedance is much lower than the load impedance at the harmonic frequency, then the harmonic current flows into the grid, and no abnormal voltage is seen.

Upon disconnection from the utility, the harmonic current flows into the load. If it is assumed that the local load is linear, then it is possible to inject a harmonic current into node “PCC”. The load produces a harmonic voltage, which can then be detected. The name of this method derives from the fact that the amplitude of the harmonic voltage produced will be proportional to the impedance of the load at the frequency of the harmonic current.

5.4.1.4 Slip Mode Frequency Shift

Slip-Mode Frequency Shift (SMFS) uses positive feedback to destabilize the PV inverter when the utility is not present, thereby preventing the reaching of a steady state that would allow a long run-on. The frequency of the grid will not be impacted by this feedback.

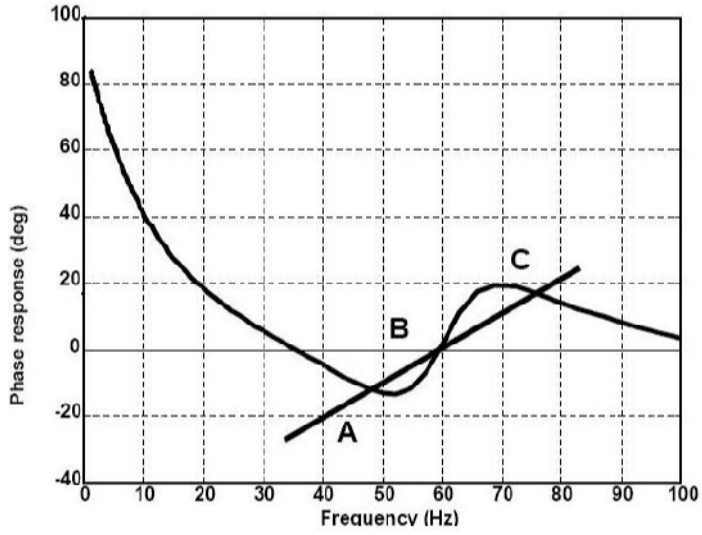


Fig. 51: Waveforms of islanding detection with slip mode frequency shift method-

Normally, PV inverters operate at unity power factor, so the phase angle between the inverter output current and the V_{PCC} voltage is controlled to be zero (or as close to it as possible). In the SMS method, the current-voltage phase angle of the inverter, instead of always being controlled to be zero, is made to be a function of the frequency of the V_{PCC} as

shown in Fig. 51. The phase response curve of the inverter is designed such that the phase of the inverter increases faster than the phase of the (RLC) load with a unity-power factor in the region near the utility frequency ω_0. This makes the line frequency an unstable operating point for the inverter. While the utility is connected, it stabilizes the operating point at the line frequency by providing a solid phase and frequency reference. However, after the island is formed, the phase-frequency operating point of the load and PV inverter must be at an intersection of the load line and inverter phase response curve. Consider the load line of the unity power factor load shown in Fig. 51.The load line and inverter curve intersect at the point labeled "B", at a frequency of 60 Hz and a phase of zero, and operate there as long as the utility is connected. Now assume the utility is disconnected. If there is any small perturbation of the frequency of the node "PCC" voltage away from 60 Hz, the S- shaped phase response curve of the inverter causes the phase error to increase, not decrease. This is the positive feedback mechanism, and it causes a classical instability. This instability of the inverter at ω_0 causes it to reinforce the perturbation and drive the system to a new operating point, either at point A or C depending on the direction of the perturbation. If the inverter phase curve has been properly designed for this RLC load, points A and C will be at frequencies lying outside the OFP/UFP trip window, and the inverter will shut down on a frequency error. SMS is implemented through the design of the input filter to the PLL.

5.4.1.5 Frequency Bias

The frequency bias or Active Frequency Drift (AFD) method is easily implemented in a PV inverter with a microprocessor-based controller. In this method, the waveform of the current injected into node "PCC" by the PV inverter is slightly distorted such that there is a continuous trend to change the frequency. When connected to the utility it is impossible to change the frequency.

When disconnected from the utility, the frequency of V_{PCC} is forced to drift up or down, increasing the "natural" frequency drift caused by the system seeking the load's resonant frequency. An example of a PV inverter output current IPV-inv waveform that implements upward AFD is shown in Fig. 52, along with an undistorted sine wave for comparison. This can also be accomplished smoothly with little or no radio- frequency interference using smooth waveforms such as a second harmonic sine wave. T_{Vutil} is the period of the utility voltage, T_{Ipv} is the period of the sinusoidal portion of the current output of the PV inverter, and T_z is a dead or zero time. The ratio of the zero time T_z to half of the period of the voltage waveform, $T_{Vutil}/2$, is referred to as the chopping fraction cf:

$$c_f = \frac{2 \cdot T_Z}{T_{Vutil}}$$ Eq. 14

During the first portion of the first half-cycle, the PV inverter current output is a sinusoid with a frequency slightly higher than that of the utility voltage. When the PV inverter output current reaches zero, it remains at zero for time T_z before beginning the second half cycle.

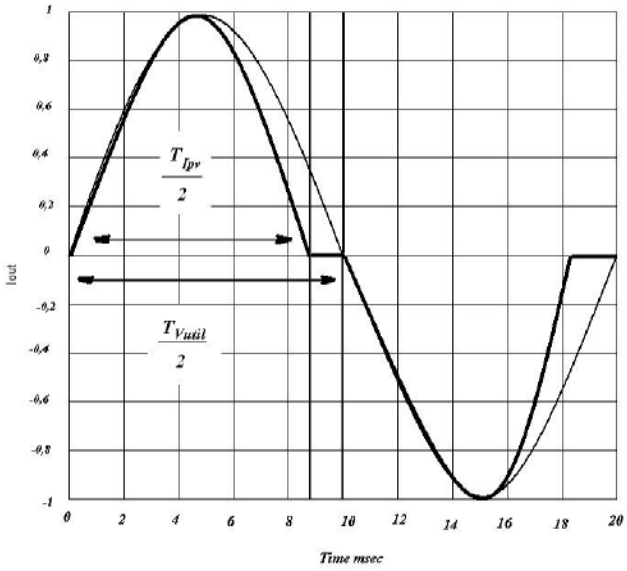


Fig. 52: Waveforms of islanding detection with active frequency drift method

For the first part of the second half-cycle, the PV inverter output current is the negative half of the sine wave from the first half-cycle. When the PV inverter current again reaches zero, it remains at zero until the rising zero crossing of the utility voltage. It is important to note that the zero time in the second half cycle is not fixed and need not equal T_z. When this current waveform is applied to a resistive load in an island situation, its voltage response will follow the distorted current waveform and go to zero in a shorter time (T_{Vutil} - T_z) than it would have under purely sinusoidal excitation. This causes the rising zero crossing of va to occur sooner than expected, giving rise to a phase error between V_{PCC} and $I_{PV\text{-}inv}$. The PV inverter then increases the frequency of $I_{PV\text{-}inv}$ to attempt to eliminate the phase error. The voltage response of the resistive load again has its zero crossing advanced in time with respect to where it was expected to be, and the PV inverter still detects a phase error and increases its frequency again. This process continues until the frequency has drifted far enough from ω0 to be detected by the over/under frequency protection (OFP/UFP).

5.4.1.6 Under/Over Voltage and Frequency

Under/Over Voltage and Frequency method is based on the detection of inverter magnitude and frequency of the output voltage. According to the configuration shown in Fig. 49, in normal condition the active and reactive power supplied by the grid are, respectively, reported in equations 15 and 16, where P_I and Q_I are the output power of the inverter while P_{Load} and Q_{Load} are the load power. Taking into account a load schematization as a parallel between resistance, inductance and capacitance, it is possible to express the load power as in equations 17 and 18. In order to sense the islanding condition, such a method considers the variations of the voltage and frequency in the point PCC, as reported in equation 19 and 20.

$$P_{Grid} = P_I - P_{Load} \quad \text{Eq. 15}$$

$$Q_{Grid} = Q_I - Q_{Load} \quad \text{Eq. 16}$$

$$P_{Load} = \frac{V_I^2}{R} \quad \text{Eq. 17}$$

$$Q_{Load} = V_I^2 \cdot \left(\frac{1}{\omega \cdot L} - \omega \cdot C \right) \quad \text{Eq. 18}$$

$$\Delta P_{PCC} = P_{PCC}(t_1) - P_{PCC}(t_0) \quad \text{Eq- 19}$$

$$\Delta Q_{PCC} = Q_{PCC}(t_1) - Q_{PCC}(t_0) \quad \text{Eq. 20}$$

where PPCC and QPCC are the active and reactive power values in the point PCC. If $\Delta P \neq 0$, the voltage amplitude of the point PCC changes. If ΔP is positive, according to equations 19 and 20, the voltage in the point PCC is bigger than the normal grid voltage. On the contrary if ΔP is negative. If $\Delta Q \neq 0$, the load voltage shows a sudden shift of the phase, then the inverter control will respond changing the frequency of the inverter output current, and thus the frequency of voltage in A is changed. If ΔQ is positive, according to equation 19 and 20, the inverter frequency grows up until the energy in the capacitor is equal of the energy in the inductor. If ΔQ is negative, the frequency decreases. The frequency changes until the load resonant frequency is reached then ΔQ is equal to zero again. The frequency drift is monitored by the block OFP/UFP. When the voltage or frequency values exceed the imposed limits, the islanding condition is recognized.

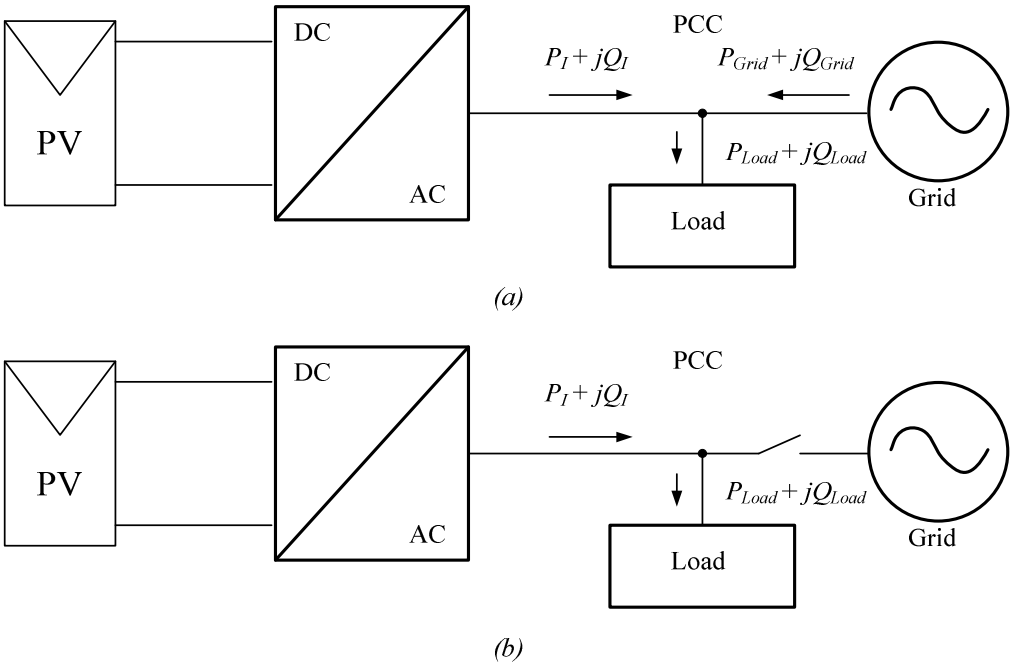


Fig. 53: Power flows in normal (a) and islanding (b) conditions

This is a simple method for detection of islanding that does not cause any distortion but it includes a "No Detection Zone" (NDZ), as it is shown in figure 3.19, related with the standard range of variation of the grid voltage and frequency and to the accuracy of the measurement. Another weakness of the Under/Over Voltage and Frequency islanding detection method is related with the PLL response. As a matter of fact, a fast tracking PLL changes the frequency suddenly but, low dynamic PLL circuits may limit the rate of frequency variation. Therefore, a step phase shift in the inverter voltage equal to the load power factor will take place and the frequency limits are not overtaken.

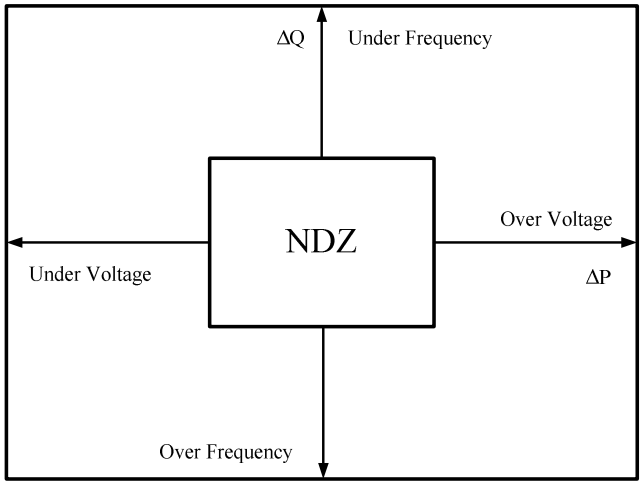


Fig. 54: Islanding not detection zone

5.4.1.7 Sandia Frequency Shift

Sandia Frequency Shift (SFS) is a method that, using a positive feedback on the reference signal of the inverter frequency, allows detecting the islanding condition by monitoring the frequency of the inverter output voltage.

According to such a technique, the frequency of the voltage at node "PCC" of Fig. 53 is forced to change from the inverter output voltage. If the grid is active, the frequency is stable as the grid is prevalent on the inverter. On the contrary, when the grid is off the inverter establishes the frequency of voltage and current of the load. Consequently, because of the positive feedback, the frequency value rapidly increases toward the limit.

The positive feedback of the frequency of the inverter reference is implemented by the following equation:

$$\theta_f = \frac{\pi}{2}\left(c \cdot f_0 + K \cdot \left(f - f_0\right)\right) \qquad \text{Eq. 21}$$

where θ_f is the reference angle, f and f_0 are, respectively, the inverter and grid frequencies, K is the gain of the positive feedback and $c*f_0$ is the chopping fraction corresponding to no frequency error condition.

When connected to the utility grid, no frequency variations in node 'PCC' are detected. On the contrary, if the utility is disconnected, as f_0 is increased the frequency error raises as well as the chopping fraction, then, the inverter frequency is also increased. This process continues until the frequency reaches the upper or lower limit. This method is easy to implement and has one of the smallest NDZ of all the active islanding prevention methods.

The main weakness of the Sandia method is that, because of the positive feedback, the output voltage and current of the inverter are slightly distorted. These effects can be managed by reducing the gain K, which increases the size of the NDZ.

5.4.1.8 Anti-Islanding

In the literature, many islanding detection techniques have been proposed, which can be classified into two big family: remote and local techniques. Local techniques are further divided into passive, active and hybrid techniques. Each technique has its own advantage and limitation, which are summarized into Table 9. Until today there is no single islanding detection technique which works satisfactorily for all systems under all situations. The choice of the islanding detection technique, mainly, depends on the type of the DG and system characteristics. Lastly, hybrid techniques appeared into islanding-detection methods. This kind of

algorithm seems to be a very good alternative,when change in system parameter is large and initiating the active technique when the change in system parameter is not so large for the passive technique to have an absolute discrimination.

Table 9

Islanding Detection Techniques s	Advantage	Disadvantages	Examples
Remote Techniques	Highly reliable	Expensive to implement	Transfer trip scheme . Power line signaling scheme
Local Techniques			
Passive Techniques	Short detection time . Do not perturb the system . Accurate when there is a large mismatch in generation and demand in the islanded system	Difficult to detect islanding when the load and generation in the islanded system closely match . If the setting is too aggressive then it could result in nuisance tripping	Rate of change of output power scheme Rate of change of frequency scheme Rate of change of frequency over power scheme Change of impedance scheme Voltage unbalance scheme Harmonic distortion scheme
Active Techniques	Can detect islanding even in a perfect match between generation and demand in the islanded system (Small NDZ)	Introduce perturbation in the system . Detection time is slow as a result of extra time needed to see the system response for perturbation . Perturbation often degrades the power quantity and if significant enough, it may degrade the system stability even when connected to the grid	Reactive power export error detection scheme Impedance measurement scheme Phase shift schemes
Hybrid Techniques	Have small NDZ. . Perturbation is introduced only when islanding is suspected.	Islanding detection time is prolonged as both passive and active technique is implemented	Technique based on positive feedback and voltage imbalance . Technique based on voltage and reactive power shift

5.5 Power Management

The power management is the core of grid connection. Basically it is composed by the cascade of two control loop: one faster and the other slower. The internal one is a current loop, with a fast response, which regulates the grid current and deal with Power Factor and Harmonic Distortion, while the external voltage loop, which controls the dc-link voltage could deal with other function like MPPT and Power Transfer. The current loop is responsible for power quality issues and current protection; thus, harmonic compensation and dynamics are the important properties of the current controller

Fig. 55 shows the complete control block scheme of a grid-connected, where the two most important blocks, respectively dealing with the grid synchronization and power control, and with MPPT algorithm implementation are clearly shown. Signal sensing is also represented

Both in centralized and distributed approach, inverters and their control algorithms are the core of the conversion system. For these reasons, control of single phase and three phase inverters, for such applications, has been deeply investigated in the past years. Nevertheless, due to utility requirements about power quality and need for high overall efficiency, the controller design is still considerably difficult. The main challenge is due to the fact that the grid is an unknown load and its interaction with the electronic system further complicates the control design process. Moreover, the time-varying nature of both the current and voltage to be controlled makes the design of the controller even more difficult.

International standards on Power Quality, the IEEE Standard 15471 and IEC 61727, require the current injected into the grid by PV converters to have a Total Harmonic Distortion below 5% for an output power above 50% of the rated one. To meet these targets many control architectures can be used. Generally the most common approach consists of two cascaded loops: a fast internal current loop, which regulates the grid current, and an external voltage loop, which controls the dc bus voltage. The dc-link voltage controller is designed for

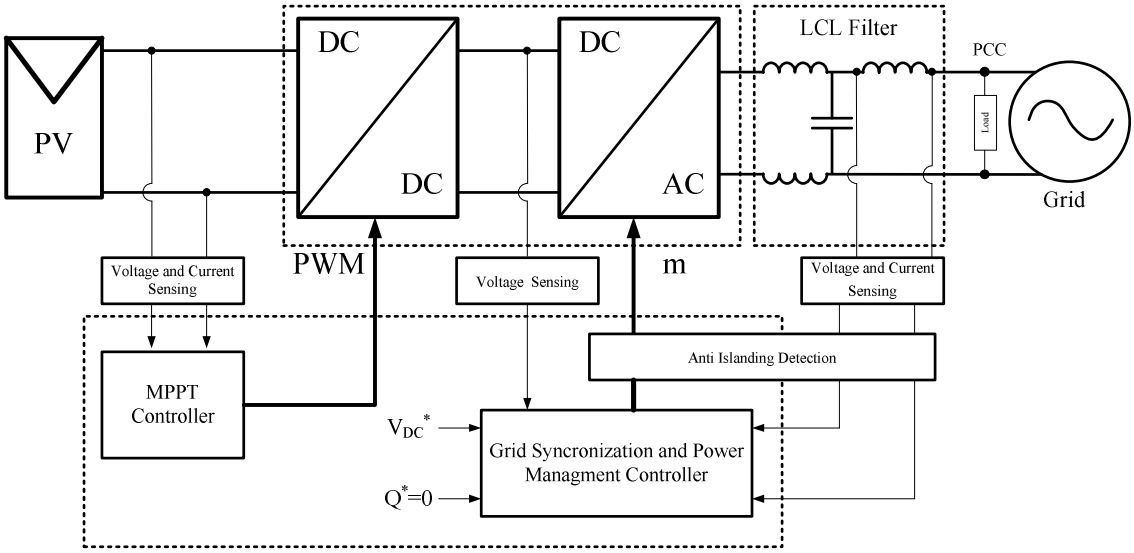


Fig. 55: Control scheme of a grid-connected converter

regulating the power flow from the source to the grid and is generally connected to the MPPT algorithm. This controller has a slower dynamic compared to the inner one.

Other possibilities are the cascade connection of a dc-link voltage loop and an inner power loop or an external power loop and an inner current loop. Another possible classification of

controllers and control algorithms can be based on the reference frame they are implemented in. For example, controllers can be implemented in stationary reference frames, where the control variables are sinusoidal. In this case, non zero steady-state error of PI controller has to be taken into account. Proportional resonant (PR) controllers are the solution to the above mentioned problem, but their implementation is more difficult and requires more computational resources compared to standard PI controllers.

Synchronous reference frame control is another option in which a reference frame transformation allows the use of standard PI controllers since the control variables become dc values.

In Fig. 56, a generic vector $\vec{X}$ is represented together with its components in both the stationary and rotating reference frames.

The control strategy scheme using such an approach is shown in Fig. 57. The DC/AC converter is a current regulated PWM inverter controlled by the modulating reference signal generated by the inverse transformation block. The inputs of this block are the outputs of two PI controllers added to some voltage feed-forward components and the so called cross

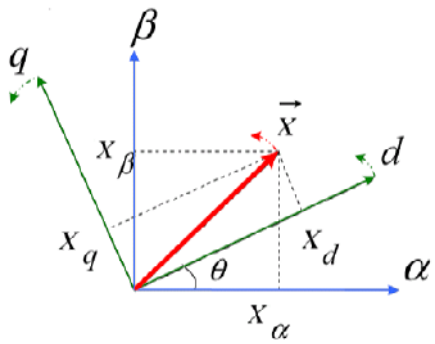


Fig. 56: Vector representation of stationary (αβ) and synchronous (dq) rotating frame

coupling terms, used to take into account the voltage drop on the coupling reactor. The inputs of the two PI controllers are the errors generated by the difference between the current component on the d axis and its reference value and by the current component on the q axis and its reference value. The reference value on the d and q axis are generated by two additional PI controllers designed to regulate the bus voltage V_{BUS} and the reactive power to zero.

The current components on the two axes can be controlled independently and are generated by the direct transformation block whose inputs are the grid current and its 90 degrees phase shift component generated via firmware.

Both the direct and inverse transformation blocks need the information generated by the PLL on the grid voltage angle.

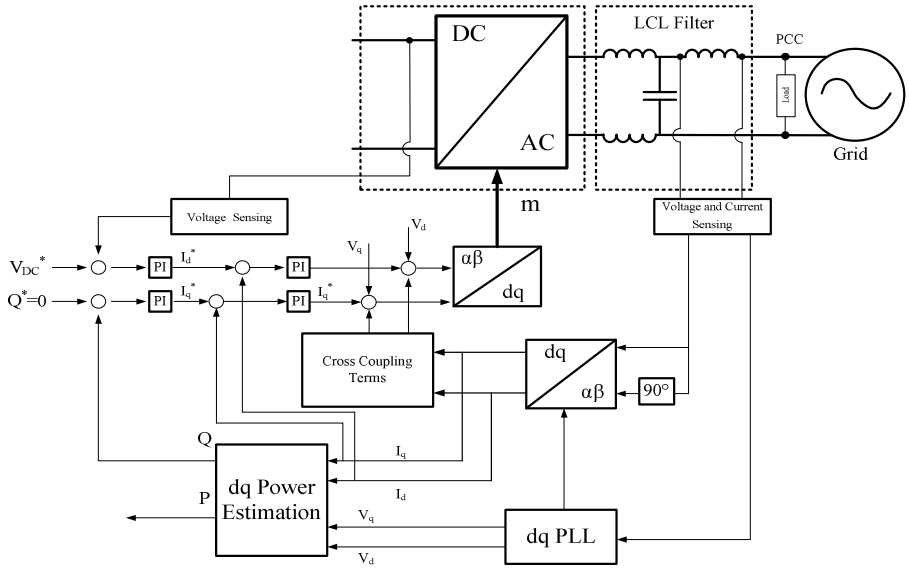


Fig. 57: Scheme of the power management control

- Direct Transformation (αβ/dq)

It implements the α,β stationary to synchronous rotating d,q frame transformation, reported in equations. 22 and 23

$$V_d = V_\alpha \cdot \sin(\theta_e) + V_\beta \cdot \cos(\theta_e) \quad \text{Eq. 22}$$

$$V_q = V_\alpha \cdot \cos(\theta_e) - V_\beta \cdot \sin(\theta_e) \quad \text{Eq. 23}$$

- Inverse Transformation (dq/)

It implements d,q to α,β stationary frame transformation, shown in equations 24 and 25.

$$V_\alpha = V_d \cdot \cos(\theta_e) - V_q \cdot \sin(\theta_e) \quad \text{Eq. 24}$$

$$V_\beta = V_d \cdot \sin(\theta_e) + V_q \cdot \cos(\theta_e) \quad \text{Eq. 25}$$

5.6 Output Filter Design

Another important issue in grid-connection is the design of the output filter. The current generated by the inverter requires adequate filtering to limit the current harmonics injected into the grid and comply with the standards. The output-filter aims to reduce the high order harmonics at the grid side, but a poor design of it can cause a lower attenuation compared to that expected or even an increase of the distortion due to oscillation effects.In practice, a simple first order L filter or a second order LC filter can be used to connect the converter to

the grid and reduce the harmonic content of the current. However, a more effective way to perform this task, compared to L or LC filter, is ensured by LCL filters. Compared to L filters, they provide better attenuation with a smaller inductance value for the same switching frequency and desired harmonic attenuation. Compared to LC filters, their interaction with the grid is considerably reduced due to better decoupling between filter and grid impedance offered by the additional reactor. For these reasons, they have been recently applied in current controlled grid connected converters, especially in the high-power range. Despite the above mentioned advantages, the design of LCL filters is more difficult and can impact on the performance of grid-connected current controllers. The other disadvantage is the increase in cost and component count. Since special care has to be taken in designing LCL filters, this section provides some design hints and guidelines to better understand the filter interaction with the grid and impact on the control algorithm stability. The design procedure starts from the choice of the filter inductance value, Li. Since the function of this inductor is to limit the current ripple on the inverter output, its value can be chosen with the following equation:

$$L_i = \frac{V_{bus} - V_{grid\_pk}}{2\Delta i} \frac{D}{f_{sw}} \qquad \text{Eq. 26}$$

where, V_{bus} is the voltage on the Dc-link, D is the modulating index value and f_{sw} is the inverter switching frequency. Generally, the ripple current value is limited to 10% of the nominal output current. Then, the value of Δi can be calculated as follows:

$$\Delta i = \frac{0.1 * \sqrt{2} P_n}{V_{grid}} \qquad \text{Eq. 27}$$

Where, P_n is the nominal output power of the inverter V_{grid} is the rms value of the grid voltage.

Knowing the value of Δi the filter inductance is:

$$L_i = \frac{V_{bus} - V_{grid\_pk}}{2\Delta i} \frac{\frac{V_{grid\_pk}}{V_{bus}}}{f_{sw}} \qquad \text{Eq.28}$$

The second step of the design procedure is to choose the filter capacitor value. Generally, the size of this capacitor is limited by the reactive power exchanged between the capacitor itself and the inductive components. A practical rule is to limit the reactive power exchange below 5% of the nominal power according to:

$$P_{Xc} = \frac{V_{grid}^{\ 2}}{X_c} = 5\%P_n \qquad \text{Eq. 29}$$

which means:

$$X_c \geq \frac{V_{grid}^{\ 2}}{P_{X\,c}} \rightarrow C \leq \frac{1}{\omega X_c} \qquad \text{Eq. 30}$$

where, X_c is the reactance of the filter capacitor, Pc is the reactive power produced by C. The last step is the design of the coupling reactor. Two basic guidelines have to be taken into account: first, the resonant frequency of the LCL filter should be comprised between ten times the grid frequency and one half the switching frequency; second, the voltage drop on the filter inductor and the grid coupling inductor must be lower than 10% of the nominal grid voltage. Then, the two following equations can be written:

$$10F_{grid} \leq F_R \leq \frac{F_{sw}}{2} \qquad \text{Eq. 31}$$

$$X_L \cdot I_{grid} \leq 0.1 \cdot V_{grid} \qquad \text{Eq. 32}$$

Where $X_L = X_i + X_g$ is the sum of the filter reactance and grid coupling reactance and FR is the resonant frequency of the LCL filter given by:

$$F_R = \frac{1}{2\pi}\sqrt{\frac{Li + Lg}{Li \cdot Lg \cdot C}} \qquad \text{Eq. 33}$$

The limitation on the voltage drop allows finding the maximum value of the grid coupling inductance as it follows:

$$\left(\mathrm{X_i} + \mathrm{X_g}\right) \cdot \mathrm{I_{grid}} \leq 0.1 \cdot \mathrm{V_{grid}} \rightarrow \mathrm{X_g} \leq \frac{0.1 \cdot \mathrm{V_{grid}} - \mathrm{X_i} \cdot \mathrm{I_{grid}}}{\mathrm{I_{grid}}} \qquad \text{Eq. 34}$$

$$L_g \leq \frac{1.14}{\omega_{grid}} \leq 3.6mH \qquad \text{Eq. 35}$$

where, I_{grid} is the nominal output current value.

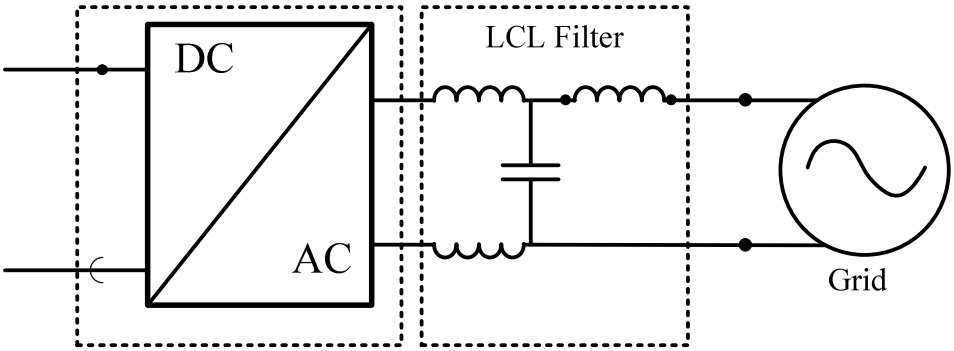


Fig. 58 LCL filter topology

5.7 PWM Techniques

Important issue in grid-connection is the PWM technique, which deal with harmonic distortion, common mode and efficiency of course. In the following paragraphs an investigation about the PWM techniques for grid converter inverter is given, starting with the well know techniques and than shown the mixed frequency technique

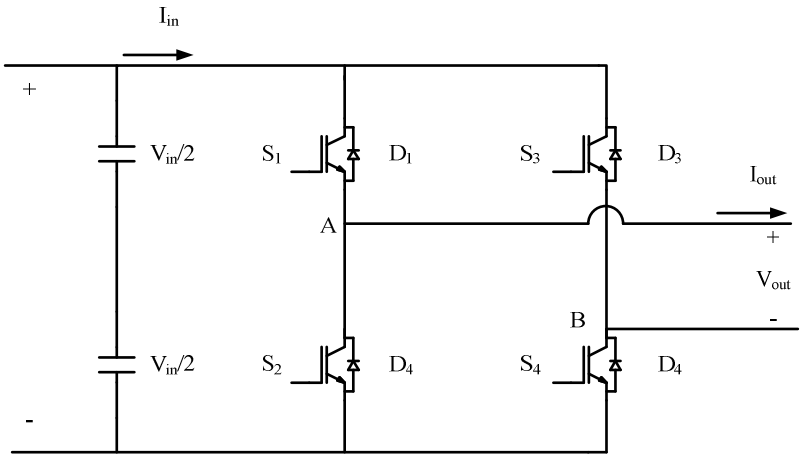


Fig. 59: Full Bridge inverter schematic

5.7.1 Bipolar technique

Basically, in this modulation technique the switches are commutated in couple S1-S4 and S2-S3 (Fig. 59). With this type of PMW switching, the output voltage waveform of the leg A is determinate by comparison of $V_{control}$ and V_{tri}. The output if the inverter leg B is negative of the leg A:

$$V_A(t) = -V_B(t)$$ Eq. 36

$$V_O(t) = V_A(t) - V_B(t) = V_{in}$$ Eq. 37

The maximum value of the output voltage is equal to

$$V_{o_1} = m \cdot V_{in} \qquad 0 \le m \le 1$$ Eq. 38

The Harmonic spectrum of the output voltage for this kind of modulation is shown in . Mixed frequency PWM

A strategy to improve the harmonic contents is the specific PWM technique described in the present paper . Referring to the schematic in Fig. 59, we can identify two legs: the one on the left called the high-frequency leg and the one on the right called the low-frequency leg. In the high-frequency leg, switches S1 and S2 are operated at the frequency chosen by the designer according to his main requirements and targets (typically in the range between 10 and 60 kHz), while the devices S3 and S4 are switched at the mains frequency (50 or 60 Hz) according to the sequence shown in Figure 1b. For example, during the positive half wave of the output voltage, S3 stays on and S4 stays off all the time, while S3 and S4 are modulated according to a unipolar PWM mode. So either a positive or a zero voltage is applied to the output of the inverter. Similarly, considering the output negative half wave, S3 is off and S4 stays on, with S1 and S2 modulated [40][41][43][44]**Error! Reference source not found.**.

The spectrum is centered to mf, and its multiples 2 mf, 3 mf. The current spectrum is identical for 0<ma<1 and for mf>9. Basically the frequencies, which are possible to find the harmonic voltage, can be determinate as following:

$$f_h = (j \cdot m_f \pm k) \cdot f_m$$ Eq. 39

The k-order harmonic

$$h = j \cdot m_f \pm k$$ Eq. 40

5.7.2 B. Unipolare

In PWM with unipolar voltage switching, the switches in the two legs of the full bridge are not switched simultaneously, as in the bipolar technique. The leg A and the leg B are controlled separately by comparing Vtri with Vcontrol and –Vcontrol, respectively, as shown in Fig. 62

$$V_{Control} \geq V_{tri} : \; S_1 = ON \quad S_2 = OFF \; V_A = V_{in} \qquad \text{Eq. 41}$$

$$V_{Control} \leq V_{tri} : \; S_1 = OFF \quad S_2 = ON \; V_A = 0 \qquad \text{Eq. 42}$$

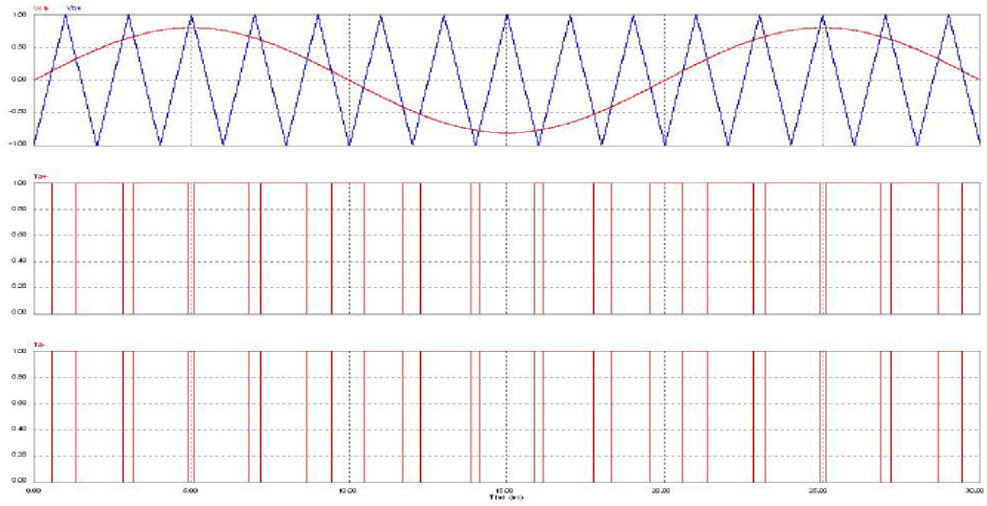


Fig. 60: Bipolar PWM modulation

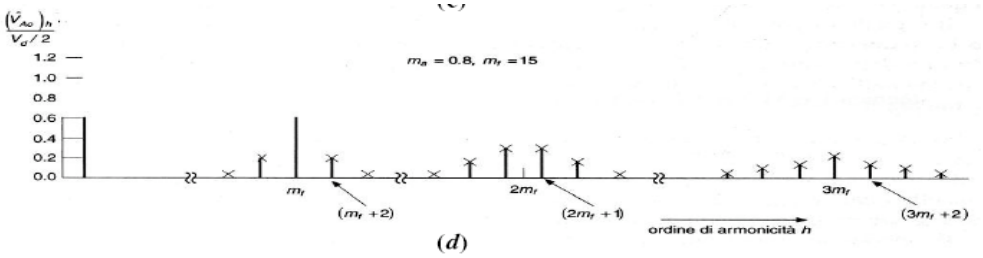


Fig. 61: Bipolar PWM modulation mf=15 e ma=0.8.

$$\left(-V_{Control}\right) \leq V_{tri} : \; S_3 = OFF \quad S_4 = ON \; V_B = 0 \qquad \text{Eq. 43}$$

$$\left(-V_{Control}\right) \geq V_{tri} : \; S_3 = ON \quad S_4 = OFF \; V_B = V_{in} \qquad \text{Eq. 44}$$

Compare to the bipolar PWM the switching frequency in the load is the double compare to the real switching frequency. This is an advantage concern to the output filter design. This is also evident into the frequency spectrum, as shown in Fig. 63.

5.7.3 . Mixed frequency PWM

A strategy to improve the harmonic contents is the specific PWM technique described in the present paper . Referring to the schematic in Fig. 59, we can identify two legs: the one on the left called the high-frequency leg and the one on the right called the low-frequency leg. In

the high-frequency leg, switches S1 and S2 are operated at the frequency chosen by the designer according to his main requirements and targets (typically in the range between 10 and 60 kHz), while the devices S3 and S4 are switched at the mains frequency (50 or 60 Hz) according to the sequence shown in Figure 1b. For example, during the positive half wave of the output voltage, S3 stays on and S4 stays off all the time, while S3 and S4 are modulated according to a unipolar PWM mode. So either a positive or a zero voltage is applied to the output of the inverter. Similarly, considering the output negative half wave, S3 is off and S4 stays on, with S1 and S2 modulated [40][41][43][44]**Error! Reference source not found.**.

$$V_{Control} \geq 0: \; S_3 = \text{OFF} \quad S_4 = \text{ON} \qquad \text{Eq. 45}$$

$$V_{Control} \leq 0: \; S_3 = \text{ON} \quad S_4 = \text{OFF} \qquad \text{Eq. 46}$$

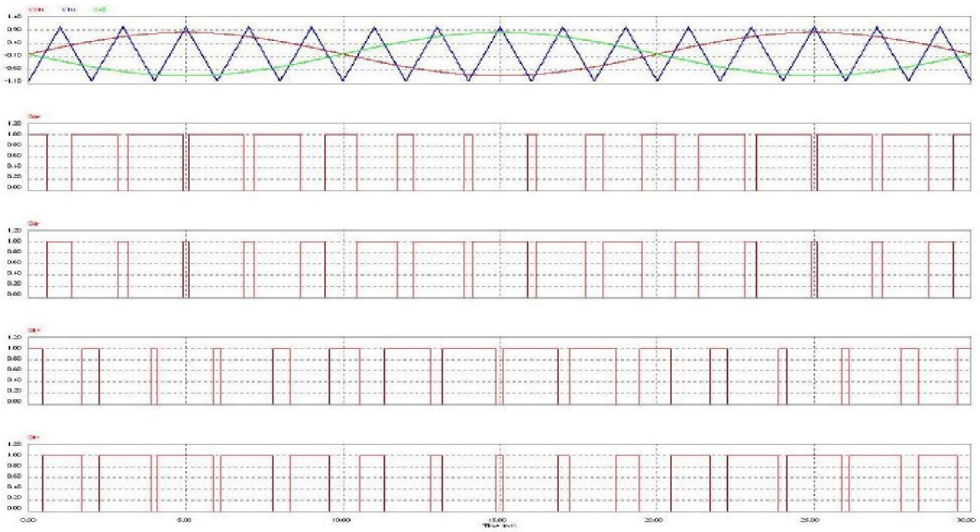


Fig. 62: Unipolar PWM modulation

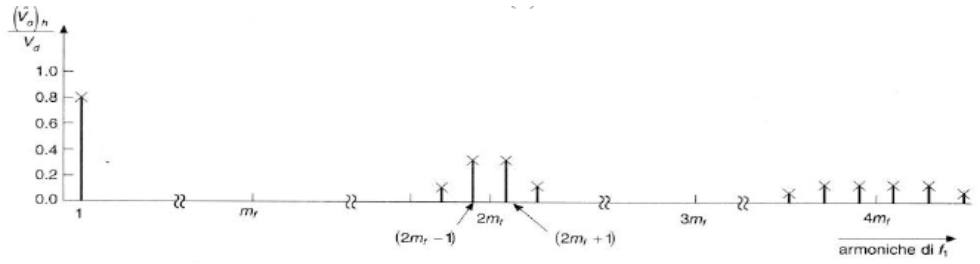


Fig. 63: Unipolar PWM modulation mf=15 e ma=0.8.

$$V_{Control} \geq 0$$
$$V_{Control} \geq V_{tri} \quad S_1 = ON \quad S_2 = OFF \quad V_{AB} = V_{in} \qquad \text{Eq. 47}$$
$$V_{Control} \leq V_{tri} \quad S_1 = OFF \quad S_2 = ON \quad V_{AB} = 0$$

$$\left(-V_{Control}\right) \leq 0$$
$$\left(-V_{Control}\right) \leq V_{tri} \quad S_{21} = OFF \quad S_1 = ON \quad V_{AB} = 0 \qquad \text{Eq. 48}$$
$$\left(-V_{Control}\right) \geq V_{tri} \quad S_2 = ON \quad S_1 = OFF \quad V_{AB} = V_{in}$$

The low switching frequency allows the converter to get high performance in term of efficiency. A further advantage is due to the fact that the low switching frequency allows the use of suitable transistor designed for low frequency commutation with a very low voltage during the on state. This allows a further reduction of the power losses concerning the on state.

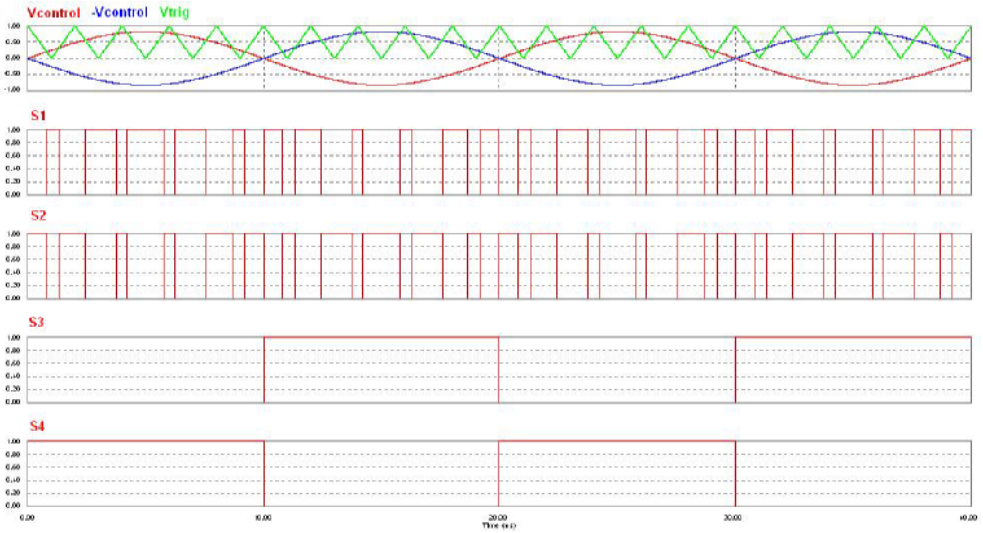


Fig.64: Hybrid PWM modulation

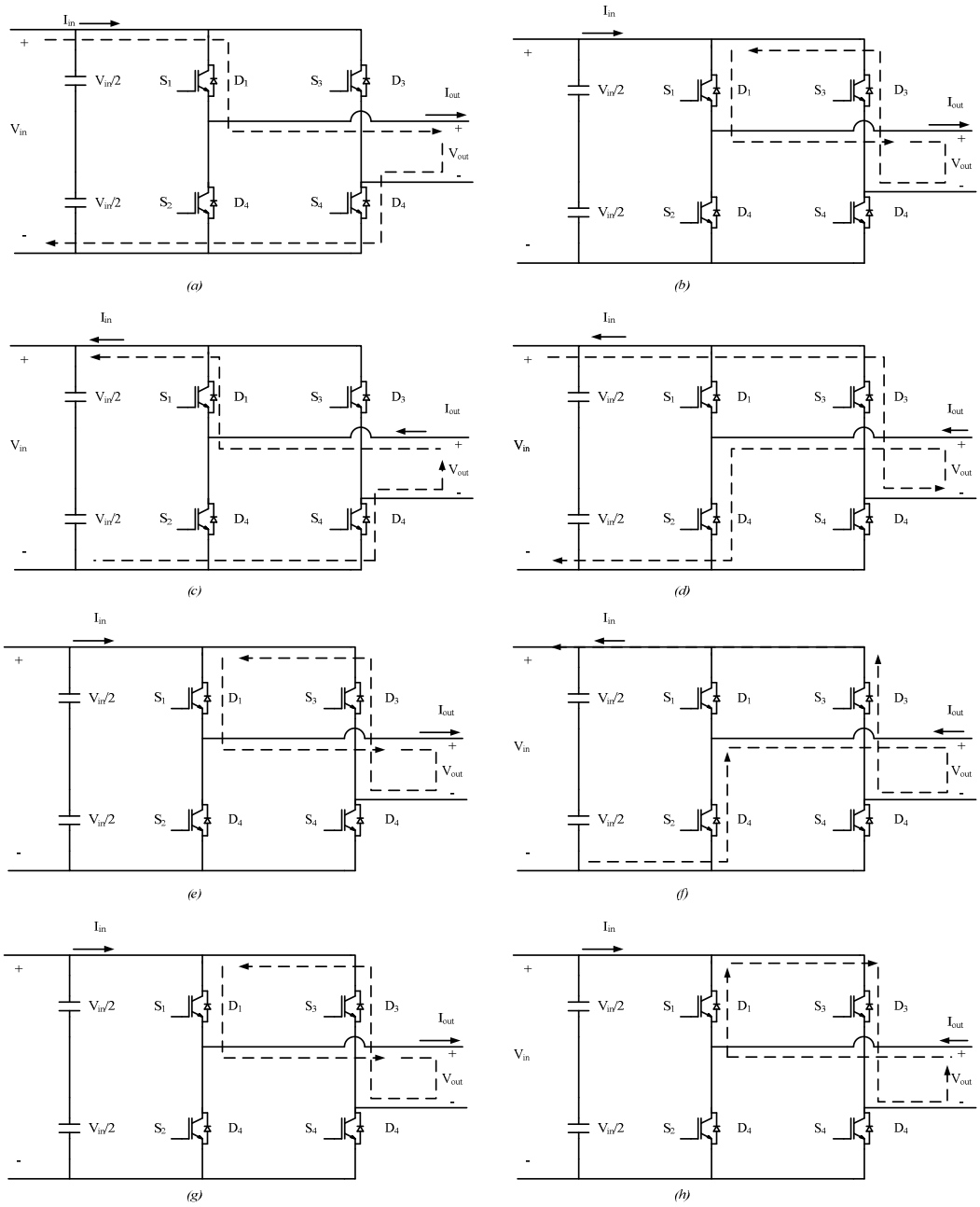


Fig. 65: State of commutation for Hybrid PWM modulation

5.7.4 . Comparison of the PWM techniques and experimental result

A Mixed Frequency technique has been implemented in order to get a low THD and a better efficiency. At the first a carefully analysis has been done by common simulation tools such as PSIM in order to understand the real advantages versus the well known techniques. The simulations has been performed using the following transistors: fast-IGBT (STGW35HF60WD), for the standard techniques and for the high frequency device S1 S3 in the hybrid technique, while for the hybrid S2 S4 low-droop IGBT(HGTG30N60B3) with ultra-fast diode in parallel D2 D4 (STTH30R06).

The simulation results have highlighted the possibility to increase the efficiency using the mixed PWM. In fact, the Hybrid technique shows a higher efficiency compare to the unipolar and the bipolar. The Hybrid technique has shown a efficiency of 98,4 % while the unipolar of 98,3 % and the bipolar .

The Mixed Frequency modulation technique has been implemented on a prototype from 3kW. The “dq” control axes has been implemented through the use of Dspace/Simulink platform. Just two types of modulation have been compared: the Unipolar and the new one. The prototype has confirmed the results of simulations.

The PWM technique has been tested in a 3 kW Full-Bridge Inverter with a 20 kHz switching frequency. Figure 8 shows the comparison between the Mixed frequency PWM technique and the Unipolar in term of Harmonic. As you can see, the Magnitude of the 3th harmonic, detected with the Mixed technique is half of the one detected with the Unipolar Technique. The current THD of the Unipolar was 5, 6%, instead for the inverter driven by the Mixed Frequency was 3.5%. For both modulation techniques, the effect of dead time was not compensated. The peak efficiency determined with the modulation technique with low losses was 98,5% and 97,3% for the tests with the modulation technique Unipolar.

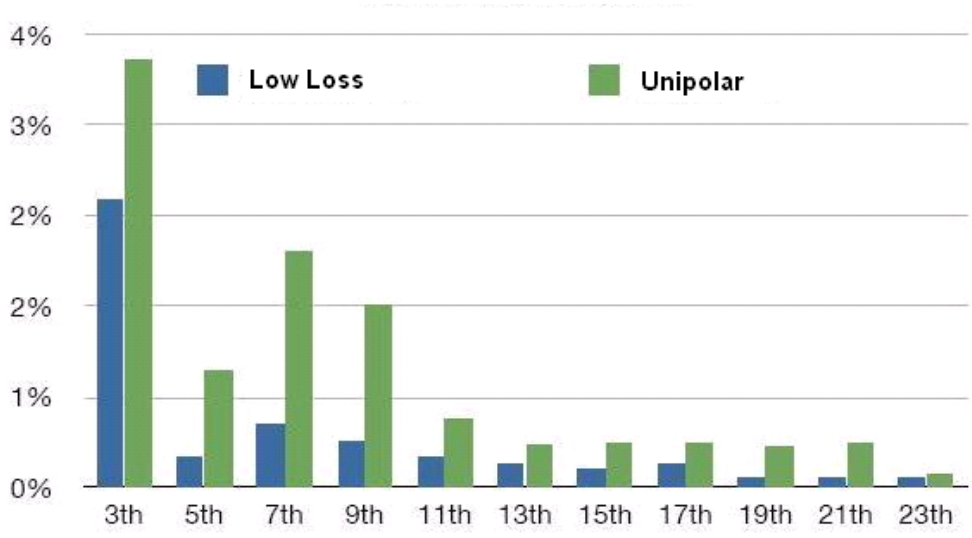


Fig. 66: Harmonic distortion comparison between mixed frequency PWM technic and Unipolar technic

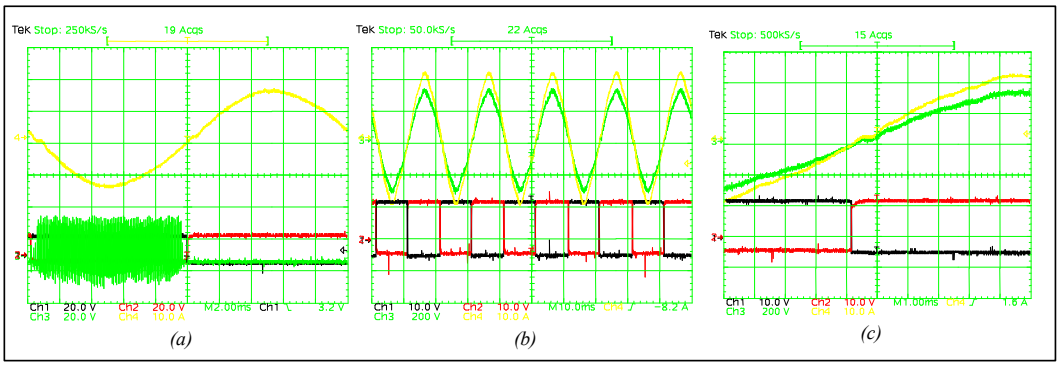


Fig. 67: Waveforme of the hybrid technique (a)Yellow output current (10A/div) ; Red Gate signal S_4 (20V/div); Black Red Gate signal S_2 (20V/div); Green(20V/div Gate signal S3; (b) Yellow output current (10A/div) ; Red Gate signal S_4 (20V/div); Black Red Gate signal S_2 (20V/div); Green output voltage(20V); (c) Yellow output current (10A/div) ; Red Gate signal S_4 (20V/div); Black Red Gate signal S_2 (20V/div); Green output voltage(20V);

In Fig. 68 is shown the measured efficiency of the inverter in case the proposed Low Loss and standard Unipolar PWM techniques are applied. The comparison clearly demonstrates the better performance of the proposed approach. In Fig. 66 are shown the current harmonics amplitude measured using a standard Unipolar or the proposed Low Loss PWM without dead-time compensation. The chart shows that, using the proposed approach, a harmonics reduction is also obtained, performing a current THDi less than 3,5 % for output power higher than 40% of the rated one.

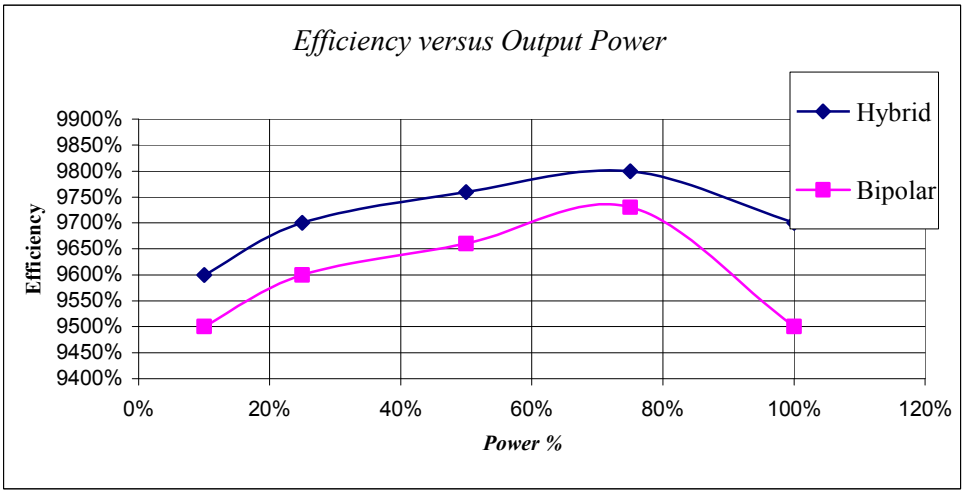


Fig. 68:: Inverter efficiency of the PV converter

5.8 Summary

After an accurate evaluation of some of the most popular single-phase PV converter control strategy, the research has been focused on the study, design of the filter, comparison of PWM modulation and PLL analysis.

Chapter 6
Control of Single Phase Inverter for grid connection

In this chapter the focus is addressed to accuracy on estimation of the phase of the grid voltage. Many algorithms have been proposed for estimation of the phase of the voltage grid based on Phased-Locked Loop (PLL) techniques. In order to evaluate the performance in terms of noise rejection and dynamic response of most used PLL algorithms, a comparison accomplished through simulations and experimental results is presented in different operating conditions and voltage disturbance.

6.1 PLL Algorithms

The increasing demand of electric energy and environmental concerns are the driving force for adopting emerging technology of grid-connected Distributed Generation (DG) systems based on alternative resources such as photovoltaic, wind and hydrogen. A difficult task that must be satisfied by such DGs consists in fulfilling the Power Quality standards. As a matter of fact, international institutes as IEEE and IEC impose some limits on the minimum power factor of the inverter output current, on current harmonics, and maximum voltage at the connection point.

In a DG system, the performance regarding power quality issues depends on the control algorithm and/or passive filters. Consequently, a suitable control strategy should be adopted, also able to reduce the number and size of passive components. A critical task for a grid synchronization and active and reactive power control, especially in single-phase systems, consists in a correct detection of the phase angle of the grid voltage. Concerning such an issue, the most used procedures are based on Phase Locked Loop (PLL) algorithms. Depending on the grid conditions, the connections of the distributed generators can occur in

such a points where the voltage grid waveform is distorted by the presence of voltage harmonics.

Moreover, to avoid unwanted disconnections of DGs, the PLL algorithms should be robust to voltage disturbances, such as sags, dips and swells, and to unwanted conditions, such as frequency variation, phase jumps normally caused by large load disconnections or faults. Finally, a relevant issue related to digital implementation of the control algorithm is the presence of an offset in the measured grid voltage. Such an offset is typically introduced by the measurement and data conversion processes.

In this chapter, exploiting simulations and experimental results, a comparison of largely adopted PLL algorithms is presented, regarding the performance accomplished for the estimation of the phase of the grid voltage under abnormal conditions. Comments on various PLL behaviors are included and a schematic classification of the response of PLL algorithms to the considered disturbance is presented.

6.2 PLL Algorithms

To estimate the phase of the grid voltage in DG, the most suitable PLL algorithms presented in literature have been employed. PLL structure basically consists of a Phase Detector (PD), a Loop Filter (LF) and a Voltage-Controlled Oscillator (VCO). Loop Filter is in general performed through a standard Proportional Integral (PI) regulator. The VCO stage generates a signal in order to minimize the output error of the phase detector.

The PLL algorithms used in the controller for synchronizing DGs with the main grid, are based on transformations of the reference frames of the electrical quantities. In particular, the PLLs can be referred to stationary or synchronously rotating reference frames [30][31][32].

6.2.1 Power based PLL (P_PLL)

One of the basic algorithm is the Power based PLL, shown in Fig. 69. The input signal Vgrid is multiplied to a sinusoidal feedback signal and processed by a low pass filter to eliminate the second order harmonics, normally present in single-phase PLLs.

Finally, the signal is integrated by a VCO in order to obtain the phase angle of the Vgrid. As the cut-off frequency of the low pass filter is low, the P_PLL bandwidth results particularly limited.

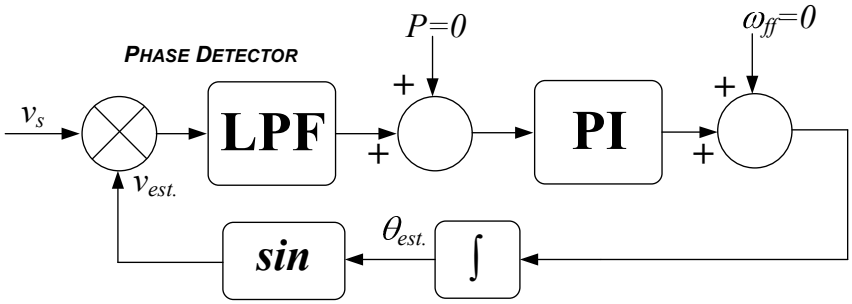


Fig. 69: Power based PLL

$$V_s \cdot \cos(\omega t) \cdot \sin(\omega' t) = \frac{1}{2}\left[\sin(\omega + \omega')t + \sin(\omega - \omega')t\right] \qquad \text{Eq- 49}$$

$$e_{rr\_filt.} = LPF\left(\frac{1}{2}\left[\sin(\omega + \omega')t + \sin(\omega - \omega')t\right]\right) = \frac{1}{2}\sin(\omega - \omega')t \cong (\omega - \omega')t = \vartheta_e - \vartheta_e' \quad \text{Eq. 50}$$

6.2.2 Enhanced PLL (E_PLL)

The block diagram of the E_PLL is shown in Fig. 70. The Phase Detection (PD) structure of the E_PLL is composed of three multiplier blocks, an integration block, a 90° phase shift block (cos(x)) and a comparator.

The main difference with the aforementioned P_PLL, is the PD structure [10]. In fact, such a PD implementation allows more flexibility and provides additional information such as amplitude and phase angle of the input signal. One more feature of this PLL structure is that the output is locked both in phase and in amplitude. In fact, E_PLL consists of an inner loop which tracks the error phase between the grid voltage signal and the estimated voltage, and an additional external loop performing a tracking on the entire input signal.

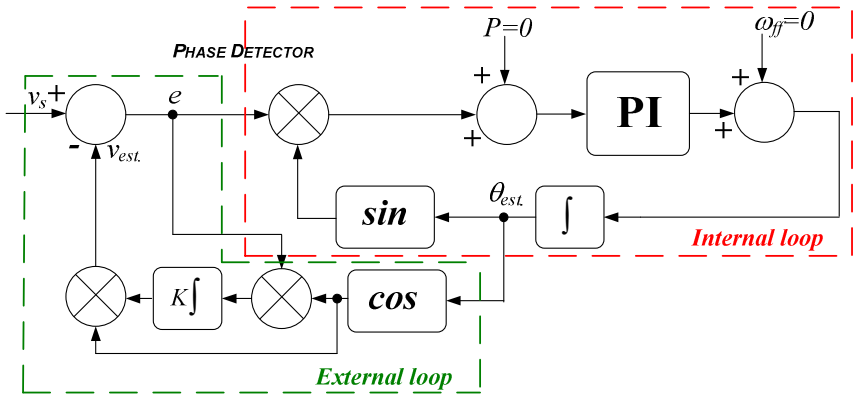


Fig. 70: Enhanced PLL

6.2.3 *XOR gate based PLL (X_PLL)*

The block diagram of X_PLL is shown in Fig. 72. The key-feature of X_PLL is the PD block, which uses two Flip-Flop logical ports. Two trigger Schmitt circuits square the input and feedback signals, and then two flip-flops generate the square-wave outputs at twice the input signal frequency. The difference between the flip-flop outputs is calculated and represents the phase detector output.

The algorithm requires symmetrical reference signals. Moreover, since this PLL is essentially a zero crossing detection based algorithm, it has an intrinsic limited bandwidth. Squaring the input voltage signal assures a quite robust rejection to disturbances [11].

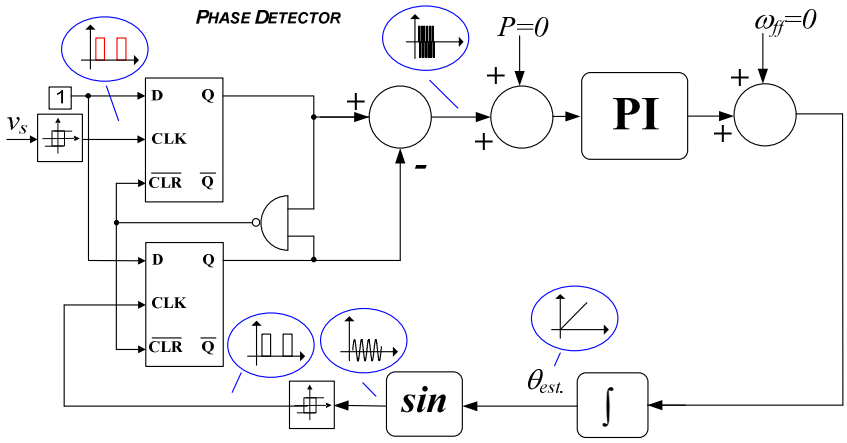


Fig- 71:: XOR gate based PLL schemes (X_PLL).

6.2.4 Orthogonal system generation based PLL (O_PLL)

The main features of the O_PLL are a decoupled control of active and reactive power and the possibility of using standard PI controllers in the control loop with further advantages in terms of easy implementation and zero steady state error.

According to Fig. 72, the control architecture requires a transformation from a stationary (α,β) into a rotating (q,d) reference frame of the controlled variables, the i.e. inverter output current and/or voltage. As the rotating frequency of the q,d reference frame is equal to the frequency of the grid voltage, the transformed quantities are constant (synchronous reference frame) and can be suitably controlled with standard PI regulators. It is clear that a correct estimation of the grid frequency is the basic requirement for this type of control. By integrating the grid frequency, information about the grid angle can be extracted and then used in the equations, performing the reference frame change.

While for three-phase inverters phase angle and voltage detection methods can be easily

obtained by synchronous reference frame PLLs, for single-phase systems this technique is not so obvious. In fact, to perform the reference frame transformation at least two voltage phases are needed. For this reason a virtual voltage phase, generally called Vβ, is generated copying and shifting the available information about the grid voltage .

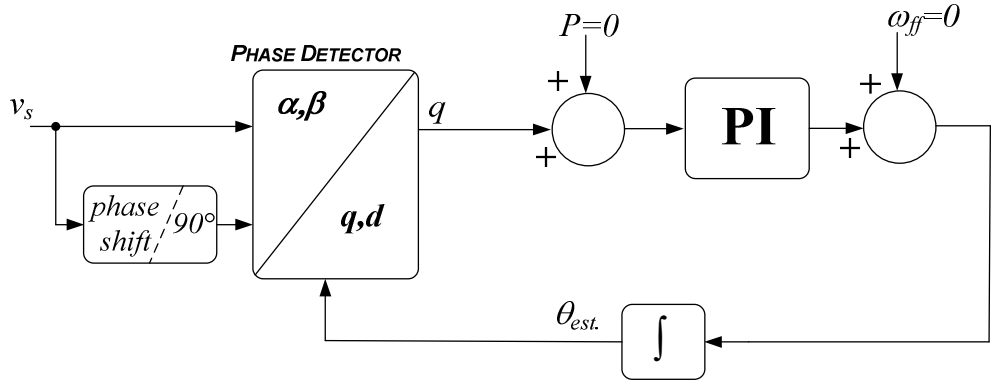


Fig. 72: Orthogonal system generation based PLL scheme (O_PLL).

6.2.5 Inverse Park transformation based PLL (I_PLL)

In I_PLL algorithm, whose scheme is shown in Fig. 73, the signal of the dummy voltage Vβ is generated in an inner feedback loop using the direct and inverse transformations. The obtained Vd signal is compared to a zero reference and processed by the LF and VCO blocks. The main difference among the O_PLL and I_PLL consists in the generation of the dummy V signal-

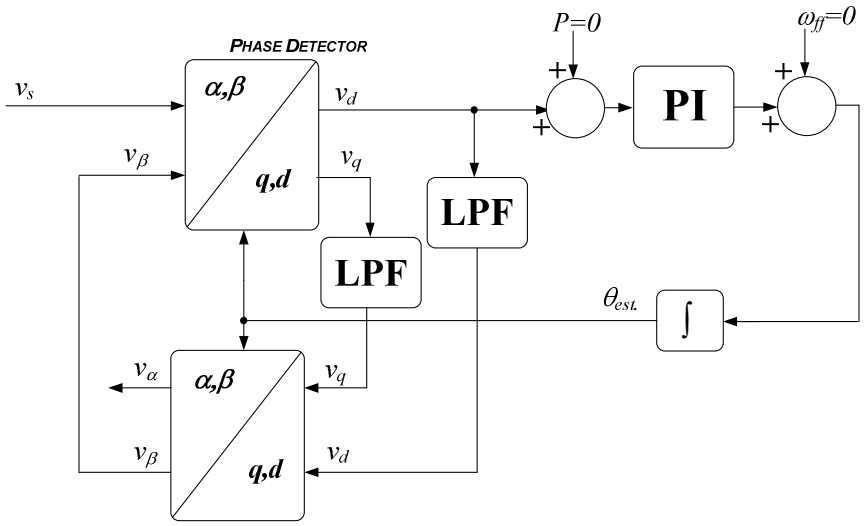


Fig. 73: Inverse Park based PLL scheme (I_PLL).

6.3 Performance Evaluation of PLLs

In general, the grid voltage is affected by some well known disturbances such as harmonics, voltage sag and swell, frequency variation and phase jump. Moreover, the voltage measurement and A/D conversion is affected by the presence of voltage offset. All non-ideal conditions cause relevant errors in the phase estimation. The validity of the estimation algorithms has been evaluated through simulations and experimental tests considering the following disturbances:

1. Presence of harmonics
2. Voltage sag
3. Voltage dips
4. Frequency variation
5. Phase jump
6. Voltage offset rejection

In all approaches, there is a trade-off between the speed of the response and the noise rejection capability.

Consequently, the gains of all analyzed PLLs have been suitably set in order to obtain similar dynamic response like in [10].

6.3.1 Presence of harmonics

According to synchronous rotating reference frame transformation, the 3rd harmonic voltage creates a ripple voltage of 150 Hz. Tests are conducted considering an additional 3th harmonic with an amplitude of 20% of the fundamental value. In

Fig. 74 are shown the estimation errors of the considered PLL algorithms, assuming that the distortion is applied at 7 s. The results show that P_PLL always shows a high ripple, E_PLL, O_PLL and I_PLL maintain a low ripple of the error while X_PLL presents a quite constant error of about -10 degrees.

6.3.2 Voltage sags

Voltage sags or swells may occur in a supply system and generally they last for a few cycles. The results shown in Fig. 75 have been obtained when a drop of voltage magnitude of

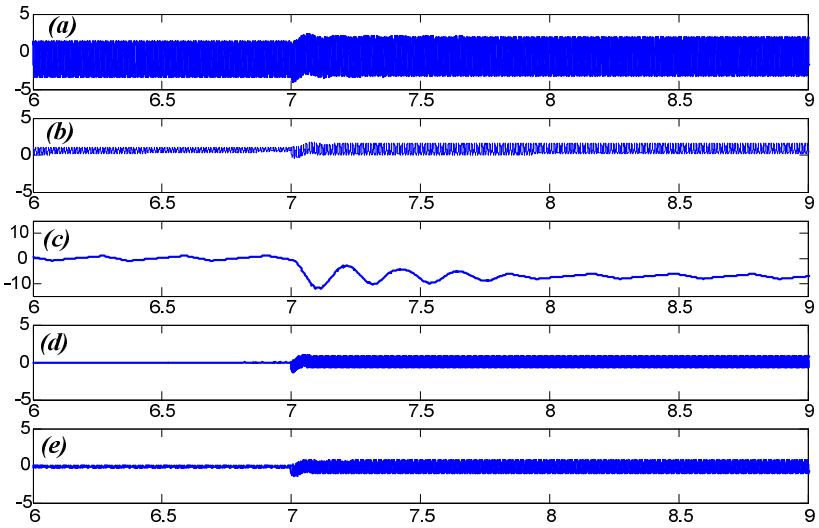


Fig. 74: Phase error with a 20% 3th harmonic.*(a)* P_PLL, *(b)* E_PLL, *(c)* X_PLL, *(d)* O_PLL, *(e)* I_PLL.*x-axis: Time [s], y-axis: errors [degrees]*.

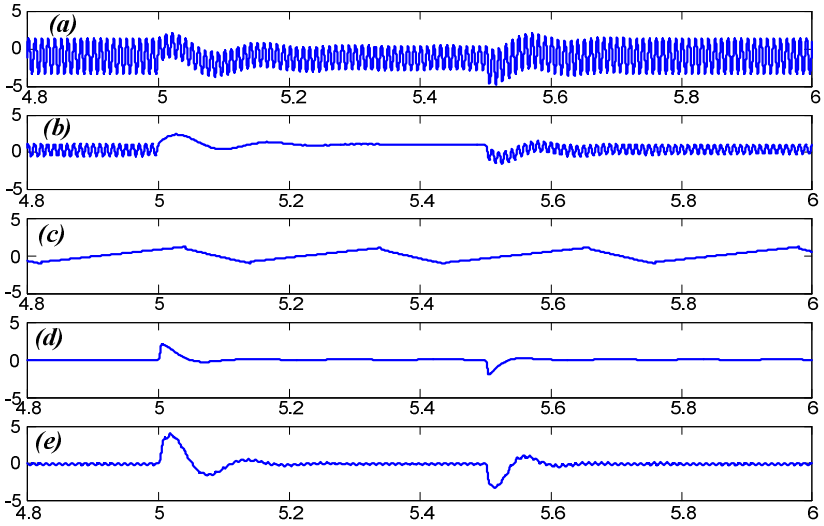


Fig. 75: Phase error during a voltage sag test.(a) P_PLL, (b) E_PLL, (c) X_PLL, (d) O_PLL, (e) I_PLL.x-axis: Time [s], y-axis: errors [degrees].

30% in all three phases has been applied. As the PLL is already phase locked with the system,there is no change in the d-axis voltage, and the q-axis voltage accurately tracks the system voltage magnitude. No disturbance has been observed in phase tracking also during a voltage swell.

6.3.3 Voltage dips

As shown in Fig 76 two simulated DIPs for each period have been inserted in grid voltage at 90° and 270°.

6.3.4 Frequency variation

To test the performance of the proposed PLL during a supply frequency variation, a step

change from 50 to 45 Hz has been given. The response of the different PLL algorithms to a 5 Hz step applied at 5 s are reported in Fig. 77, where the error amplitude of estimated angle is shown. As it is possible to note, the best result is obtained with the O_PLL, while the worse with X_PLL

6.3.5 Phase jump

Sudden phase change in load terminal voltage may occur if a large load is disconnected from the grid or due to faults in the distribution network. To test the performance of the

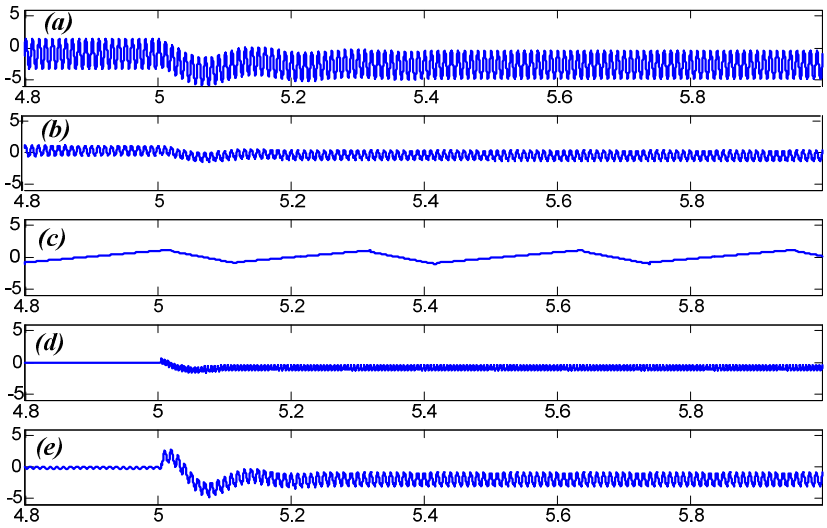


Fig 76: Voltage dips test.*(a)* P_PLL, *(b)* E_PLL, *(c)* X_PLL, *(d)* O_PLL, *(e)* I_PLL.*x-axis: Time [s], y-axis: errors [degrees]*.

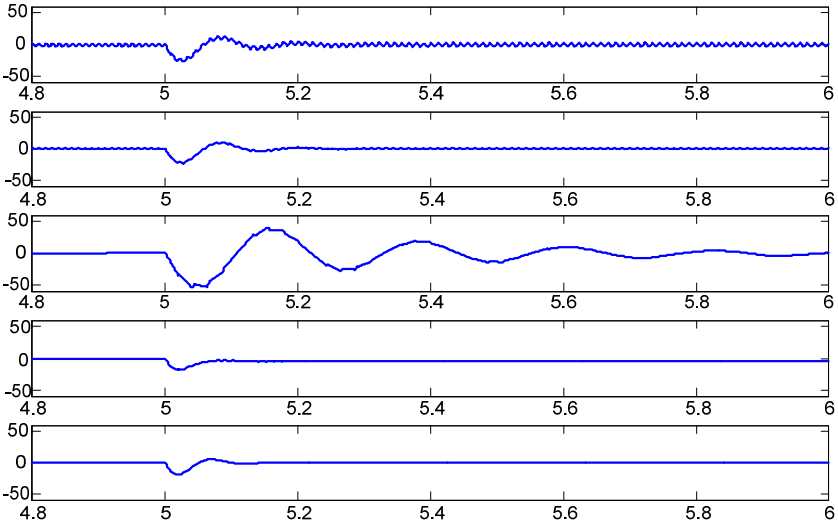


Fig. 77: Frequency variation.*(a)* P_PLL, *(b)* E_PLL, *(c)* X_PLL, *(d)* O_PLL, *(e)* I_PLL.*x-axis: Time [s], y-axis: errors [degrees]*.

considered PLLs in such a condition, a step change of 10 degree in the grid voltage has been applied. As it is possible to note, the best result is obtained by the O_PLL and I_PLL,

while the worse by X_PLL(shown in Fig. 78).

6.3.6 Voltage offset

Control algorithms for grid connection are normally implemented on microprocessors or DSP boards with low-cost Analog-to-Digital (AD) conversion. In order to be elaborated, all measurements must be acquired adding a offset in order to acquire bipolar signals. A offset must be added to the grid voltage signal before the AD conversion in order to deliver a suitable positive signal to the input of the fixed point DSPs. Therefore, an important issue associated with accurate grid voltage monitoring is the presence of a offset error in the acquired grid voltage. This voltage offset, typically introduced by the quantization and data conversion processes and causes errors for the estimated parameters of the grid voltage. Fig. 79 shows the simulation results obtained adding a DC error to the grid voltage signal equal to 10% of its amplitude. It is possible to note an increasing of the noise level to grid voltage phase estimations for all the algorithms except X_PLL. In this last technique, the additional offset produces a considerable phase shift error in the estimation.

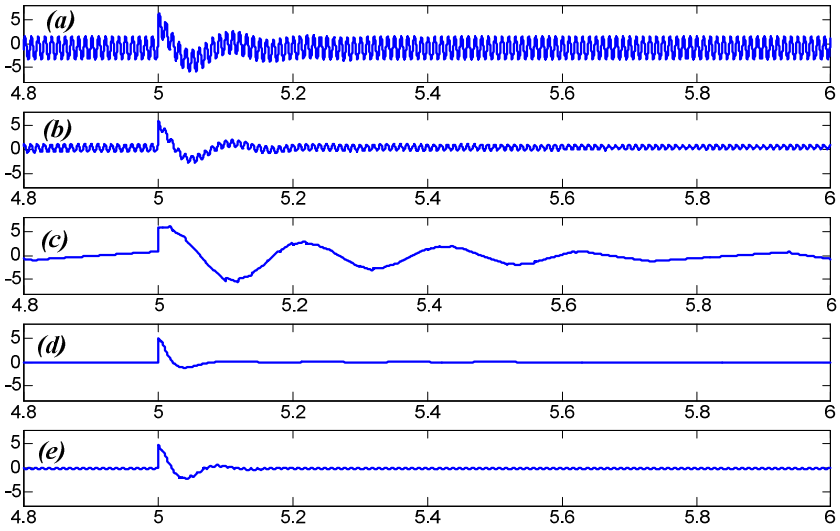


Fig. 78: Phase jump.*(a)* P_PLL, *(b)* E_PLL, *(c)* X_PLL, *(d)* O_PLL, *(e)* I_PLL.x-axis: Time [s], y-axis: errors [degrees]**.**

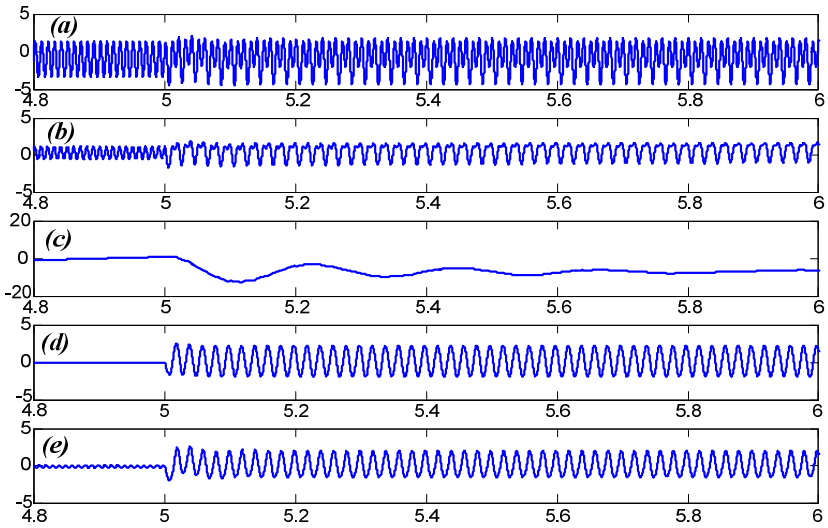
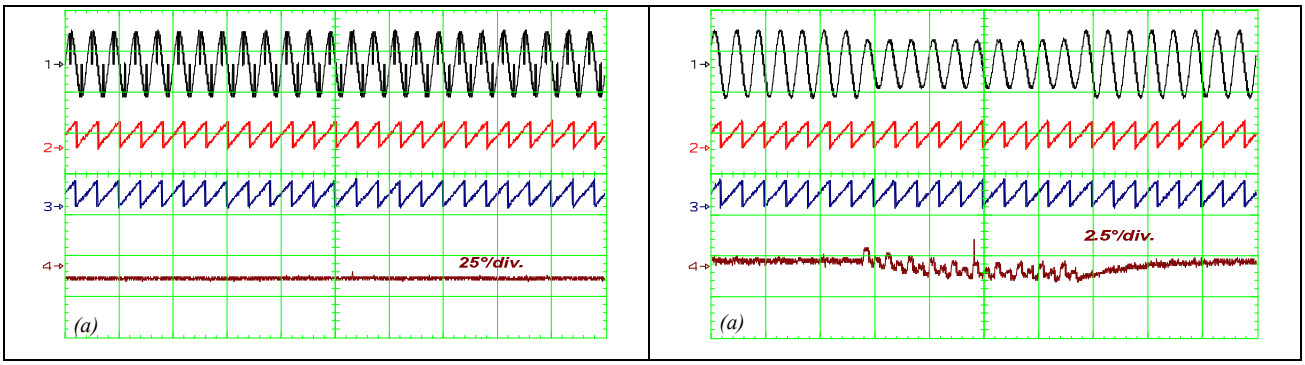


Fig. 79: Offset Rejection.*(a)* P_PLL, *(b)* E_PLL, *(c)* X_PLL, *(d)* O_PLL, *(e)* I_PLL. *x-axis: Time [s], y-axis: errors [degrees]*

6.3.7 Experimental results

In order to evaluate the performance of the PLL an experimental setup has been set, composed by a single-phase 6 kVA programmable AC power supply (ELETTROTEST TPS 6000VA) with a modified output filter to reproduce the distorted voltage and by a EMC tester (EMC-PARTNER Transient 2000) for simulating transients of different interference sources like voltage dips, sags and swells. Moreover, a standard IGBT inverter with a Maximum Power Tracking Point (MPPT) control for photovoltaic DG applications has been used.

In the considered tests, the grid voltage has been considered affected by dips of 100% at 90° and 270° of each period, as shown in Fig. 80, and sags of 200ms (10 periods of the fundamental) to 70% of nominal grid voltage (Fig: 81). In both figures (a) represent P_PLL, (b) E_PLL, (c) X_PLL, (d) O_PLL, and (e) I_PLL, as in Figs 74÷79. As it is possible to see experimental results confirm how evidenced in simulations.



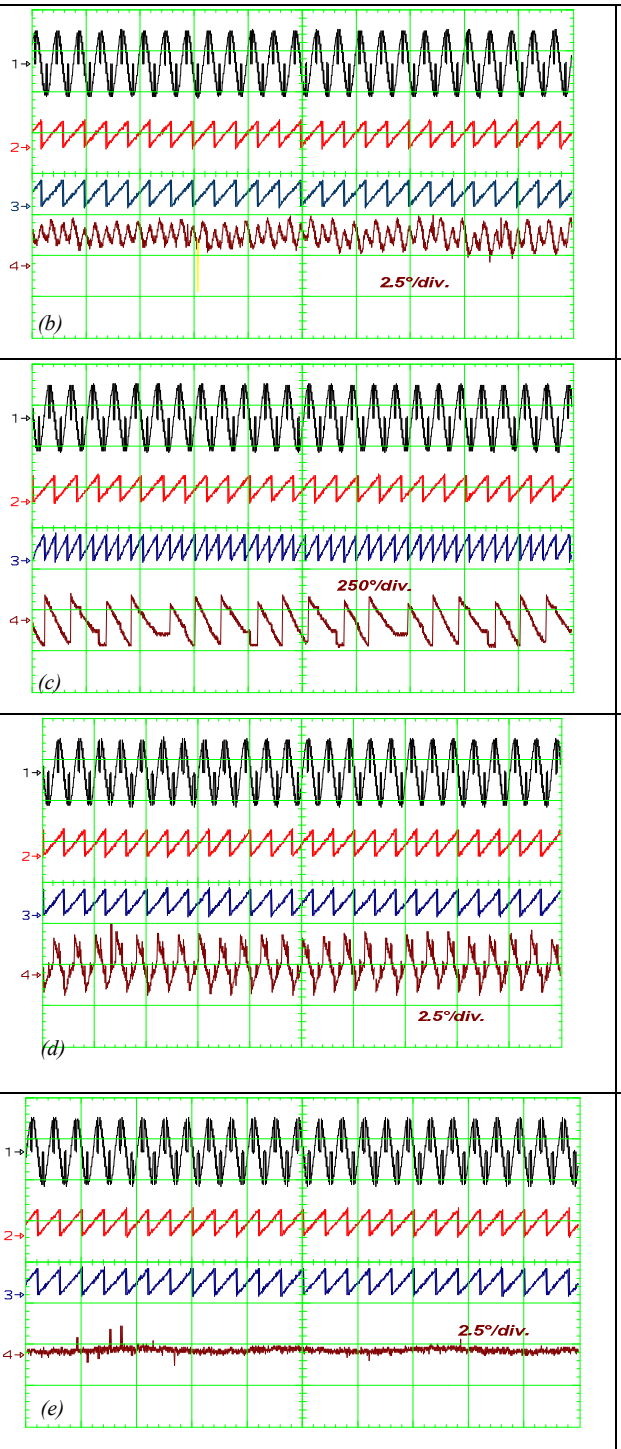


Fig. 80: Grid voltage dips. *(a)* P_PLL, *(b)* E_PLL, *(c)* X_PLL, *(d)* O_PLL, *(e)* I_PLL, ch1) Grid voltage waveform [250 V/div.]; ch2) Grid voltage phase without distortion [2π rad/div.]; ch3) Grid voltage phase with distortion [2π rad/div.]; ch4) phase error between the ideal and distorted grid voltage waveforms, *Time 50ms/div*.

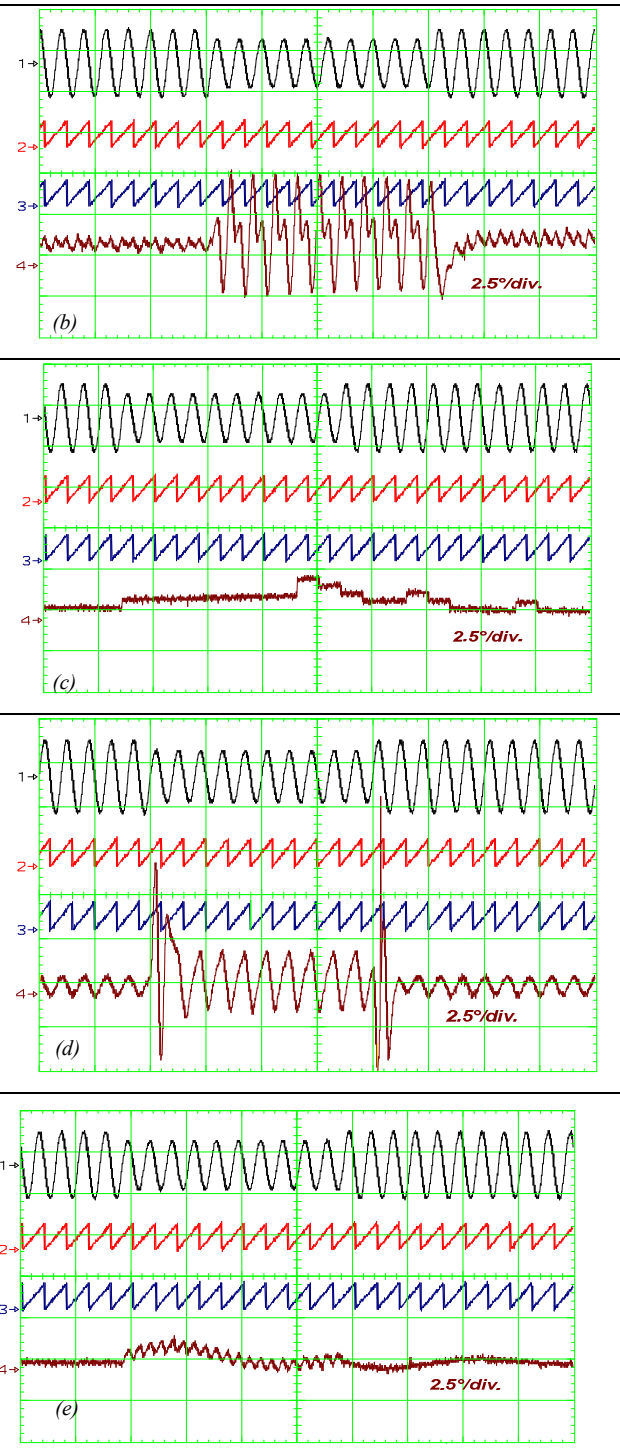


Fig: 81 Grid voltage sags. *(a)* P_PLL, *(b)* E_PLL, *(c)* X_PLL, *(d)* O_PLL, *(e)* I_PLL, ch1) Grid voltage waveform [250 V/div.]; ch2) Grid voltage phase without distortion [2π rad/div.]; ch3) Grid voltage phase with distortion [2π rad/div.]; ch4) phase error between the ideal and distorted grid voltage waveforms, *Time 50ms/div*.

Table 10 synthesizes performance of the various PLLs methods and relatively compare

their behavior. The possible range of performance has been divided into five scores from very bad to very good, as follows:

Table 10

	(a) P_PLL	*(b)* E_PLL	*(c)* X_PLL	*(d)* O_PLL	*(e)* I_PLL
1. Presence of harmonics	acceptable	very good	very bad	good	good
2. Voltage sag	acceptable	acceptable	very bad	good	very good
3. Voltage dips	bad	good	very bad	good	good
4. Frequency variation	acceptable	acceptable	bad	very good	good
5. Phase jump	acceptable	acceptable	bad	very good	good
6. Voltage offset rejection	bad	good	very bad	acceptable	acceptable

6.4 Summary

Many algorithms have been proposed for accurate estimation of the phase of the voltage in grid-connected application of distributed generation sets, based on PLL techniques. In this paper, in order to evaluate the performance in terms of noise rejection and dynamic response of most used PLL algorithms, a comparison accomplished through simulations and experimental results has been presented considering different operating conditions and voltage disturbances. The analysis conducted in the paper has shown advantages and drawbacks of various PLL structures and has been synthesized in a table useful to choose the appropriate algorithm at the design stage.

Part III

Multilevel technologies and topologies

Chapter 7
New Control of Single Phase Inverter for grid connection

Key factors, in designing solar inverters and UPS, are efficiency, reliability, performance and costs. In this chapter a comparison of the latest Power Devices Technology, available on the market, is presented. This new technologies allow very suitable design, also for the needed of the next generation of inverter.

7.1 Introduction

Nowadays, the standard, concerning grid connection, try to update the system to the reality. At the moment PV inverters feed only active power to the grid, using a power factor equal to 1. But the high penetration of PV inverter in the last years has caused some problem, because the power injected at the distribution level has been increased by the DGPS without to be update. In fact, when there are many inverters injecting active power at the same time, the voltage at Point of Common Coupling (PCC) might rise over the limits stated in the standards and trigger the safety of the inverters leading to disconnection or limit the power production below the available power. To overcome the before-mentioned disadvantage, the next standard all over the world, will impose to add a new functionality to control help the grid to keep the voltage at the PCC in the range of the limits. One of the possible way to do this is the reactive power control at the common coupling point. In principle all inverter-coupled generators, also PV generators are capable of providing reactive power. One limit is the maximum current of the power electronic elements. As long as the absolute value of the current does not exceed the limit the phase angle of the current vector can be

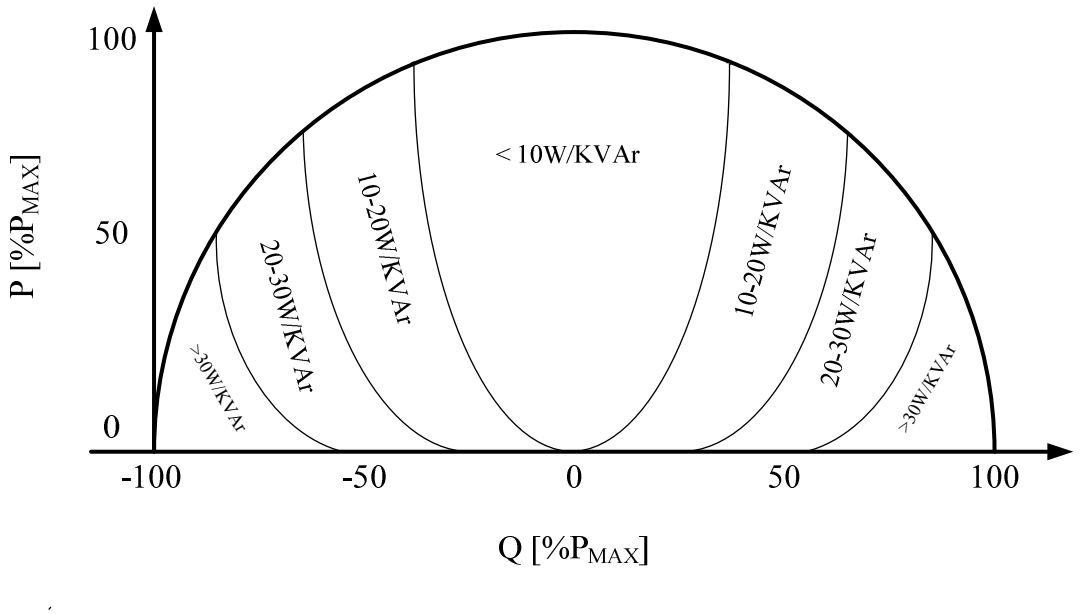


Fig. 82: Relative additional losses [W/kVAr] of reactive power supply Q [%Pmax] of an inverter with 96% maximal efficiency generating active power P [%Pmax]

arbitrarily controlled. It is possible to control active and reactive currents independently from each other. This injection of reactive power will change the structure for the new inverter.

As aforementioned, the costs of reactive power, for PV system, consist of investment costs due to over sizing, operational costs due to energy losses and additional minor cost factors. The focus here is on the dynamically changing operational costs of reactive power supply due to additional losses in the energy converters of DGs. These energy losses are compensated by active power having respective operational costs. Fig. 82 gives an example illustrating the dependencies of additional losses of reactive power supply according to actual active and reactive power supply within the semicircle according to the maximum current transfer capacity. The relative losses increase rapidly at low active power transfer with increasing reactive power supply. An important factor of the absolute value of active power losses is the converter's efficiency: the higher the efficiency the smaller the losses [33][34][35].

In this scenario new topology will appear in the next generation of PV inverter. Modified Neutral Pont Clamped inverter with new technologies of power devices are presented in this thesis..

7.2 Mixed-frequency topology review

The so-called mixed frequency inverters are becoming increasingly popular. They lead to higher system efficiency and better harmonics control. The aim of the present paragraph is to focus, in particular, on the aspects related to silicon power dissipation and efficiency as a natural consequence.

7.2.1 Focus on three-level topology

One of the most widely spread topologies in a three-phase inverter is the standard half bridge. It requires high-voltage devices (1200 V). In the past few years, the multi-level topology has become the most efficient solution on the market. This kind of system provides an output waveform very close to a sinusoidal wave with extremely low harmonic distortion.

Neutral point clamped topology, the most common structure for multilevel inverters, uses a mixed switching frequency strategy to allow for an output voltage waveform that switches through three voltage levels, which is why this topology is also known as three-level [36][37][38][39].

Hence, the requested blocking voltage for the switches is half that requested in a standard half-bridge system. This leads to a clear loss reduction, especially at high frequency. In fact, even if the number of the switches is doubled, they are switched at half voltage, thus hardly reducing the switching losses also due to the higher speed typical of lower breakdown voltage devices. Moreover, the conduction losses are kept low by the use of very low voltage drop devices in the inner part (S2 and S3 in Fig. 83).In Fig. 83, the PWM strategy is illustrated.

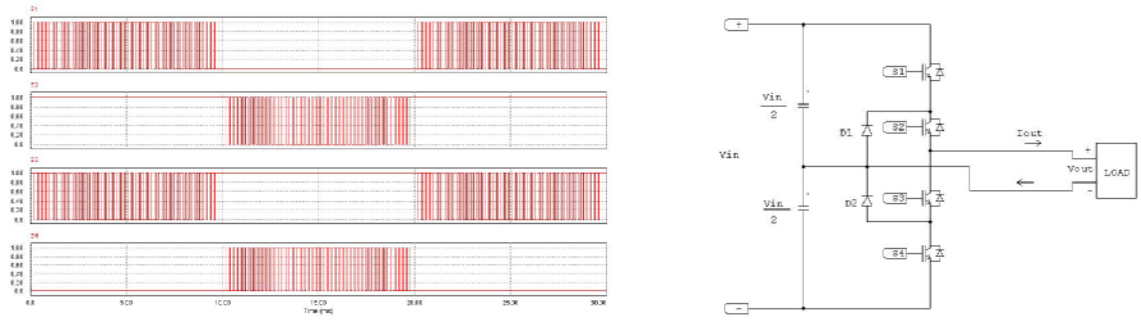


Fig. 83: (a) Neutral point clamped inverter;(b) PWM pattern

7.3 Power switches: latest technologies description and benefits

7.3.1 FDmesh II and MDmesh V

The MDmesh V family combines proprietary fifth-generation super-junction technology with our proven PowerMESH™ horizontal layout, giving superior performance compared to the competing devices.

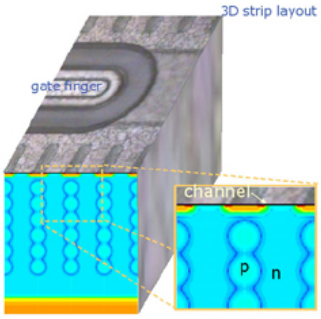
MDmesh V technology delivers the lowest on-state resistance per unit area compared to conventional MOSFETs and competing super-junction devices. Furthermore, 650 V (@25°C) MDmesh™ V series can guarantee 50 V more breakdown voltage than the standard 600 V in the Market making this technology specifically tailored for PV inverters that can benefit of devices rated at least 600V even in the worst temperature conditions (see figure 3a).

While emphasizing ultra-low on-state resistance, the devices also achieve low switching losses, thereby enabling an overall efficiency boost, higher power density and lower operating temperatures leading to better reliability.

FDmesh II family features the state of the art among fast-recovery diode MOSFETs combining enhanced switching performance with the lowest on-resistance compared to other fast recovery competing MOSFET technologies. The devices have high dv/dt rating for higher reliability during switching.

7.3.2 HF advanced planar PT IGBTs

The HF family is based on a new advanced planar technology concept to yield an IGBT with more stable switching performance (Eoff) versus temperature, as well as lower conduction losses. The W series is a subset of products tailored to high switching frequency operation. The main structural characteristics are the presence of a double drift layer with an optimized doping profile and an optimized horizontal layout on the top. The first product of the family is the STGW35HF60WD whose main features are: improved Eoff at elevated temperature, minimal tail current, low conduction losses and ultrafast soft recovery antiparallel diode.The S series is a subset of products tailored to mixed frequency topologies. You may benefit of its extremely lo voltage drop while keeping relatively low switching losses. The first product of the family is the STGW50HF60S



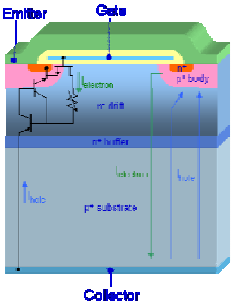


Fig. 84: Multiple Drain Mesh (MDmesh/FDmesh Series): 3D strip layout IGBT Advanced planar structure

7.4 Loss calculation on a three-level converter

This section focuses on power loss evaluation in a neutral point clamped inverter. The target for our benchmark is 3.3 kVA with a voltage bus of 800 V. In order to investigate the losses in all the possible working modes for such a topology, the analysis and comparison is based on several switching frequencies and power-factor (cos(φ)) values.

7.4.1 Devices under comparison

At the moment, there is no standard solution for this kind of converter. Both Power MOSFETs and IGBTs can offer a good performance under specific load conditions as outer devices (S1 and S4 in Fig. 83), while the best compromise between cost and performance can be achieved by using low drop IGBTs as inner switches (S2 and S3).

The following devices are compared:

S1 and S4 are MOSFETs (FDmeshII or MDmeshV) or IGBTs (advanced planar Technology [5]).

S2 and S3 are very low drop IGBT, FDmesh II or MDmesh V.

However, all the devices under comparison could be a suitable choice depending on design and cost constraints.

7.4.2 Simulation results

In order to evaluate the conduction and switching losses, the following equations are used:

$$P_{TOT} = P_{con} + P_{turn-on} + P_{turn-off}$$ Eq. 51

$$P_{cond} \approx \frac{I_{c-peak} \cdot V_{to}(T_j) \cdot D_{peak}}{4} + \frac{2R_{CE}(T_j) \cdot D_{peak} \cdot I_{C,peak}^2}{3\pi}$$ (outer IGBTs) Eq. 52

$$P_{cond} \approx \frac{2R_{DS(on)}(T_j) \cdot D_{peak} \cdot I_{C,peak}^2}{3\pi}$$ (Outer MOSFETs) Eq. 53

$$P_{sw} = \frac{\left(E_{turn-on}(I_{c-peak}, T_j) + E_{turn-off}(I_{c-peak}, T_j)\right) \cdot f_{sw}}{\pi}$$ (outer IGBTs or MOSFETs) Eq. 54

$$P_{cond} \approx \frac{I_{c-peak} \cdot V_{to}}{\pi} + \frac{R_{CE} \cdot I_{C,peak}^2}{4}$$ (inner IGBTs) Eq. 55

$$P_{cond} \approx \frac{R_{DS(on)} \cdot I_{C,peak}^2}{4}$$ (inner MOSFETs) Eq. 56

$$P_{diode-clamp} \approx I_{c-peak} \cdot V_d \left(\frac{1}{\pi} - \frac{D_{peak}}{4}\right) + R_D \cdot I_{C,peak}^2 \left(\frac{1}{4} - \frac{2D_{peak}}{3\pi}\right)$$ Eq. 57

It is worth noticing that IGBT voltage drop has been modelized using the following equation:

$$V_{CE} = V_{t_0} + R_{CE} \cdot I_C$$ Eq. 58

All the energies and parameters in the above equations are referred to the following conditions: Tj=125°C, Vin=700V, Dmax, maximum duty cycle, is 0.9 in the present job. Referring to figure 2a, D1 and D2 are ultrafast diode: STTH30R06D. In the case STGW50HF60S is used as inner device, the relative anti-parallel diode is STTH15R06D placed externally.

The lower is the power-factor the higher is the impact of the antiparallel diodes and of commutation of inner switches to the overall power losses. As a starting point let's consider PF=1. In that case IGBTs antiparallel diodes contribution can be neglected, as well as the inner IGBTs switching losses.

The following table 1 contains the overall power losses affecting a leg with three-level structure. The performances offered by using both ST IGBTs, MOSFETS or their combination are reported at different switching frequencies. In the first column referred to a certain switching frequency, single switch losses are reported, while in the second one the

total silicon losses, excluding external clamping diodes (D_1 and D_2 in Fig. 82), can be appreciated.

Table 11 Power losses affecting three-level inverters at 3 kVA and PF=1

Device	16 kHz		32 kHz		48kHz	
	Each Transistor	Total	Each Transistor	Total	Each Transistor	Total
STGW35HF60WD (outer switch)	12.97 W	45.62 W	18.87 W	57.42 W	24.75 W	69.18 W
STGW35HF60WD (inner switch)	9.84 W		9.84 W		9.84 W	
STGW35HF60WD (outer switch)	12.97 W	36.84 W	18.87 W	48.64 W	24.75 W	60.4 W
STGW50HF60S (inner switch)	5.45 W		5.45 W		5.45 W	
STW77N65M5 (outer switch)	9.39 W	29.68 W	13.54 W	37.98 W	18.03 W	46.96 W
STGW50HF60S (inner switch)	5.45 W		5.45 W		5.45 W	
STW77N65M5 (outer switch)	9.39	30.78	13.54	39.08 W	18.03	48.06 W
STW77N65M5 (inner switch)	6		6		6	

From the previous table it's clear that the best solutions, from a performance point of view, are given by either using MDmesh V or "mixing" MOSFETs and IGBTs, working respectively as outer and inner switches. Anyhow it is important to note that the lower is the load, MOSFETs based solution performs better as the reader can easily understand by looking at figure 4. This is due to the voltage drop evolution with collector and drain current.

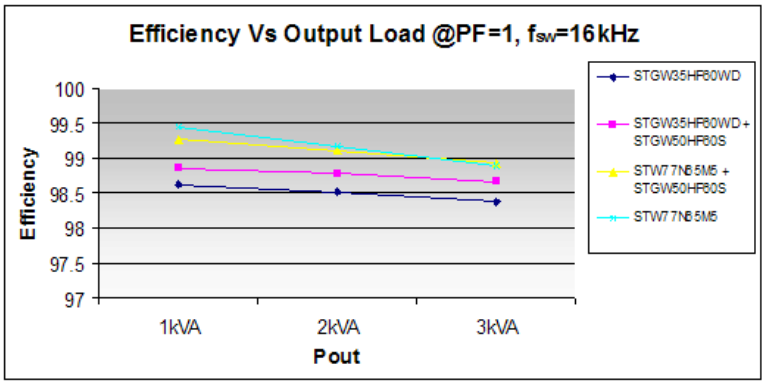


Fig. 85: Efficiency as a function of output load at fsw=16kHz, PF=1

The Fig. 85 reports the inverter efficiency as a function of the output power. The simulation includes only the losses affecting the power switches and the clamping diodes.

When PF is not unitary, losses calculation has to be performed again. In the case minimum PF is 0.9, the losses during conduction of inner and outer devices can be assumed to be the

same. On the contrary, different losses contribution is due to both outer and inner devices during switching. For that reason formula 8 will be considered instead of 4. Moreover the additional losses contribution, due to the switching of inner devices, is given by formula 9.

$$P_{sw} = \frac{\left(E_{turn-on}(I_{c-peak}, T_j) + E_{turn-off}(I_{c-peak}, T_j)\right) \cdot (1 + \cos(\varphi))}{2\pi} f_{sw} \text{ (outer, PF≠1)} \qquad \text{Eq. 59}$$

$$P_{sw} = \frac{\left(E_{turn-on}(I_{c-peak}, T_j) + E_{turn-off}(I_{c-peak}, T_j)\right) \cdot (1 - \cos(\varphi))}{2\pi} f_{sw} \text{ (inner, PF≠1)} \qquad \text{Eq. 60}$$

Table 12 Power losses affecting three-level inverters at 3 kVA and PF=0.9

Device	16 kHz		32 kHz		48kHz	
	Each Transistor	Total	Each Transistor	Total	Each Transistor	Total
STGW35HF60WD (outer switch)	12.67 W	45.62 W	18.28 W	57.42 W	23.85 W	69.18 W
STGW35HF60WD (inner switch)	10.14 W		10.43 W		10.72 W	
STGW35HF60WD (outer switch)	12.67 W	38.48 W	18.28 W	51.9 W	23.85 W	65.34 W
STGW50HF60S (inner switch)	6.75 W		7.68 W		8.80 W	
STW55NM60ND(outer switch)	11.96 W	44.18 W	17.04 W	56.6 W	22.12 W	69 W
STW55NM60ND (inner switch)	10.13 W		11.26 W		12.38 W	
STW77N65M5 (outer switch) STW77N65M5 (inner switch)	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.

The STW77N65M5 is not applicable since the body diode is not fast. For the same reason in the third row of table 2, FDMesh II has been considered as a possible option. Again, as stated before, at different load the results will be different as you may see looking at Fig. 86, where the converter efficiency as a function of load, is depicted.

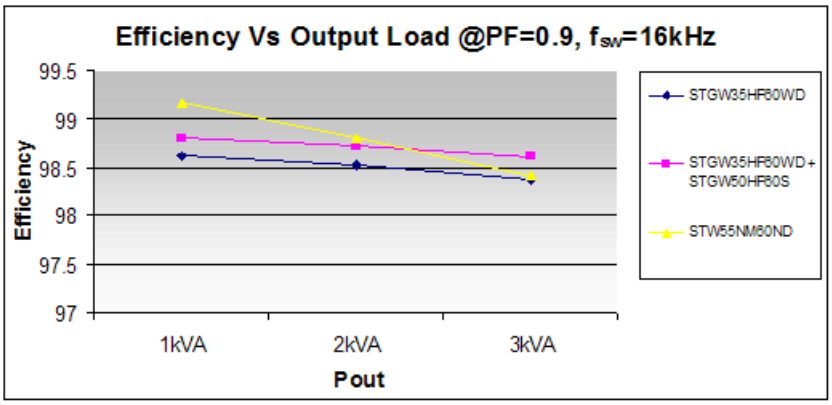


Fig. 86: Efficiency as a function of output load at fsw=16kHz, PF=0.9

7.5 Experimental results

Concerning the IGBTs solutions, the conditions showed in the previous paragraph have been verified on the bench in a real 3kVA DC-AC converter.

Case operating temperatures are reported in the table below; all the IGBTs and clamping diodes were screwed on a 0.65°C/W heat-sink, the ambient temperature was 23°C during the tests.

Table 13 IGBTs' case temperatures at different frequencies and load conditions

Load/Device		Tcase (S1,S4) (STGW35HF60WD) Tcase (S2,S3) (STGW35HF60WD) [°C]			Tcase (S1,S4) (STGW35HF60WD) Tcase (S2,S3) (STGW50HF60S) [°C]		
		16kHz	32kHz	48kHz	16kHz	32kHz	48kHz
PF=1	1kVA	35 35	42 40	51 47	34 32	41 38	49 43
	2kVA	51 50	61 56	74 66	50 44	59 50	70 61
	3kVA	64 63	79 68	96 79	60 51	76 63	92 73
PF=0.90	1kVA	35 34	42 40	51 47	34 33	40 38	50 44
	2kVA	51 51	61 56	74 67	50 46	61 53	71 63
	3kVA	64 63	79 69	96 81	62 54	76 65	94 76

All the experimental results show a perfect adherence with all the simulations done in the previous paragraph 4.

When PF is not unitary the inner switches are forced to work at high frequency too for some time (the time when output voltage and current have opposite signs). Nevertheless, the use of low drop IGBTs is still the preferred choice. This is due to the characteristics of HF series IGBTs, S family as highlithed in paragraph 7.3.2.

7.6 Summary

As anticipated in the introduction and shown in the previous paragraphs, all the devices under comparison could be a suitable choice depending on design and cost constraints. Anyhow we can try to give some comments and suggestions.

In case of PF=1, MOSFETs based solution ensures the absolute maximum efficiency especially at low load. A very cost effective solution can be achieved by mixing MOSFETs and low drop IGBTs. In fact, their combination allows reaching an excellent efficiency at a lower price.

A different scenario occurs when PF is not 1. In the present study, with minimum PF=0.9, the experimental results confirm that using the IGBTs as both outer switches (W series) and inner switches (Very Low drop, S series) the best trade-off between cost and performances can be achieved.

Chapter 8 Conclusion

The core of this thesis has been the study and implementation of converters for solar applications, focusing on control and topology. That has required multi-disciplinary knowledge and adequate know-how using software and hardware.

In order to get this goal mathematical models have been built for identify the relationships between the different elements in this system, understand the weaknesses of actual prototype.

The major focus has been on the followings aspects:

- Integration of DC/DC converter in PV cell
- Converter Topology
- Control techniques

In order to achieve the above goals, previous analysis of the following points has needed:

- Characteristics of the Photovoltaic Cell
- Characteristic of the Solar Converter
- Analysis of Control Techniques

The research project has been moved through the following steps:

State of the art analysis for each of the key points

- Definition of Models
- Simulation of new Solutions
- Experimental tests on a Real System

A careful study of integration of the DC/DC converter in a PV Cell, Algorithms for Grid Synchronization, Multilevel Topology, Control Techniques and Multilevel Inverter for Grid Connection have been performed in order to understand the advantages and disadvantages from each of them. All the analyses have been take into account the economic aspect as well, to perform a real evaluation about possible solutions on the market for the future. After the first step new solutions have been presented in all the topics analysed. Finally all the solutions have been tested and evaluated.

8.1 Achievements

The main achievements during my PhD include:

- ACModules (String Converter)
- Control techniques
- Multilevel topologies

A short list of contributions is included in the order they appear in the thesis.

- Review and simulation of ACModule topologies

A comprehensive review is presented modelling several structures: DC/DC and DCAC topologies, focusing on efficiency and cost. It has been shown that the topology proposed is one of the best compromises in cost, efficiency and high voltage gain. It is also emphasized that where isolation is needed the best topology is a classic boost interleaved with isolation and regenerative active clamp (presented in the bidirectional DC/DC converter for HEV).

- Review and comparison of control algorithm for grid synchronization

A deep review and comparison of the most popular grid synchronization algorithms have been done in this thesis. The comparison has been lead by using simulations tools (Matlab/Symulink and Dspace platform) and tested using real setup. All the algorithms have been tested and compered under several distortions conditions (reference)

- PWM techniques comparison

An analysis of the effect of the different PWM techniques applied to the PV inverter have been done, taking into account Total Harmonic Distortion factor and efficiency. The analysis has been done to the standard unipolar and bipolar technique and the mixing frequency technique. This analysis has been shown the potentiality of the mixing frequency techniques compered to the standard techniques.

- New topology

Nowadays, the standard, concerning grid connection, try to update the system to the reality. At the moment PV inverters feed only active power to the grid, using a power factor equal to 1. But the high penetration of PV inverter in the last years has caused some problem, because the power injected at the distribution level has been increased by the DGPS without to be update. In fact, when there are many inverters injecting active power at the same time, the voltage at Point of Common Coupling (PCC) might rise over the limits stated in the standards and trigger the safety of the inverters leading to disconnection or limit the power production below the available power. To overcome the before-mentioned disadvantage, the next standard all over the world, will impose to add a new control for power curtain or for reactive power injection. This injection will change the structure for the new inverter. Modified Neutral Pont Clamped inverter with new technologies POWER devices have been presented in this thesis.

Bibliography

[1] VV. AA., “Energy Efficiency – the Role of Power Electronics”, ECPE and EPE European Workshop, Brussels, 7 February, 2007.

[2] S. Kjaer, J. Pedersen, F. Blaabjerg, “ A Review of single-Phase Grid Connected Inverters for PhotoVoltaic Modules”, IEEE Trans. on Industry Applications, vol.41, no.5, Oct. 2005, pp.1292-1306.

[3] G.R. Walker, P.C. Serzia; "Cascaded DC-DC converter connection of photovoltaic modules", IEEE Transection on Power Electronics, Vol. 19 , Issue 4, 2004, pp. 1130-113

[4] Yu-Kang Lo, Huang-Jen Chiu, Ting-Peng Lee, I. Purnama, Jian-Min Wang, “Analysis and Design of a Photovoltaic System DC Connected to the Utility With a Power Factor Corrector” IEEE Transactions on Industrial Electronics, Vol. 56, no. 11, November 2009, pp. 4354-4362.

[5] Quan Li, P. Wolfs, ”Recent Development in the Topologies for Photovoltaic Module Integrated Converters”, IEEE 37th Power Electronics Specialists Conference. PESC '06, Jeju, Korea, 18-22 June, 2006, pp. 1-8.

[6] C. Rodriguez, G.A.J. Amaratunga,” Long-Lifetime Power Inverter for Photovoltaic AC Modules” IEEE Transactions on Industrial Electronics, Vol. 55, no. 7, July 2008, pp. 2593-2601.

[7] N. Femia, G. Lisi, G. Petrone, G. Spagnuolo, M. Vitelli,” Distributed Maximum Power Point Tracking of Photovoltaic Arrays: Novel Approach and System Analysis” IEEE Transactions on Industrial Electronics, Vol. 55, no. 7, July 2008, pp. 2610-2621.

[8] G. Velasco-Quesada, F. Guinjoan-Gispert, R. Pique-Lopez, M. Roman-Lumbreras, A. Conesa-Roca, “ Electrical PV Array Reconfiguration Strategy for Energy Extraction Improvement in Grid-Connected PV Systems” IEEE Transactions on Industrial Electronics, Vol. 56, no. 11, November 2009, pp. 4319-4331.

[9] R. Gules, J. De Pellegrin Pacheco, H.L. Hey, J. Imhoff," A Maximum Power Point Tracking System With Parallel Connection for PV Stand-Alone Applications" IEEE Transactions on Industrial Electronics, Vol. 55, no. 7, July 2008, pp. 2674-2683.

[10] B. Sahan, A.N. Vergara, N. Henze, A. Engler, P. Zacharias," A Single-Stage PV Module Integrated Converter Based on a Low-Power Current-Source Inverter" IEEE Transactions on Industrial Electronics, Vol. 55, no. 7, July 2008, pp. 2602-2609.

[11] M.J.V. Vazquez, J.M.A. Marquez, F.S. Manzano," A Methodology for Optimizing Stand-Alone PV-System Size Using Parallel-Connected DC/DC Converters" IEEE Transactions on Industrial Electronics, Vol. 55, no. 7, July 2008, pp. 2664-2673.

[12] M. Cacciato, A. Consoli, V. Crisafulli, "Power Converters for PV Generation Systems in Smart Grid Applications", Proc. of COBEP'09, Bonito, Brasile, 28-30 September 2009, pp 1-6.

[13] Rong-Jong Wai, Chung-You Lin, Yung-Ruei Chang, "High Step-Up Bidirectional Isolated Converter With Two Input Power Sources" IEEE Transactions on Industrial Electronics, Vol. 56, no. 7, July 2009, pp. 2629-2643.

[14] M. Cacciato, A. Consoli, R. Attanasio, F. Gennaro, "Soft-switching Converter With HF Transformer for Grid-Connected Photovoltaic Systems", IEEE Transactions on Industrial Electronics, Vol. 57, no. 5, May 2010.

[15] Lung-Sheng Yang, Tsorng-Juu Liang, Jiann-Fuh Chen, "Transformerless DC–DC Converters With High Step-Up Voltage Gain" IEEE Transactions on Industrial Electronics, Vol. 56, no. 8, August 2009, pp. 3144-3152.

[16] S.J. Chiang, Hsin-Jang Shieh, Ming-Chieh Chen " Modeling and Control of PV Charger System With SEPIC Converter" IEEE Transactions on Industrial Electronics, Vol. 56, no. 11, November 2009, pp. 4344-4353.

[17] Byung-Duk Min, Jong-Pil Lee, Jong-Hyun Kim, Tae-Jin Kim, Dong-Wook Yoo, Eui-Ho Son, "A New Topology With High Efficiency Throughout All Load Range for Photovoltaic PCS" IEEE Transactions on Industrial Electronics, Vol. 56, no. 11, November 2009, pp. 4427-4435.

[18] M. Cacciato, R. Attanasio, A. Consoli, F. Gennaro "An Innovative Boost Converter for Fuel Cells Stationary Generation Systems", IEEE 30th Annual Conference of the Industrial Electronics Society, IECON'04, 2-6 November, 2004, Busan, Korea.

[19] P. Klimczak, S. Munk-Nielsen, "Boost Converter with Three-State Switching Cell and Integrated", Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual, Febraury 2009 , pp. 1378-1383 .

[20] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, R. Gules, "Voltage Multiplier Cells applied to non-isolated DC-DC converter," IEEE Transactions on Power Electronics , vol. 23, no 2, March 2008, pp. 871–887.

[21] B.P. Divakar, K.W.E. Cheng, D.H. Wang, Dong Ping; K.F. Kwok, "Implementation of a Voltage Multiplier Integrated HID Ballast Circuit With Dimming Control for Automotive Application" IEEE Transactions on Industrial Electronics, Vol. 56, no. 7, July 2009,pp. 2479-2492.

[22] Yungtaek Jang, Milan M. Jovanovic, "New two-inductor boost converter with auxiliary transformer", IEEE Transactions on Power Electronics, Vol. 19, no. 1, January 2004, pp.169-175.

[23] Sung-Sae Lee, Seung-Wu Rhee, Gun-Woo Moon, "Coupled Inductor Incorporated Boost Half-Bridge Converter With Wide ZVS Operation Range" IEEE Transactions on Industrial Electronics, Vol. 56, no. 7, July 2009, pp. 2505-2512.

[24] T. Nussbaumer, K. Raggl, J.W. Kolar, "Design Guidelines for Interleaved Single-Phase Boost PFC Circuits" IEEE Transactions on Industrial Electronics, Vol. 56, no. 7, July 2009, pp. 2559-2573.

[25] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1398-1409, Oct. 2006.

[26] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications" IEEE Trans. on Industrial Electronics, Vol. 55, No. 8, pp. 2923-2932, August 2008.

[27] D. Yazdani, M. Pahlevaninezhad, A. Bakhshai, “Single-Phase grid-synchronization algorithms for converter interfaced distributed generation system,” Canadian Conference on Electrical and Computer Engineering,CCECE’09, 3-6 May 2009, pp. 127-131.

[28] S.M. Silva, B.M. Lopes, B.J.C. Filho, R.P. Campana, W.C. Bosventura, “Performance evaluation of PLL algorithms for single-phase grid-connected systems,” Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE, Volume 4, 3-7 Oct. 2004 Page(s):2259

[29] M. Karimi-Ghartemani and M. R. Iravani “A nonlinear adaptive filter for online signal analysis in power system: Applications,” IEEE Trans. Power Del., vol. 17, pp. 617, Apr. 2002.

[30] Consoli, A.; Scarcella, G.; Scelba, G.; Testa, A.; Royak, S.;Phase modulation-based technique for saliency position estimation of IPMSMs Energy Conversion Congress and Exposition, 2009. ECCE. IEEE 20-24 Sept. 2009 Page(s):2489 - 2495

[31] S. Shinnaka “A Robust Single-Phase PLL System With Stable and Fast Tracking,” IEEE Trans. Industry Applications, vol. 44, no. 2, pp. 624-633, March/April 2008.

[32] S. M. Silva, B. M. Lopes , B. J. C. Filho , R. P. Campana and W. C. Boaventura “Performance evaluation of PLL algorithms for single-phase grid-connected systems,” 39th Conf. Rec. IEEE IAS Annu. Meeting, vol. 4, Aug. 2004, pp. 2259-2263.

[33] N. Mohan, T. Undeland, W.P. Robbins: "Power Electronics: Converters, Application, and design 3rd", Wiley; 3 edition, October 10, 2002

[34] [2] J. Holtz, T.A.Lipo, “Pulse Width Modulation for Power Converters: Principles and Practice” IEEE Press Series on Power Engineering.

[35] [3] M. Cacciato, A. Consoli, V. Crisafulli, G. Frascatore “Tecnica PWM a Basse Perdite per Sistemi di Generazione Monofase Connessi alla Rete”: Convegno Nazionale AEIT, Catania 2009

[36] [4] S. Riming, G. Zhenhong, C. Liuchen ”A PWM Strategy for acustic Noise Reduction for Grid-Connected Single-Phase Inverters” Applied Power Electronics Conference, APEC 2007, pp. 301-305

[37] T. Bruckner, S. Bemet, “Loss balancing in three-level voltage source inverters applying active NPC switches”, Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE, pp. 1135-1140 vol.2

[38] Jung-Dae Lee, Tae-Jin Kim, Jae-Chul Lee, Dong-Seok Hyun, “An improved strategy to detect the switching device fault in NPC inverter system”, 7th Internatonal Conference on Power Electronics, 2007, ICPE '07, 22-26 Oct. 2007, pp 132-136.

[39] D. Floricau, E. Floricau, G.Gateau,” Three-level active NPC converter: PWM strategies and loss distribution”, 34th Annual Conference of Industrial Electronics, 2008. IECON 2008, 10-13 Nov. 2008,pp. 3333-3338

[40] Meng Qing-yun, Ma Wei-ming, Sun Chi, Jie Gui-sheng, Qi Wei,”Analytical calculation of the Average and RMS currents in Three-Level NPC Inverter with SPWM”, 35th Annual Conference of Industrial Electronics, 2009. IECON 2009, 3-5 Nov. 2009,pp. 243 – 248

[41] Ma Lin, Jin Xinmin, T. Kerekes, M. Liserre, R. Teodorescu, P. Rodriguez, ”The PWM Strategies of Grid-connected Distributed Generation Active NPC Inverters”, Energy Conversion Congress and Exposition, 2009, ECCE 2009, 20-24 Sept. 2009, pp. 920-927

[42] C. M. Liaw, T. H. Chen, T. C. Wang, G. J. Cho, C. M. Lee, C. T. Wang, “Design and Implementation of a Single Phase Current-Forced Switching Mode Bilateral Converter”, IEE Proceedings , no.3, May 1991, pp 129-136,

[43] CEI EN 61727 (CEI 82-9): Sistemi fotovoltaici (FV) - Caratteristiche dell’interfaccia di raccordo con la rete;

[44] CEI EN 61000-3-2 (CEI 110-31): Compatibilità elettromagnetica (EMC) - Parte 3: Limiti - Sezione 2: Limiti per le emissioni di corrente armonica (apparecchiature con corrente di ingresso “ = 16 A per fase);