micro-tip to perturb the polarization on the ferroelectric capacitor. The signal generator has been used to mimic en external target electric field signal. Figure 4-32c shows an example of the ST output voltage signal visualized by the oscilloscope after applying the perturbing signal. As in the previous case with the Penn State capacitor the perturbation on the sensing electrode produce an "amplitude modulation" (the low frequency signal) of the relative high frequency driving voltage.

A data acquisition campaign have been carried out for a more deep investigation. Acquired data have been then processed by Matlab® scripts and results are given in the sequel. Figure 4-33 shows examples of hysteresis of the ferroelectric capacitor for a driving signal of $6V_{pp}$@1kHz and four amplitudes (5 mV, 100 mV, 500 mV and 1V) of the potential applied to the sensing electrode at a frequency of 10Hz. The potential applied to the central plate produces a perturbation of the hysteresis whose degree depends on the potential amplitude itself. Hysteresis are given in the voltage domain taking in account the driving voltage signal and the ST circuit output voltage signal which are related to the E-field applied to the ferroelectric and the polarization in the ferroelectric by equations (4.4) and (4.5), respectively.

Two examples of Sawyer-Tower output voltage signals for a driving voltage of 6 V_{pp} @ 510 Hz amplitudes (1 V and 500 mV) of the potential applied to the tip at the frequency of 10 Hz are given in Figure 4-34. The dependence of the "amplitude modulation" of the driving signal on the amplitude of the perturbing potential is clearly visible. A spectral analysis of the signals has been performed by the power spectral density (PSD) to evaluate the effect of the potential on the polarization.

Analysis of the PSD reveals that with the application of the potential a peak in the PSD in correspondence to the frequency of the signal applied to the sensing electrode appears. The peak amplitude is depending on the potential amplitude. Examples of PSD together with a zoom in correspondence of the frequency of the disturbing potential are reported in Figure 4-35.

A comparison of the peak amplitude of the PSD at 1 Hz and 10 Hz for various amplitudes of the potential applied to the sensing electrode and

a driving voltage of 6 V_{pp} @ 510 Hz and 1 kHz is given in Figures 4-36 (a) and (b), respectively. Results are summarized in Figure 4-37.

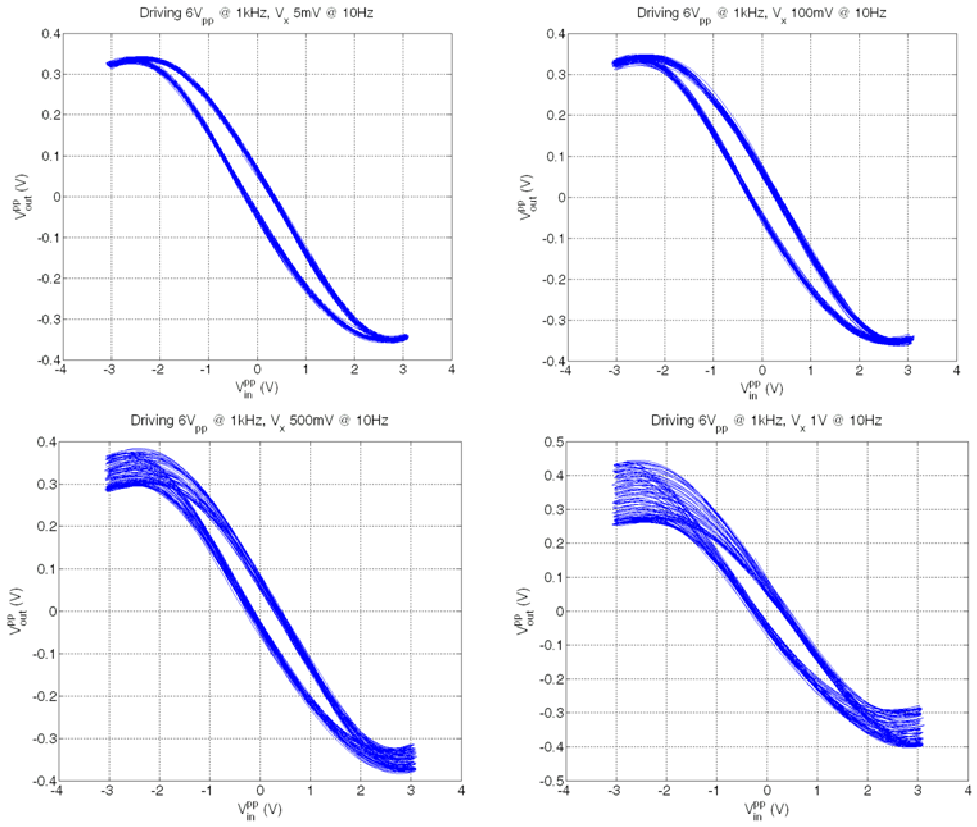
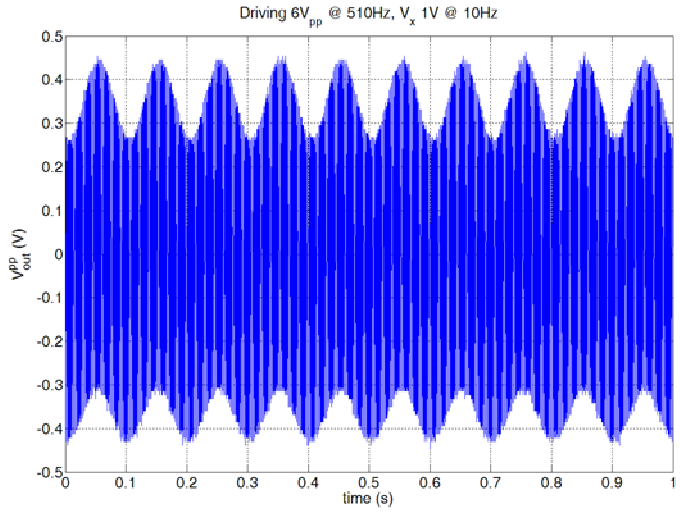
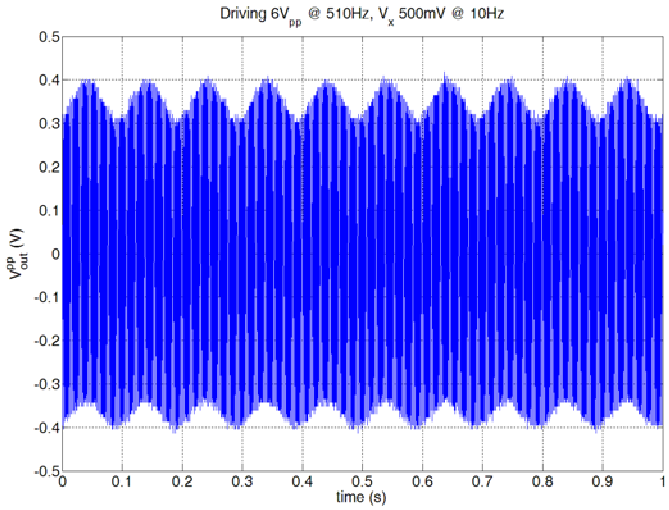


FIGURE 4-33 Effect on the ferroelectric hysteresis of the potential applied to the micro-tip by the signal generator used to mimic an external target E-field.



(a)



(b)

FIGURE 4-34 Examples of Sawyer-Tower output voltage signals for a driving voltage of 6 V_{pp} @510 Hz and for two amplitudes (a) 1V and (b) 500 mV of the potential applied to the tip at the frequency of 10 Hz.

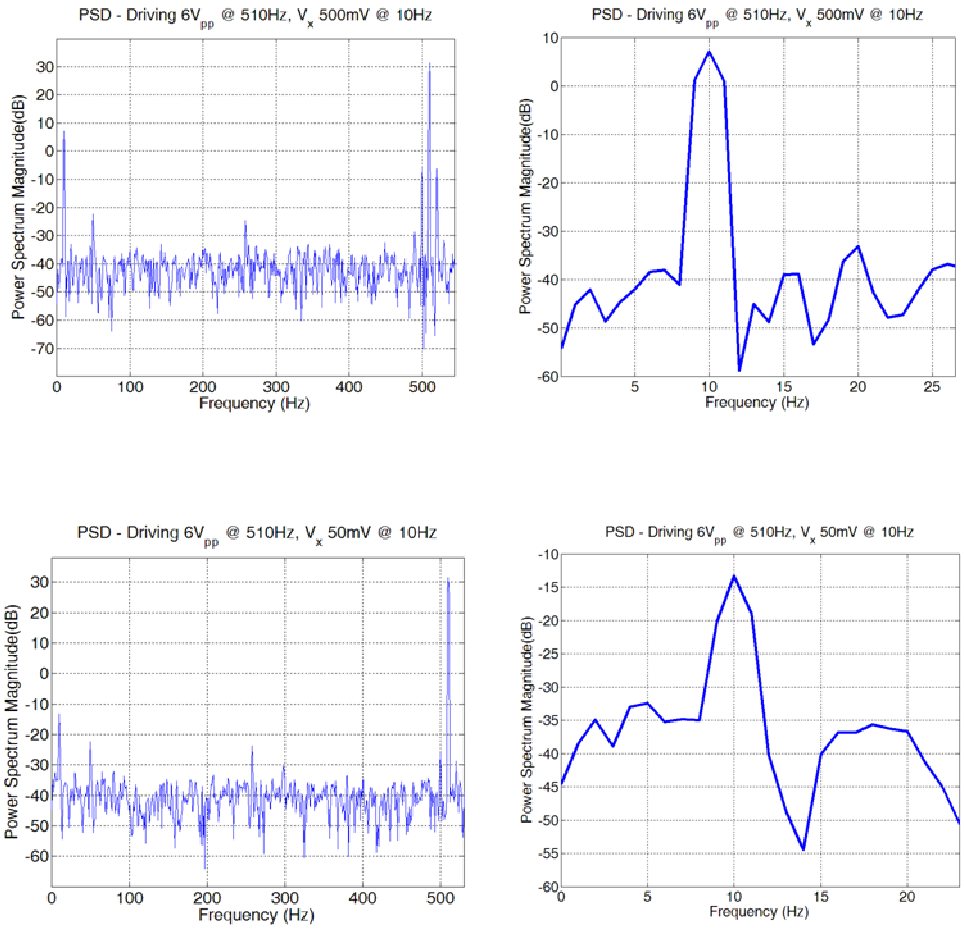
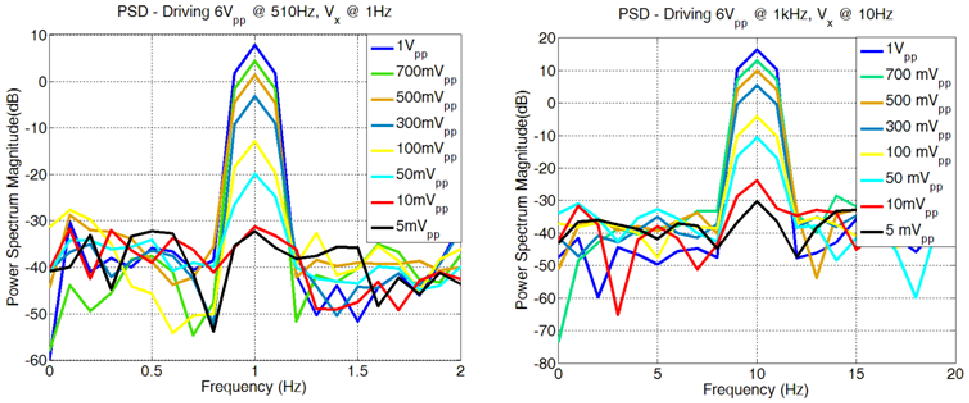


FIGURE 4-35 Examples of PSD together with a zoom in correspondence of the frequency of the disturbing potential.



(a) (b)

FIGURE 4-36 A comparison of the peak amplitude of the PSD at 1 Hz (a) and 10 Hz (b) for various amplitudes of the potential applied to the sensing electrode and a driving voltage of 6 Vpp @ 510 Hz and 1 kHz.

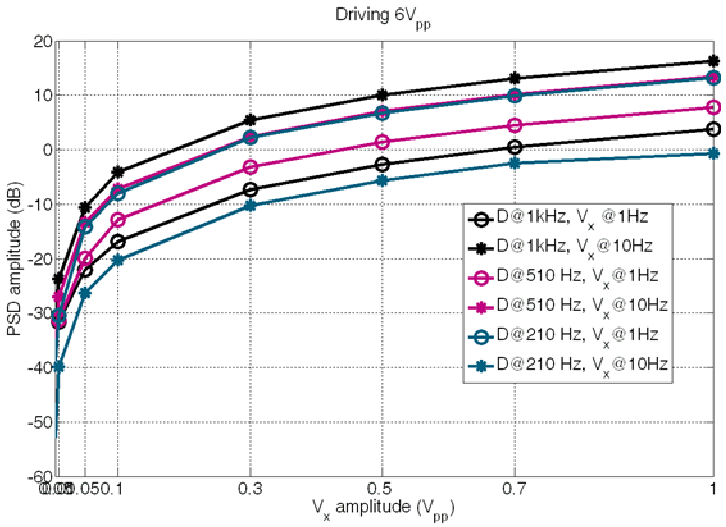


FIGURE 4-37 Trend of the PSD amplitude at the frequencies of 1 Hz and 10 Hz for various amplitudes of the potential applied to the micro-tip and driving voltage of 6 V_{pp} at the frequencies of 210 Hz, 510 Hz and 1 kHz.

5.3 THE DIEES CAPACITOR

Above investigation has had a twofold target: to verify the suitability of the Radiant technology to our scope and to have a further confirmation of the soundness of our idea with a capacitor having a structure almost similar to the ideal one. Established it, with very propelling results, we started the design of a new integrated ferroelectric capacitor with the central sensing electrode bonded to a metal pad on the die to make possible to contact it to an external charge collector. This work, including checking and cross-checking and concurrent changes in the technology that is still under development and which has compelled to review the design, has taken nearly an year and a half and has been carried out with the continuous support of Dr. Joe Evans founder of Radiant Technology Inc. The first packaged capacitors have been shipped us in mid-September then only in the last month it has been possible to work on them.
In next sections more details on the structure of the capacitors will be given together with the results of the behavior characterization in the P-E domain and the experimental results of the investigation of the behavior of the capacitor as single E-field sensor. Afterwards the investigation of the coupled configuration will be discussed.

5.3.1 THE TECHNOLOGY AND THE LAYOUT

The Radiant's 5μ integrated PZT capacitor process technology [166] has been discussed in section 5.2. The same technology has been employed to fabricate the DIEES capacitors with the exception of the ferroelectric material that in these new capacitors it consists of approximately 0.25 microns (2550 Å) of 4% niobium doped 20/80 PZT, designated 4/20/80 PNZT at Radiant. The LSCO electrodes use a 50:50 ratio of strontium to lanthanum.
Radiant uses two contact printers for its photolithography steps. The first is a Kasper 2000 3" printer. The Kasper has been re-manufactured by Quintel and modified by Radiant to work with 4" or 100 mm wafers. It has a clear area of 3.6" or 91.44 mm and doesn't print any features outside of the radius of 1.8" or 45.7 mm from the center of the wafer.

The Quintel is the primary printer used by Radiant for all but the backside and trench layers. Radiant has an alignment tolerance of 1 μ layer-to-layer on the Quintel printer.
The second system is a Suss MA/BA-6. The MA/BA-6 can handle 6" wafers and execute back-to-front alignment. The back-to-front alignment has a minimum specification of 5 μ. The MA/BA-6 is used primarily for the backside and trench layers [166].
Capacitors have been designed by the ICWIN layout editor [167] a free-ware tool used and suggested by Radiant, capable of streaming and unstreaming the GDSII file format used by the mask manufacturers. Radiant has created a starter project for the IC Editor called STARTW. It consists of a 4" wafer with alignment marks and process test cells already laid out on the wafer. Layout process has started from this project placing the new developed cells on the wafer without having to be concerned with alignment mark placement.
The command file RC104.CMD for the STARTW project defines the standard layers used by Radiant in its processes. Design rules for the 5μ process technology have been provided us by courtesy of Radiant Technology Inc.
The whole wafer with all the designed structures placed in it is shown in Figure 4-38. The wafer is divide in two main regions: the upper side of the wafer is dedicated to the ferroelectric capacitors while in the bottom side others devices (MEMS suspended structures) have been placed. These latter devices are not of interest for us in this work. The test structures and the alignment cells are easy to recognize in the central part of the wafer placed between the two regions. Others are placed in both the two regions among the cells.

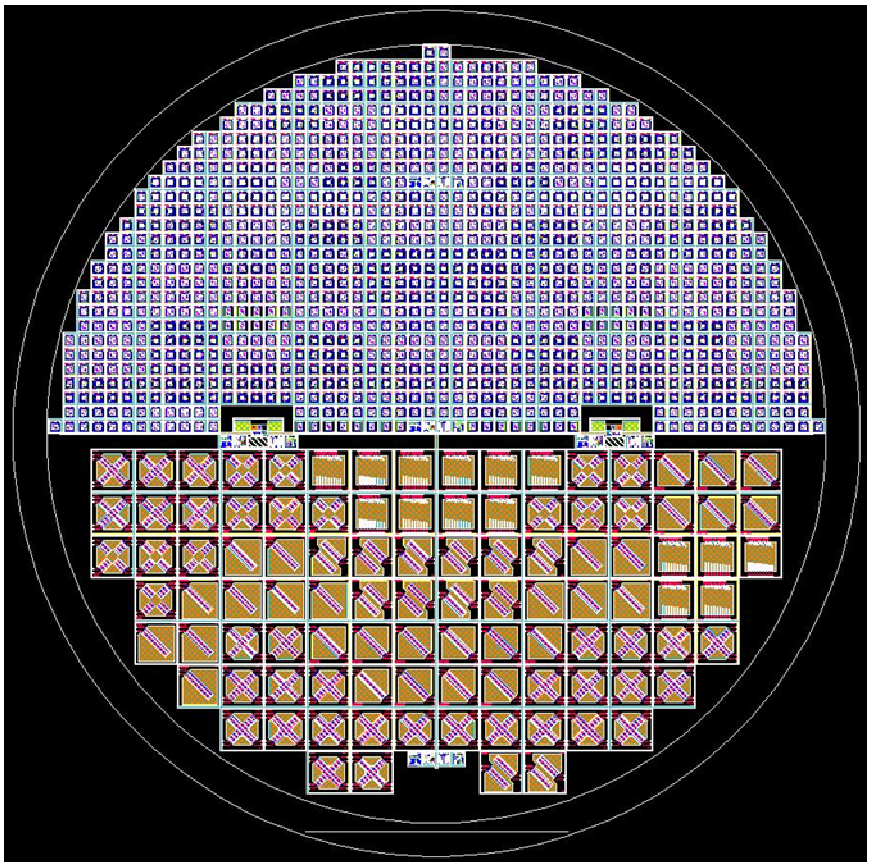


FIGURE 4-38 The wafer with all the designed structures. The upper side of the wafer is dedicated to the ferroelectric capacitors while in the bottom side others devices (MEMS suspend structures) have been placed.

Capacitors were designed with different sizes of square shaped driving and sensing electrodes and changing the distances between them.
To obey the design rules we choose to fix the size of the bottom driving electrode (1010μm) and change only the size of the top driving electrode so changing even the size of the polarized region of the ferroelectric layer and the capacitance. Different sizes of the charge collectors have been then designed to change the size of the sensing region. In total a set of 22 different capacitors have been designed. Examples of layout of the capacitors are given in Figure 4-39. In Figure 4-39a the driving and

the sensing electrodes are highlighted. Every single capacitor is contained in a separate cell having the size of the die which will host it. Every capacitor is then replicated many times and grouped in sets of five-to-ten and placed in different locations in the upper side of the wafer. Every set of ten capacitors is replicated at least four times in the wafer. In all a total of 1070 capacitors have been placed in the wafer. A summary of all the ferroelectric capacitors designed together with the list of groups for each capacitor is given in Appendix.

This strategy allow us to have sets of capacitors having the same characteristics (on average) and which we can consider (without fear of big mistakes) ideally equals. This will come in handy when we will discuss the coupled configuration.

Moreover the placement of the sets of capacitors in different locations in the wafer allow us to perform tests on the reliability of the process technology and on the ferroelectric material.

To the purpose to be able to recognize every capacitor some characteristics sizes have been reproduced on the die using the metal layer. In Figure 4-39a the relation between the sizes indicated in the upper part of the die and the geometrical features is highlighted. Furthermore, to univocally recognize the position of the capacitor on the wafer a binary code has been added at the bottom right corner of the die. A real microscope image of a capacitor is given in Figure 4-40 together with zoom in the regions where metal stripes bond the driving and sensing electrodes.

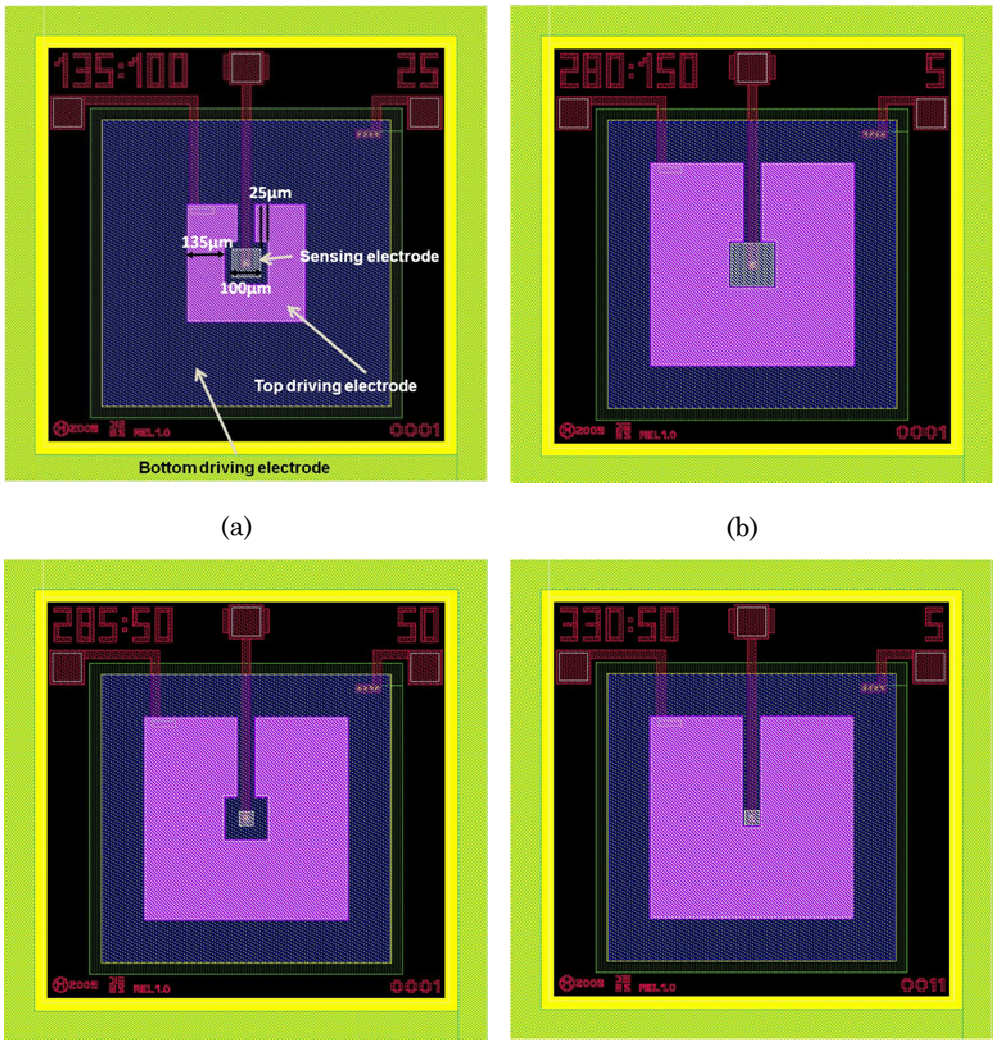


FIGURE 4-39 Examples of layout of the capacitors. Four capacitors with different sizes of the top driving electrode and of the sensing electrode are shown. In (a) the driving and sensing electrodes are highlighted together with the relation between the sizes indicated in the upper part of the die and the geometrical features. The binary code in the bottom right corner of the die allows to univocally recognize the position of the capacitor on the wafer.

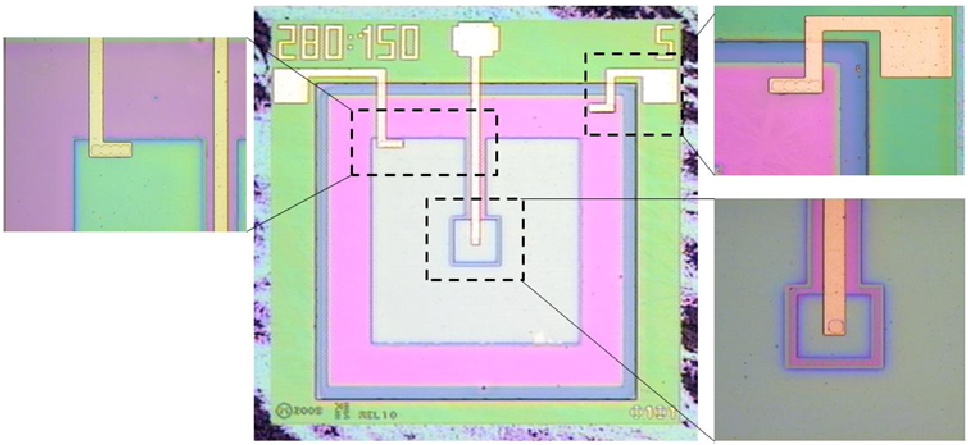


FIGURE 4-40 Microscope image of a capacitor and zoom of the regions where metal stripes bond the two driving electrode and the sensing electrode.

Each die containing one capacitor is packaged in a four-lead TO-18 header. A schematic of the header with the pin assignments is shown in Figure 4-41. One package lead is connected to the case and is labeled GND or CASE. Optionally it can be connected to the circuit ground to provide a Faraday shield around the capacitor. The COMMON lead is bonded to the bottom electrode while the other two electrodes have separate leads labeled as COMMON OUTER and SMALL CENTER for the top driving electrode and the sensing electrode, respectively.
A picture of the packaged capacitors is given in Figure 4-42.

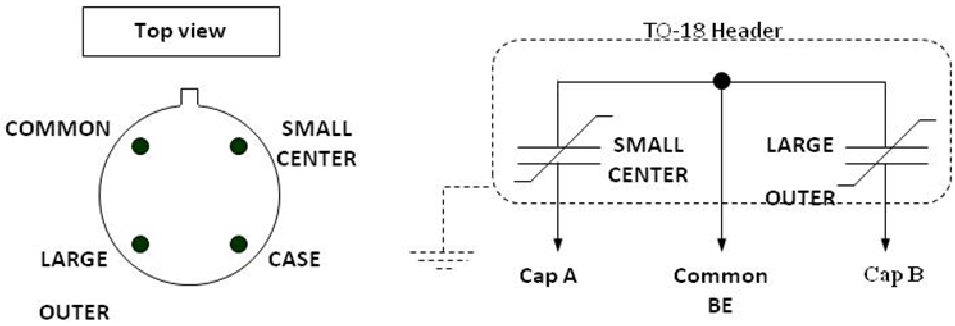


FIGURE 4-41 Schematic of the four-lead TO-18 header used to package the die with the single capacitor showing the pin assignment.