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A CMOS Frequency Synthesizer for Wireless Sensor Network transceivers

TESI DI DOTTORATO

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Chapter 1

Introduction

1.1 Motivation and thesis overview

In last years the wireless market has rapidly expanded to unimaginable dimensions. Wireless systems are quickly penetrating all aspects of our lives, from job to spare time, evolving from luxury items to indispensable tools.

The development of ultra low-power devices for wireless communication systems may extend the frontiers of sensor networks to innovative home and automotive applications, advanced healthcare treatments, and complex structures monitoring. These applications have common requirements, such as high nodes autonomy, small physical size, and high reliability.

Nowadays, the radio front end is the most critical part of the wireless node since it significantly contributes to the entire system power consumption and greatly affects the overall performance. In particular the frequency synthesizer, used for local oscillator signal generation, is a key block since must guarantee high performance with extremely low current consumption.

The work, which is the subject of this thesis, mainly focuses on the design, implementation and experimental characterization of a low-power wideband frequency synthesizer usable for Wireless Sensor transceivers.

The thesis is organized as follows. This first introductive chapter deals with a brief overview concerning the Wireless Sensor Network communication. Chapter 2 discusses the design key-points for implementing

an ultra low-power wideband radio transceiver for sub-GHz Wireless Sensor Networks. The attention is then moved to the frequency synthesizer, which is the main topic of this thesis. Chapter 3 and 4 are the core of this dissertation, since they describe the voltage controlled oscillator and the quadrature generator, respectively, which are the most critical part of the proposed frequency synthesizer. Chapter 5 summarizes the experimental results. The following chapter draws the conclusions, whereas a closing chapter makes a list of published papers related to this PhD work. Further publications have not yet submitted due to fabrication and measurement delays.

1.2 WSN applications

A Wireless Sensor Network (WSN) consists of a large number of low-cost, low-power, and multifunctional sensor nodes deployed in a region of interest. These sensor nodes are small in size, but are equipped with sensors, embedded microprocessors and radio transceivers, and therefore have not only sensing capability, but also data processing and communicating capabilities [1]. They communicate over a short distance via a wireless medium and collaborate to accomplish a common task, for example environment monitoring or industrial process control.

Sensors can be used to detect or monitor a variety of physical parameters or conditions, for example light, sound, humility, pressure, temperature, soil composition, air or water quality, attributes of an object such as size, weight, position, speed, and direction.

Wireless sensors have significant advantages over conventional wired sensors. They can not only reduce the cost and delay in deployment, but also be applied to any environment, especially those in which conventional wired sensor networks are impossible to be deployed. The availability of low-cost sensors and wireless communication systems make possible the development

of a wide range of applications.

Environmental monitoring is one of the earliest applications of sensor networks. WSNs can be deployed on the ground or under water to monitor air or water quality, can be used to monitor biological or chemical hazards, or can be densely deployed to detect natural disasters. Furthermore, a WSN can be used to monitor a variety of environmental parameters or conditions, in order to monitor the conditions of animals or plants in wild habitats as well as the parameters of the habitats.

WSNs can be used for health care purposes, for instance to monitor and track elders and patients, relieving the shortage of health care personnel and reducing the health care costs. A message from these networks can alert doctors when the patient requires immediate medical attention. Wearable sensors can be used to monitor vital signs, environmental parameters, and geographical locations, with instantaneous alerts in case of emergency. Finally, implantable wireless sensors make possible radio communications with a pacemaker or other electronic implants.

The industries may use WSNs to monitor manufacturing processes or the condition of manufacturing equipment. Wireless sensors can be instrumented to production and assembly lines to monitor and control production processes. Tiny sensors can be embedded in equipments inaccessible by humans to monitor the condition of the machine and alert for any failure.

Wireless networks may enable intelligent living environments. Indeed, water, gas, or electricity can be sensed and remotely read, and also the contents and schedules of TV, DVD, or CD players can be monitored and controlled remotely.

In addition to the above applications, self-configurable WSNs can be used in many other areas, for example in traffic control and in public infrastructures monitoring.

Fig. 1.1 shows a possible deployment of wireless sensors for precision

agriculture purposes. Sensors might detect temperature, light levels and soil moisture at hundreds of points across the field and communicate their data over the network for analysis.

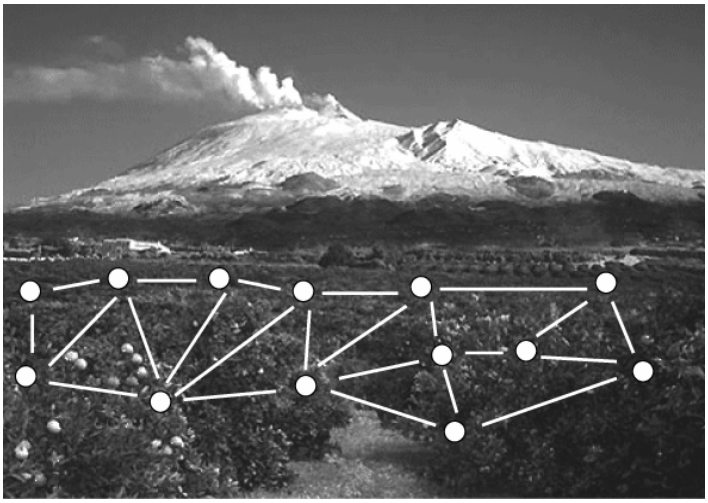

Fig. 1.1. *A WSN in a agriculture field.*

However, a number of technical issues must be solved before these exciting applications become a reality.

1.3 Implementation requirements

The characteristics of sensor networks and requirements of different applications have a decisive impact on the network design. The main requirements include:

- Small node size, in order to facilitate the sensor node deployment.
- Low node cost, in order to reduce the cost of the whole network. Indeed, sensor nodes are usually deployed in a harsh or hostile environment in large numbers and cannot be reused.
- Low-power consumption, in order to prolong the lifetime of the sensor nodes, as well as the whole network lifetime. Indeed,

sensor nodes are powered by battery and it is often very difficult or even impossible to change or recharge these batteries.

Each of these factors are somewhat intertwined. For example, electronic components are already so small that overall module size is limited by power supply or energy storage requirements. For this reason, reducing power consumption of the electronics is an effective way to shrink size as well. Another example is that highly integrated circuits with few external components can simultaneously reduce both size and cost.

1.4 Wireless node technology

The concept of WSNs was originally introduced three decades ago [2]. At that time, this concept was more a vision than a technology that could widely be exploited because of the state-of-the-art in sensor, computer, and wireless communication technologies. However, recent technological advances in MEMS, wireless communication, and low-cost manufacturing technologies have enabled the development of tiny, cheap, and smart sensors, which has therefore stimulated the development of sensor networks and their applications.

1.4.1 MEMS

Micro Electro-Mechanical Systems (MEMS) is a key technology for manufacturing tiny, low-cost, and low-power sensor nodes. It is based on micromachining techniques, which have been developed to fabricate micron-scale mechanical components that are controlled electrically. Through highly integrated processes, these electromechanical components can be fabricated with microelectronics. There are different micromachining techniques, for example, planar micromachining, bulk micromachining, and surface micromachining, which involve different fabrication processes.

Most micromachining processes begin with a substrate 100 μm thick, usually composed of silicon, other crystalline semiconductors, or quartz, on which a number of subsequent steps are performed, for example, thin-film deposition, photolithography, etching, oxidation, electroplating, machining, and wafer bonding. Of particular interest are the processes that combine CMOS transistors with micromachining capabilities. There are a number of techniques for performing post-process micromachining on foundry CMOS [3]. By using the MEMS technology, many components of sensor nodes can be miniaturized and integrated together, for example, sensors, communication blocks, and power supply units, which can also lead to a significant reduction in cost through batch fabrication, as well as in power consumption.

1.4.2 Hardware and software

The development of WSNs largely depends on the availability of low-cost and low-power hardware and software platforms for sensor networks.

Low-power circuit and system design [4] has enabled the development of ultra low-power hardware components, for example, microprocessors and microcontrollers. Meanwhile, power consumption can further be reduced through efficiently operating system resources using some dynamic power management (DPM) technique. For example, a commonly used DPM technique is to shutdown idle components or put them in a low-power state when there is little or no load to process.

Low-power circuit and system design together with power management techniques, have enabled the development of many low-power sensor platforms. The commercial availability of these platforms has significantly stimulated the further development of WSNs.

1.4.3 Wireless communication

All wireless sensors require an on-board transceiver to support

communications. A transceiver is typically defined as a combined transmitter and receiver, sharing common circuitry or a single housing. Today most conventional wireless networks use radio frequency (RF) for communication. The primary reason is that RF communication does not require a line of sight and provides omni-directional links.

Most communication protocols for RF wireless networks, for example cellular systems, wireless local area networks (WLANs), and wireless personal area networks (WPANs), do not consider the unique characteristics of sensor networks, in particular, the energy constraint in sensor nodes. Therefore, they cannot be applied directly without modification. A different suite of network protocols is required to address these new networking issues, taking into account the unique characteristics of WSNs.

Among all the node functions, the wireless communication power consumption is the dominant component. Indeed, in many applications the power consumption of the radio front end circuitry is equal to 70-80% of the whole power budget [5] [6]. A heavy power consumption reduction is essential to enable the use of new power supply technologies like energy harvesting [7] and low cost printable batteries [8]. These early-stage technologies cannot supply much power, so any means of reducing power requirements will hasten the adoption of next-generation power supplies.

1.5 Standardization of WSNs

Hardware constraints and the trade-off between antenna efficiency and power consumption limit the choice of a carrier frequency for such transceivers to the ultra high frequency (UHF) range [9].

In case of wireless implantable devices for advanced healthcare treatments, the radio transceivers have been regulated to operate in the 402-405 MHz band conforming to the Medical Implant Communications

Service (MICS) specifications [10] defined by the U.S. Federal Communications Commission (FCC). Two additional bands has been proposed by the European Telecommunications Standards Institute (ETSI) [11] [12] at 401-402 MHz and 405-406 MHz for further medical services. Since the radio allows communication with electronic implants, such as a pacemaker, the maximum transmit power is very low, EIRP=25 μW, in order to reduce the risk of interfering with other users of the same band.

Conversely, transceivers for general purpose WSNs commonly make use of license-free Industrial Scientific Medical (ISM) frequency bands (315-433-868-915 MHz), whose allocations is not the same in all countries [13]-[15]. The main advantages of using the ISM bands are the free radio, huge spectrum allocation, and global availability. Communication in ISM bands is not bound to a particular standard, thereby giving more freedom for the implementation of energy-efficient networking protocols for WSNs. On the other hand, since the ISM bands are not regulated or assigned to a particular type of user, there are various rules and constraints, such as power limitations and harmful interference from existing applications.

A lot of efforts have been made and are under way in many standardization organizations in order to unify the WSN market, leading to low-cost and interoperable devices. To this end, the IEEE 802.15.4 [16] standards body was formed for the specification of low data-rate wireless transceiver technology with long battery life and very low complexity. Nevertheless, nowadays the standardization process is still in an initial stage.

1.6 Energy efficiency in WSNs

Power consumption is the most important challenges to be faced when designing sensor nodes for wireless sensor networks. One approach for energy efficiency is to limit the transmission power by reducing the distance between

the nodes, thus adopting a multi-hop networking. Another approach is to reduce the amount of energy consumed by idle listening by means of periodical turn-on and turn-off of transceiver radios.

1.6.1 Multi-hop networking

A sensor network typically consists of a large number of sensor nodes densely deployed in a region of interest, and one or more base station nodes located close to or inside the sensing region. Taking into consideration for instance the wireless communication from a node to its base station, given a transmission power P_{TX}, the received signal power P_{RX} can be calculated by using the well known Friis formula

$$P_{RX} = L_F \left(\frac{\lambda}{4\pi} \right)^2 \frac{G_{TX} G_{RX}}{d^n} P_{TX} \tag{1.1}$$

where L_{F} is a loss factor which takes into account the TX and RX antennas coupling losses, G_{TX} and G_{RX} are the TX and RX antenna gains, d is the distance between the transceivers, while n ranges from 3 to 5 considering indoor or outdoor conditions. The Friis formula states that the received power P_{RX} is in inverse relation at least to the cube of the distance d. As a consequence, increasing the distance between the sensor node and the base station the required transmission power P_{TX} rapidly increases.

As a consequence, only if the WSN region of interest is physically enough limited (d ~ 10 m) can be done a low-power data transmission by adopting a single-hop communication, as shown on the left in Fig. 1.2. In this case each sensor node communicates directly with the base station. However, sensor networks often cover large environments and multi-hop communication, shown on the right in Fig. 1.2, is the commonly adopted technique. In this case, sensor nodes must not only capture and disseminate their own data, but also serve as relays for other sensor nodes, that is, they

must collaborate to propagate sensor data towards the base station.

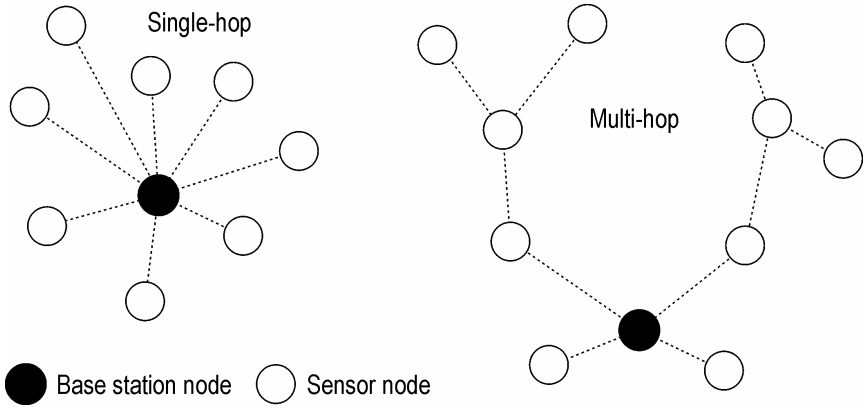

Fig. 1.2. *Single-hop versus multi-hop communication.*

The task of finding a multi-hop path from a sensor node to the base station, is one of the most important challenges in the WSN networking.

1.6.2 Low duty cycle operation

As highlighted, the radio transceiver is the dominant source of power consumption in a sensor node. The power consumption of the radios available today (tens of *m*W) does not allow several years of autonomy. To give a better idea of the power consumption constraint, let us consider a node powered by only a single coin battery with a capacity of 100 *m*Ah and a radio consumption of 10 *m*A. The node lifetime is lower than one day, and thus is clearly impossible to keep this transceiver active all time.

In order to understand how cut down the power consumption, it is important to underline the unique network characteristics of WSNs. In most application scenarios, each node deal with only a few packets/second. In addition, the packets are relatively short (typically less than 200 bits/packet). As a result, the average data-rate rarely exceeds 1 kbit/s. The amount of data to be transferred depends on the specific application, but most sensing and monitoring applications fit this general form with sparse communications and

long periods of idle time.

The natural way to take advantage of the low activity rate is the heavy duty-cycling of sensor nodes [17]. Duty-cycling is a very powerful means to reduce energy usage and increase battery life. By turning on the electronics of the node for short periods of time and then entering a low-power sleep mode, average consumption can easily be reduced by orders of magnitude. The periodic listen and sleep scheme is depicted in Fig. 1.3.

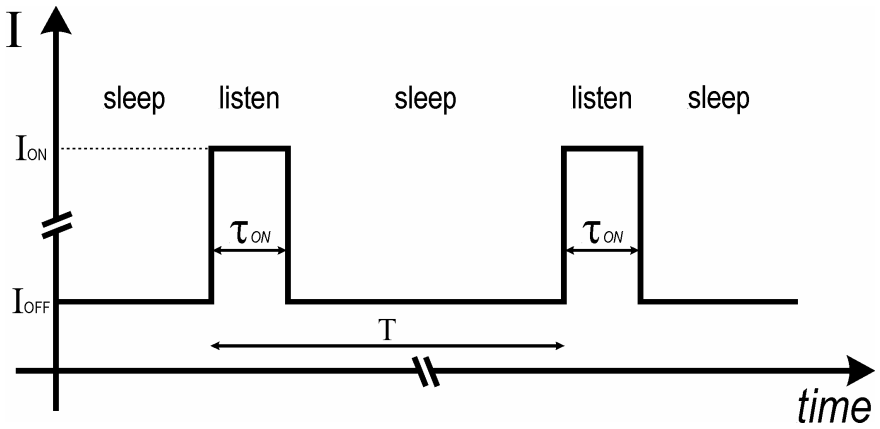

Fig. 1.3. *Period listen and sleep modes of operations.*

In Fig. 1.3 I_{ON} is the transceiver current consumption, whereas I_{OFF} is the current wasted when the transceiver is turned off (typically lower than 1 μA).

Based on this scheme, each node sets a wake-up timer and goes to sleep for the specified period of time. At the expiration of the timer, the node wakes up and listens to determine if it needs to communicate with other nodes. The main challenge is put together low duty cycle along with multi-hop networking. Indeed, during the sleep periods the sensor node cannot receive messages from its neighbours nor can it serves as a relay for others. Some networks rely on wake-up on demand strategies [18] to ensure that nodes can be woken up whenever needed. Usually this involves devices with two radios, an ultra low-power radio used to receive wake-up calls and a radio activated in

response to a wake-up call. Another strategy is adaptive duty cycling, wherein not all nodes are allowed to sleep at the same time since a subset of the nodes in a network remain active to form a network backbone.

The parameter that governs the percentage of the wake-up period to the sleep period is called duty cycle, and is given by

$$D = \frac{\tau_{ON}}{T} \tag{1.2}$$

while the average current consumption of the duty-cycled transceiver by

$$I_{avg} = I_{ON} \cdot D + I_{OFF} \cdot (1 - D) \tag{1.3}$$

It is worth noticing that considering for instance D = 0.0001 (which is a duty cycle of 0.01%) the current consumption is reduced of four orders of magnitude, if I_{OFF} do not limit such average reduction, prolonging the node lifetime from days to years. The minimum tolerable value of duty cycle strictly depends on the amount of data to be transferred. However, only extremely low I_{ON} allow to rewrite the equation (1.3) as

$$I_{avg} \approx I_{OFF} \tag{1.4}$$

and the average current I_{avg} is almost equal to I_{OFF}.

As a consequence, the reduction of the energy dedicated to RF transceiver is a key target for implementing ultra low-power WSNs.

Chapter 2

A low-IF radio transceiver for Wireless Sensor Networks

This chapter discusses key-points for implementing an ultra low-power wideband CMOS radio transceiver for WSNs. The main target is to implement a transceiver able to cover all the sub-GHz frequency bands nowadays used for WSN (300-403-434-868-915 MHz) and to support different operating range, thus providing a worldwide solution.

The radio transceiver, which has been implemented in a 90-*n*m CMOS technology, operates in the 300-470/780-960 MHz frequency ranges. It supports a GFSK modulation scheme with a maximum data bit-rate of 100 kb/s. The target RX sensitivity is –92 dBm while the nominal TX output power is 0 dBm. The circuit is designed to provide a target operating range of 20 m with a power consumption of 4.2 *m*A and 5 *m*A from a 1.2-V supply for the RX and TX, respectively.

2.1 Transceiver objectives and specifications

2.1.1 Objectives of the transceiver

The transceiver has the aim to represent a low-cost small-size solution and therefore the use of any expensive external components, such as SAW filter, should be avoided. The minimum distance between two sensor nodes is considered equal to 1 m. On the other hand, the maximum operating range

should be higher than 20 m with a maximum bit-rate of 100 kbit/s and FSK/GFSK modulation schemes. A raw bit error rate (BER) of 10^{-3} has been estimated acceptable for the RX [19]. In order to avoid excessive power consumption during transmission time slots, the nominal maximum output power level of the TX is 0 dBm. However, the TX should be also able to deliver an higher output power level of 10 dBm, if required by any specific applications. The peak power consumption of the transceiver should be compatible with a lifetime of the sensor node higher than 5 years. Obviously, the transceiver must be properly duty-cycled to achieve a such performance. The target specifications of the transceiver are summarized in Table I.

TABLE I
TRANSCEIVER OBJECTIVES

Parameter	Value
Operating bands	300-470/780-960 MHz
Operating range	> 20 m
Maximum bit rate	100 kbit/s
Modulation schemes	FSK/GFSK
RX BER	1e−03
TX maximum output power	0-dBm (typically) 10-dBm (if required)
External components	No SAW filter, minimum passive components
Lifetime	> 5 years

2.1.2 Target specifications of the transceiver

In order to ensure a BER of 10^{-3} with 100 kbit/s GFSK signal, the required signal-to-noise ratio (*SNR*) at the demodulator input should be around 10 dB. On the other hand, the receiver input signal power (P_{RX}) can be calculated by using the Friis formula (equation 1.1). Supposing that the antennas are isotropic (G_{TX} and G_{RX} equal to 0 dB) and the loss factor is 0.5,

the receiver input signal at 20 m distance is around −88 dBm. Considering these data, the overall receiver noise figure (*NF*) can be obtained from the following formula

$$NF \leq -\left(-174 + 10\log\left(B\right)\right) - S - SNR \tag{2.1}$$

where B is the input signal bandwidth, which can be considered roughly equal to 200 kHz for a 100kbit/s GFSK modulated signal. S is the sensitivity level, which has been set to −92 dBm to ensure robust operation. The resulting *NF* from equation (2.1) is lower than 19 dB. Considering a such noise figure, with a 10 dBm TX output power, an operating range of 37 m can be achieved. Moreover, supposing that the transceiver exhibits the same *NF* performance at 300 MHz, the maximum operating range vary from 35 m to 65 m with a TX output power ranging from 0 to 10 dBm.

The maximum input power level at the RX input results −25 dBm, supposing a maximum TX output power of 0 dBm and a receiver device at 1m distance. Therefore, the variable-gain dynamic range of the receiver results typically around 70 dB.

In order to guarantee a robust operation in presence of in-band interferers, the receiver chain should ensure the BER specification with the presence of two in-band interferers. When the wanted signal is at sensitivity level (−92 dBm), the power level of the two in-band interferers is supposed to be as high as −56 dBm. This means that when a receiving node is listening from a node placed at the maximum distance, any nodes of the sensor network within 10 m cannot transmit in adjacent channels.

A target Intermodulation Rejection (IMR) greater than 36 dB has also been defined as a good value to guarantee a strong robustness of the receiving chain against in-band interferers. Fig. 2.1 shows the operative condition that must be satisfied.

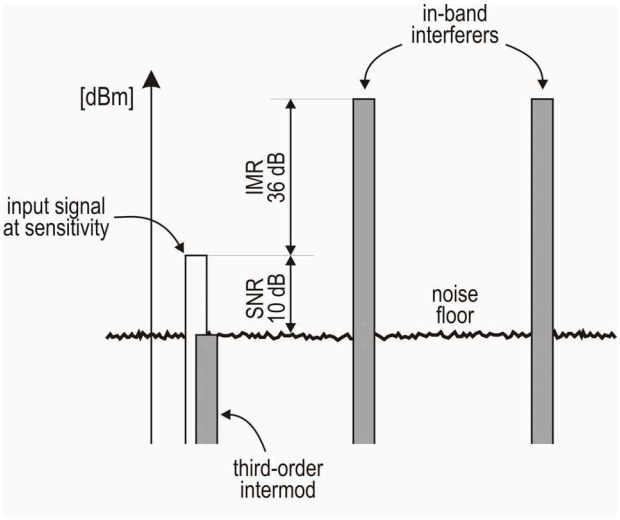

Fig. 2.1. *Intermodulation rejection test.*

In other words, the condition is equivalent to guarantee an IM_3 ratio greater than 46 dB when two tones of –56 dBm (sensitivity + IMR = –92 dBm + 36 dB) are received. This IM_3 specification results in an input IP3 of –33 dBm. Considering the above mentioned scenario, the adjacent channel rejection (*ACR*) spec is around 46 dB with a *SNR* of 10 dB.

The *ACR* dictates an upper limit for the Phase-locked loop (PLL) phase noise and spurs rejection. The phase noise at an offset frequency equal to the channel spacing must be satisfied the following condition

$$L\left(\Delta f_{ch}\right) \leq \frac{1}{B \cdot ACR} \tag{2.2}$$

where Δf_{CH} is the channel spacing. In our case, the channel spacing is 300 kHz since a guard band of 100 kHz between two adjacent channel has been considered. Equation (2.2) suggest a phase noise at 300 kHz offset lower than –99 dBc/Hz. As far as the PLL spurs is concerned, the upper limit is –46 dBc. However, to avoid a BER degradation due to the simultaneous effects of the phase noise and spurs a more stringent specification for spurs rejection can be adopted.

The sensor node is supposed to be supplied by a coin battery with a typical storage capacity of 100 mAh. The sensor node average current consumption should be lower than 2 μA in order to ensure a life time longer than 5 years. Considering that the transceiver consumes a average current of 1 μA during sleeping mode and the peak current consumption for the radio transceiver is around 5 *m*A, the duty cycle of the sensor node should be on the order of 0.01%. Such a current consumption could be compatible with a TX output power of 0 dBm. For a 10 dBm TX output power, the current consumption is surely higher. Therefore, if a such output power is required, a lower duty cycle or a shorter life time must be tolerated by the applications.

Since the battery energy is a precious resource, the time required to establish a communication channel between two sensor node must be carefully evaluated to avoid an excessive energy waste. This time was assumed equal to the PLL start-up time supposing that the PLL has the slowest transient response of the transceiver. Fig. 2.2 shows the battery energy wasted as a function of this time. The curves are calculated considering a 100 kbit/s data-rate, 0.01% duty cycle, and are given for different value of packet length.

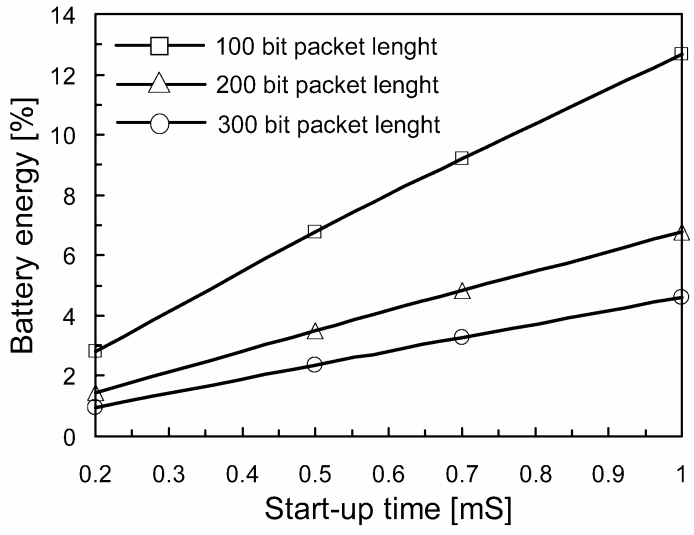

Fig. 2.2. *Battery energy wasted during start-up.*

The RX and TX radio front-end circuits are considered turned off and the PLL current, assumed equal to 1.5 mA, is supposed to be the main contribution of the overall current drawn from battery during start-up. As highlighted in Fig. 2.2, for a packet length longer than 200 bit, a value of 0.5 *m*S results in a negligible waste of energy.

As far as the technology choice is concerned, a 90-nm CMOS process has been selected. The proposed radio will be included in system-on-chip device. Therefore, a 90-*n*m CMOS process has been considered to trade off minimization of the digital part area and the RF/analog circuit performance. Table II summarizes the target specifications of the radio transceiver.

TABLE II
TRANSCEIVER SPECIFICATIONS

Parameter	Value
NF	< 19 dB
Maximum input power (0-dBm TX output power)	–25 dBm
Variable-gain range	70 dB
IIP3	–33 dBm
Adjacent channel rejection	46 dB
PLL phase noise (300-kHz offset freq.)	–99 dBc/Hz
PLL spur rejection	46 dB
PLL start-up time	≈500 μS
RX current consumption	< 3.5 mA
TX current consumption	< 3.5 mA
PLL current consumption	< 1.5 mA
Technology	90-nm CMOS
Supply voltage	1.2 V

2.2 Transceiver architecture

The small size constraint dictates for an highly-integrated transceiver architectures. Therefore, the most suitable solutions are the zero-IF [19] [20] and the low-IF architectures [21] [22]. The major drawback of the zero-IF architecture is related to the high sensitivity to DC offset and flicker noise. While the low-IF transceiver guarantees the integration level of homodyne architecture, it achieves a better frequency isolation due to small but non-zero separation between LO and RF frequencies. However, high accuracy between I/Q paths must be ensure to provide image rejection ratio (IRR) higher than 40 dB [21] [23]. Fig. 2.3 shows the block diagram of the proposed transceiver.

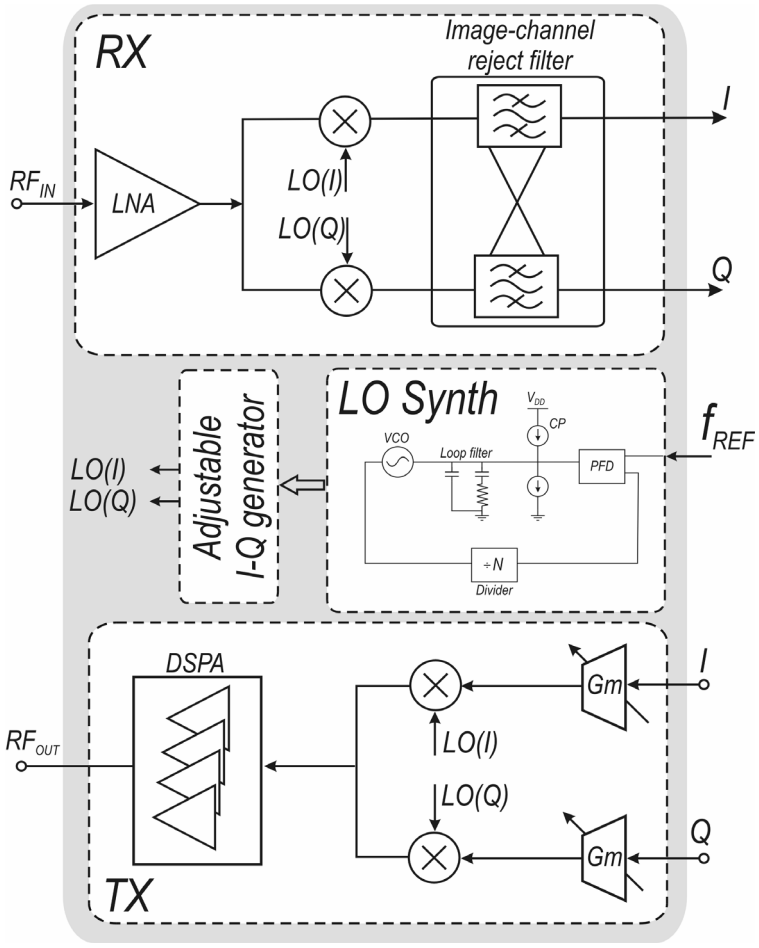

Fig. 2.3. *Block diagram of the radio transceiver.*

2.2.1 Receiver

A low-IF architecture has been adopted for the RX chain. The RF down-conversion part, consists of a single-ended two-stage low-noise amplifier and *IQ* mixer. The analog baseband *IQ* section provides image and channel rejection filtering. An IF frequency of 300 kHz was chosen to trade off performance and power consumption. Indeed, a higher IF frequency helps to reduce the impact of flicker noise, the start-up time of the analog baseband circuits, and the image-channel filtering selectivity. However, it results in a higher power consumption for the analog-to-digital converter (ADC) and digital baseband circuits.

In order to guarantee a proper IRR, amplitude and phase mismatch correction must be included. For this purpose a variable-gain I/Q amplifiers, featuring fine gain-control step, can be adopted. The correction of the I/Q phase errors is performed by the adjustable I/Q signals generator, which is a part of the LO frequency synthesizer. To ensure a IRR equal to the ACR, which is 46 dB, the I/Q phase and the amplitude should be lower than 0.8 degree and 0.1 dB, respectively.

In this design, the adoption of an analog channel-image rejection approach plays a key role to reduce the complexity and the power consumption of the ADC and digital baseband circuits.

The required signal-to-(noise+distortion) ratio (SNDR) is given by the following formula

$$SNDR \leq 6 + ACR + SNR_M \tag{2.3}$$

where ACR is the adjacent channel rejection, SNR_{M} represents the estimated margin to make negligible the error introduced by the analog-to-digital conversion and is assumed to be 10 dB, whereas 6 dB has been added to the SNDR to consider a scenario with two tones 36 dB higher than the wanted

signal. The resulting SNDR is 62 dB without any filtering. If we consider a RF band of around 5 MHz, the frequency separation between the wanted signal and the spurious tone could be 5 MHz and the ADC sampling frequency six times higher (i.e. 30 MHz).

The energy per Nyquist sample of a state-of-the-art DAC with a 62-dB SNDR is around 5e−11 Joules [24], which corresponds to a power consumption of around 1.5 *m*W with a 30-MHz sampling rate. Moreover, the digital baseband must provide channel-image filtering and works with a 30-MHz clock frequency. On the other hand, by providing a 36 dB channel filtering, the SNDR is reduced to 26 dB and the sampling frequency can be reduced to 3 MHz (ten times of 300 kHz). The resulting DAC power consumption becomes negligible being around 1 μW [24]. Moreover, the circuit complexity of the digital part is greatly reduced and a lower clock frequency can be adopted (3 MHz instead of 30 MHz).

2.2.2 Transmitter

As far as the TX section is concerned, a direct conversion architecture was adopted. The circuit comprises a quadrature up-converter, a power amplifier, and an external (off-chip) matching network. The matching network is the only frequency-selective block of the proposed architecture, while the other building blocks are designed for wideband operation in the 300–960 MHz frequency range.

The concept of dynamic biasing is extensively employed in order to improve the system efficiency through the whole TX power range (–20/10 dBm), not only at the nominal power level [25]. To this purpose, a digitally sized power amplifier (DSPA) architecture has been adopted for the final stages of the TX chain. This solution entails the use of multiple amplifying cells in parallel connection. The cells can be switched on and off, according to the required output power level. At back-off power levels, turning off a

portion of the DSPA results in reduced current consumption and hence improved efficiency. To the same purpose, a convenient gain control methodology has been adopted for the variable-gain up-converter, which is able to reduce the signal power at the DSPA input while simultaneously lowering the up-converter bias current.

Assuming an efficiency of 30% for the TX for a 0-dBm output power level, the current consumption of the TX is around 3 *m*A from a 1.2-V supply.

2.2.3 The proposed frequency synthesizer

The frequency synthesizer is one of the most critical building blocks of the RF front-end for WSNs. Indeed, the constraint of a very low-power consumption imposes severe limits to phase noise and tuning range performance and makes challenging the generation of highly-accurate I/Q signals.

Fig. 2.4 shows the simplified block diagram of the proposed frequency synthesizer, which is implemented by means of a programmable integer-*N* Phase-Locked Loop [26] [27].

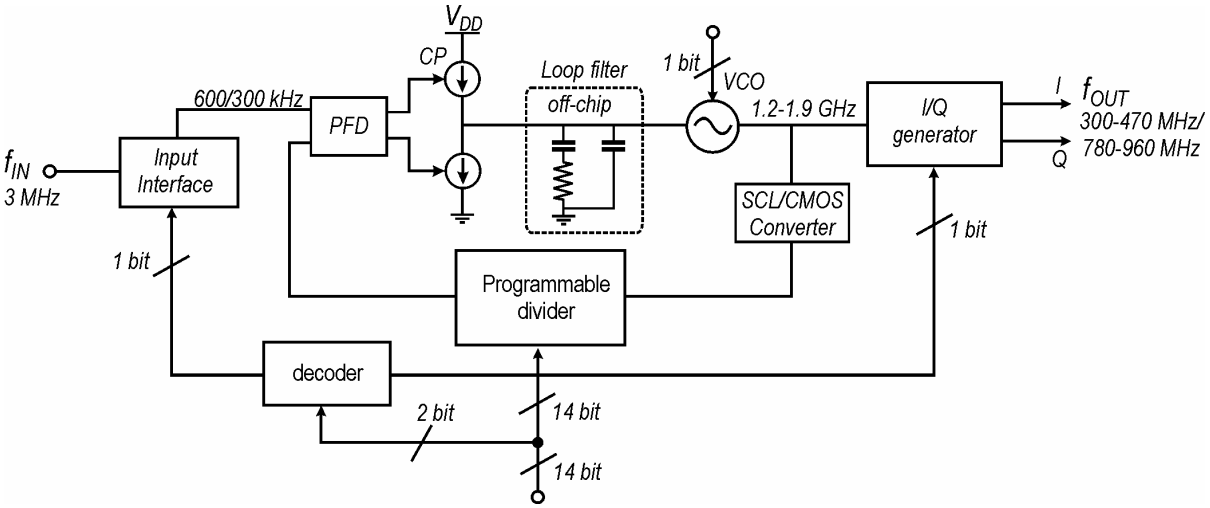

Fig. 2.4. *Frequency synthesizer block diagram.*

The VCO provides two sub-bands, which are selected by a control bit. The lower band is 1.2-1.5 GHz, whereas the higher one is 1.5-1.9 GHz.

The operating LO bands are obtained by properly dividing the VCO output by means of the I/Q generator, which was inserted out of the PLL loop as shown in Fig. 2.4. The 300-470 MHz band is obtained dividing by 4 both VCO lower and higher band, whereas the 780-960 MHz band is obtained dividing by 2 the VCO higher band.

The channel selection is performed by setting of a 14-bit digital word, which control the programmable integer divider.

The input interface circuit generates a programmable 300/600-kHz PLL reference employing a fixed 3-MHz input signal. A control bit, decoded from the divider control word, sets the PLL reference to 600-kHz in case of 300-470 MHz band and to 300-kHz in case of 780-960 MHz band. In this way fixed 150-kHz frequency steps are synthesized.

Because of the low-frequency input reference, the loop filter was implemented using off-chip components. It was sized to obtain a 7-kHz loop bandwidth.

It is worth noticing that the 600-780 MHz band can be easily obtained dividing by 2 the VCO lower band. Moreover, the frequency synthesizer offers 150-kHz frequency steps, even though the transceiver channel spacing is 300 kHz. For these reasons, the implemented frequency synthesizer can be employed for further sub-GHz applications, which were not included in the proposed radio transceiver.

2.3 Frequency synthesizer building blocks

2.3.1 Phase/frequency detector and charge pump

The phase/frequency detector was implemented by means of the well-known three-state machine with a delay circuit in the reset path to

eliminate the dead zone.

Fig. 2.5 shows the schematic of the charge pump. The circuit adopts a source-switching topology [28], which guarantees high speed while avoiding high current spikes at the output. To minimize the current variation over the output voltage swing, a low-voltage cascode structure was employed for the current mirrors. The triode-biased transistors M_3, M_6, and M_{12} were used for replica biasing to guarantee the same bias condition when the charge pump is turned on.

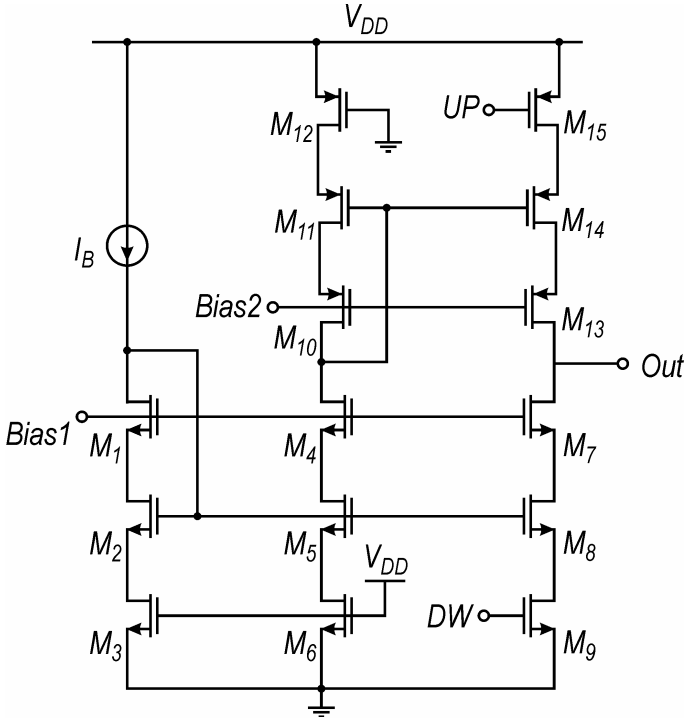

Fig. 2.5. *Schematic of the charge pump.*

2.3.2 Voltage controlled oscillator

The schematic of the adopted voltage controlled oscillator is shown in Fig. 2.6 [29]. It is based on a complementary cross-coupled topology, which increases the transconductance gain and hence minimizes the current consumption for reliable start-up condition. The *LC* tank makes use of shunt-connected switched-coupled inductors (L_1, L_2), which provide coarse tuning.

The inductors are AC-coupled by means of MIM capacitors C_D. L_2 switching is performed by using the NMOS transistor M_{sw}. The proposed varactors configuration employs accumulation mode thin (C_{12}) and thick (C_{33}) MOS devices, which are differently biased to obtain tuning range maximization along with minimization of the amplitude-to-phase noise conversion.

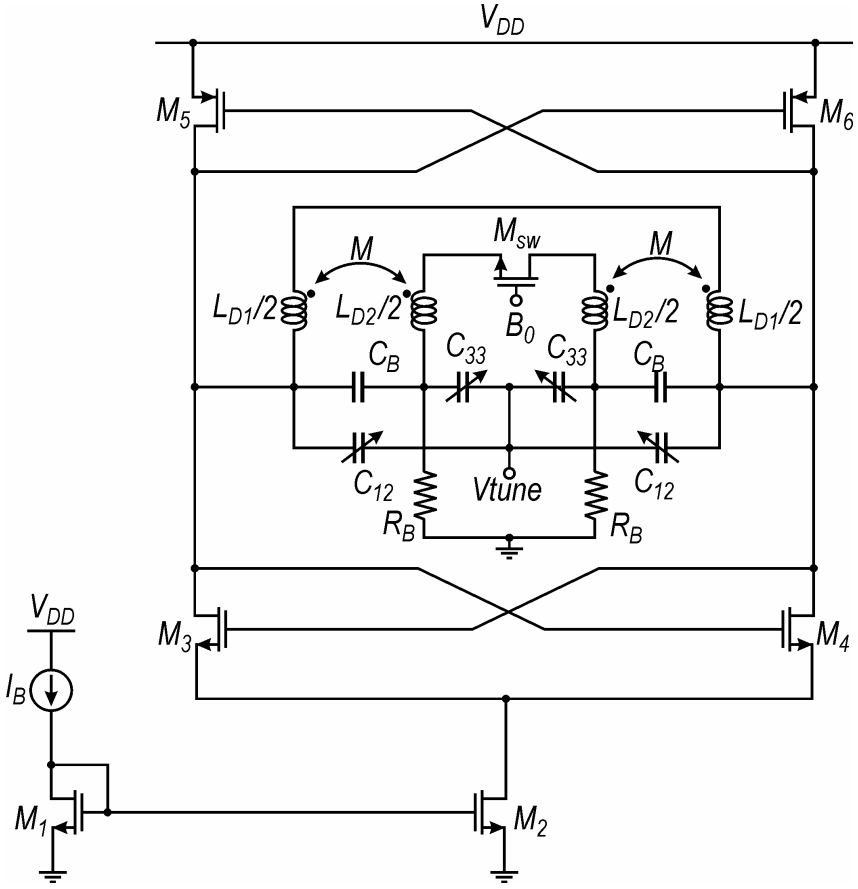

Fig. 2.6. *Schematic of the VCO.*

The in-depth design of the *LC* VCO is presented in chapter 3.

2.3.3 SCL/CMOS converter and programmable divider

The SCL/CMOS logic level converter was implemented by means of a single-stage stacked-mirror operational transconductance amplifier, which guarantees rail-to-rail swing operation. A CMOS buffer was inserted at the

SCL/CMOS converter output to properly drive the programmable divider.

The programmable divider must be carefully designed to support different frequency bands while avoiding increased circuit complexity. The simplified block diagram is shown in Fig. 2.7.

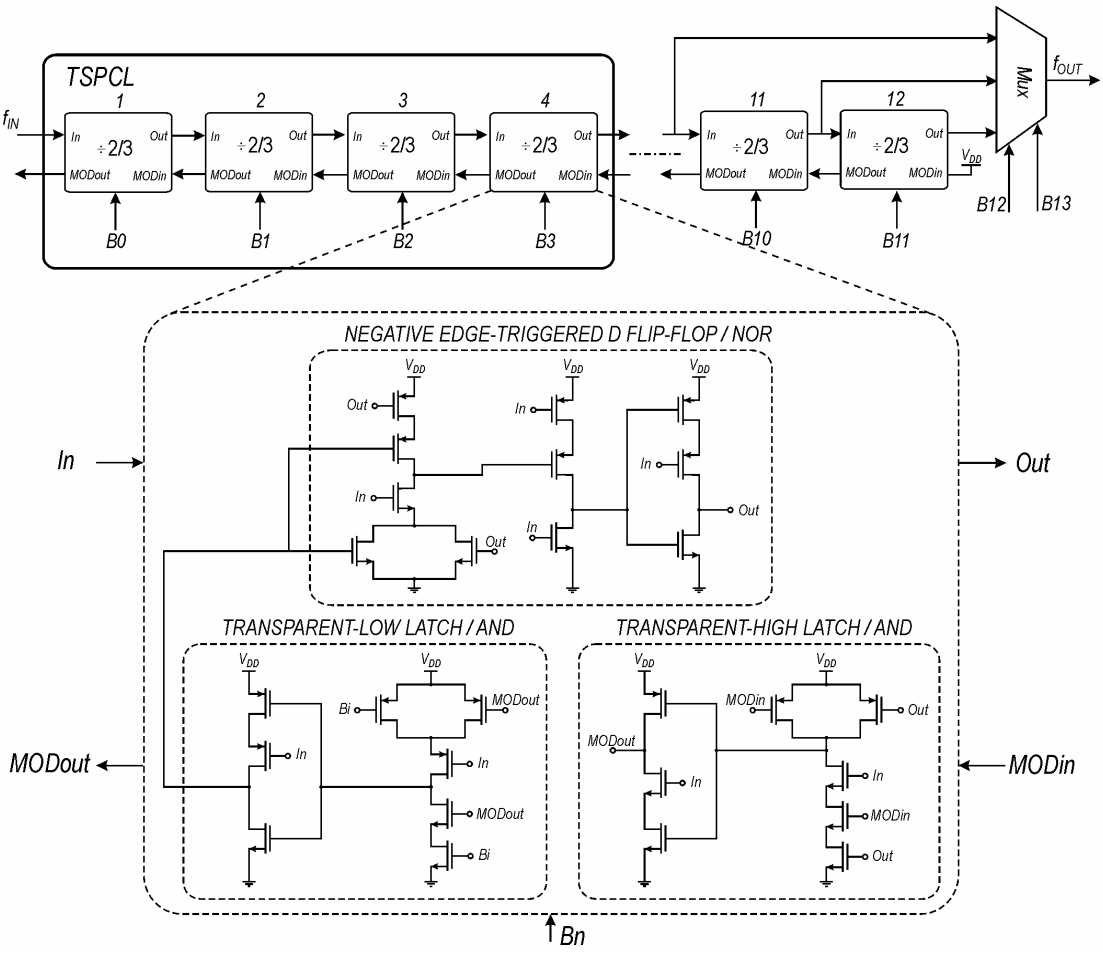

Fig. 2.7. *Block diagram of the programmable divider and schematic of the high frequency 2/3-dividers.*

The circuit is based on a truly modular architecture and includes a chain of twelve 2/3-dividers. In order to reduce the power consumption, the high-frequency 2/3-dividers, whose schematic is detailed in Fig. 2.7, are implemented using TSPCL cells. The low-frequency 2/3 dividers make use of CMOS static logic cells.

The last two 2/3-dividers can be bypassed by means of a multiplexer. When the last two 2/3 dividers are included in the chain, the divider is programmed to provide a division ratio ranging from 5000 to 6330, the PLL input reference is set to 300-kHz and the VCO output signal is divided by 2 (780-960 MHz band). On the other hand, when one or both the last 2/3-divider cells are bypassed, the divider is programmed to provide a division ratio ranging from 2000 to 3130, the PLL input reference is set to 600-kHz and the VCO output signal is divided by 4 (300-470 MHz band).

2.3.4 I/Q generator

The I/Q generator has the target of producing quadrature signals with phase error lower than 1 degree in the whole operating bands with respect to process, temperature and power supply variations, to be compliant with a IRR higher than 40 dB.

This phase accuracy has been achieved by means of an auto-calibrated I/Q generator, whose block diagram is shown in Fig. 2.8.

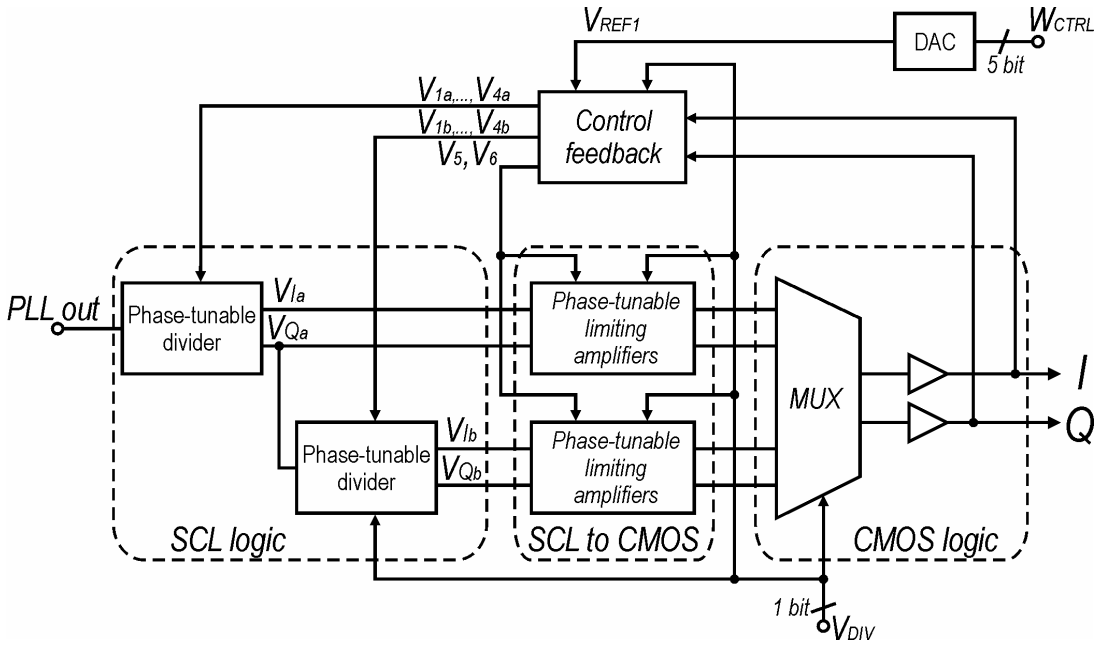

Fig. 2.8. *Block diagram of the I/Q generator.*

The quadrature correction is performed by means of a control feedback circuit based on a DLL, which detects the quadrature phase error and properly drives the phase-tunable divider and the phase-tunable limiting amplifier. These phase-tunable circuits represent the core circuits of the I/Q generator since they provide an efficient way to control the phase of the I/Q signals.

The in-depth design considerations about the phase-tunable circuits as well as the detailed description of the I/Q generator block diagram are presented in chapter 4.

Chapter 3

Design of a 1-mW wideband VCO

The implementation of fully-integrated low-power wideband voltage controlled oscillators (VCOs) for WSN applications is very challenging, since the constraint of low-power consumption imposes severe limits to the achievable phase noise and tuning range performance [5] [30]-[32].

LC VCOs with off-chip tank inductors have been usually adopted in sub-GHz transceivers to provide low-power consumption along with excellent phase noise performance [5]. On the other hand, several techniques have been demonstrated for the implementation of fully-integrated wideband VCOs with tuning range higher than 50% and excellent phase noise performance [33]-[42]. However, the reported power consumptions are not compatible with the requirements dictated by the WSN applications.

This chapter describes a low-power wideband 1.2-1.9 GHz VCO, which exploits an integrated *LC* tank based on shunt-connected switched-coupled inductors and a proper varactors configuration. Thanks to the adopted techniques, the VCO exhibits low-power consumption while providing excellent phase noise performance. It provides two sub-bands. The lower band is 1.2-1.5 GHz, whereas the higher one is 1.5-1.9 GHz. In Section 3.1, the coarse tuning techniques are described and compared. Section 3.2 and 3.3 detail the adopted coarse tuning technique and varactor configuration, respectively. Finally, the VCO design is highlighted in Section 3.4.

3.1 Coarse tuning techniques

Two main classes of coarse tuning techniques can be individuated, which are the capacitive and the inductive techniques. The capacitive coarse tuning technique is based on the variation of the capacitive part of the *LC* tank [33]-[35] whereas the inductive coarse tuning approach varies the inductive part [36]-[42]. In this section, these two different coarse tuning techniques are compared in terms of power consumption, phase noise, and tuning range.

3.1.1 Power dissipation

The start-up condition represents a fundamental constraint for the design of VCOs. For the complementary cross-coupled VCO topology shown in Fig. 3.1, the start-up condition is given by

$$R_p \geq \left(\frac{2}{g_{mNMOS}} // \frac{2}{g_{mPMOS}} \right) \tag{3.1}$$

where g_{mNMOS} and g_{mPMOS} are the transconductance gain of the cross-coupled NMOS and PMOS transistor pairs, respectively, and R_{p} is the tank equivalent parallel loss resistance.

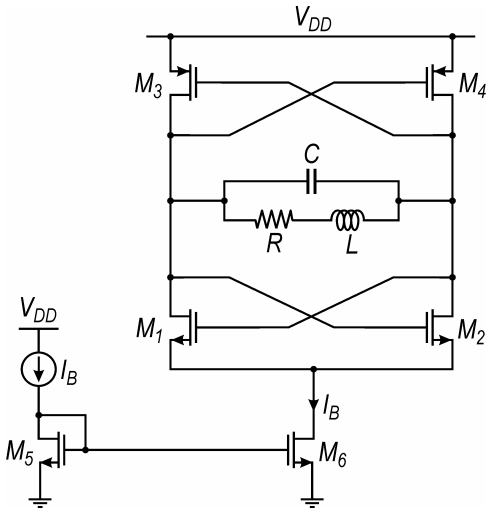

Fig. 3.1. *Cross-coupled complementary* LC *VCO.*

Supposing that the tank capacitor has a considerably higher quality factor than the inductor, R_p can be approximated as $(\omega_0 L)^2/R$, where ω_0 is the VCO oscillation frequency and R is the series loss resistance of the tank inductor. If $g_{mNMOS} = g_{mPMOS} = g_m$ equation (3.1) can be re-written as

$$g_m \cdot \left[\frac{(\omega_0 L)^2}{R} \right] = g_m \cdot (\omega_0 Q_L L) \geq 1 \tag{3.2}$$

where Q_L is the inductor quality factor. R_p, and hence the start-up condition, exhibits a frequency dependence that must be considered in a wideband design.

Wideband VCOs, which adopts capacitive coarse tuning technique, must be designed to provide start-up condition at the low end of the tuning range, where R_P reaches its lowest value. As a consequence, the VCO power consumption exhibits a bias current excess as the operating frequency increases. By exploiting trimming of the bias current or auto-calibration techniques [34], the g_m value can be varied to guarantee wideband start–up condition while providing power saving in the upper portion of the tuning range. However, the adoption of a fixed tank inductor in large tuning range VCOs does not allow to achieve a minimum power consumption design. Indeed, low-power consumption means high inductance to have high $\omega_0 QL$ product, but that is in contrast with large tuning range performance.

Inductive coarse tuning technique has the potential to provide significant saving in power consumption. Indeed, the equalization of the start-up condition can be accomplished with a fixed bias current by selecting a higher-R_p (lower-R_p) tank inductor in the lower (upper) portion of the supported tuning range. This can be easily achieved by varying the inductance L. Inductive coarse tuning techniques have been implemented using several approaches, such as, series-connected or shunt-connected switched-inductors

[35] [36], transformer-based tanks [37] [38], and magnetically-coupled switched-inductors [39]-[42]. However, the switch parasitic resistance and magnetic losses in any inductive coarse tuning techniques have to carefully considered since can affect the overall tank quality factor and hence the minimum bias current for reliable start-up condition.

3.1.2 Phase noise

The oscillation amplitude plays a key role in the optimization of VCO phase noise performance. Indeed, several works [26] [43]-[45] demonstrate that exists an optimum value of oscillator amplitude, which minimizes the phase noise.

Fig. 3.2 reports the phase noise of the VCO shown in Fig. 3.1 simulated with SpectreRF.

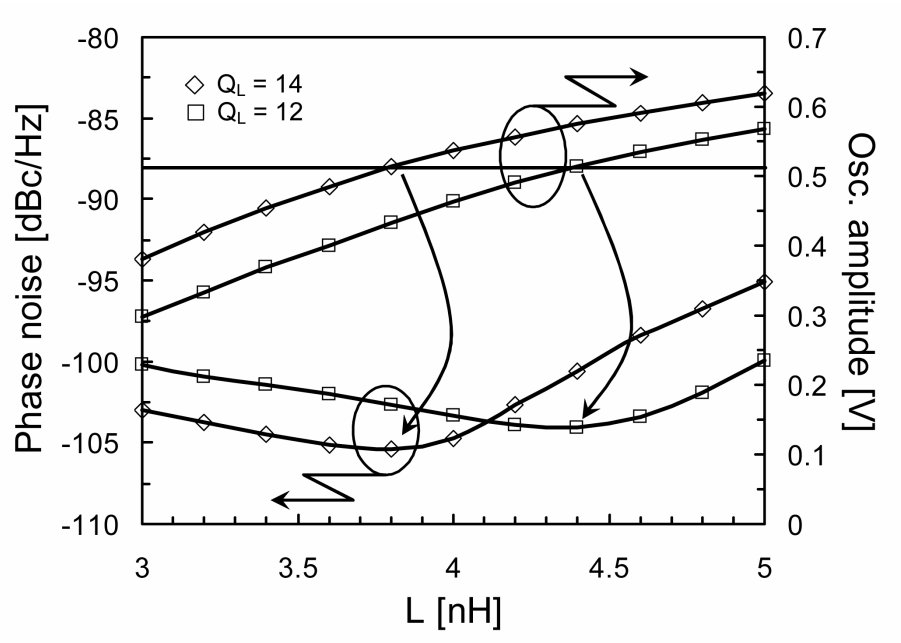

Fig. 3.2. *Phase noise and oscillation amplitude vs. inductance for different quality factor values (f_0 = 1.5 GHz, offset frequency = 100 kHz, I_{bias} = 600 μA).*

Phase noise at 100-kHz offset and oscillation amplitude are given as a function of the tank inductance for two different values of Q_L and a fixed carrier frequency (1.5-GHz). As highlighted in Fig. 3.2, the phase noise can be minimized by choosing a proper tank inductance, which guarantees the optimum value of oscillator amplitude. More specifically, for each inductor quality factor an optimum inductance value exists, which minimizes the phase noise. Therefore, the optimization of phase noise involves a proper choice of both inductance and quality factor to have the optimum oscillation amplitude. Obviously, if a proper inductance is selected, a higher quality factor of the tank inductor results in a better phase noise. It is worth noting that at different offset frequencies phase noise optimization is provided by the same tank inductor.

A variation of the bias current results in the translation of the phase noise curves with respect the inductance axes, as reported in Fig. 3.3.

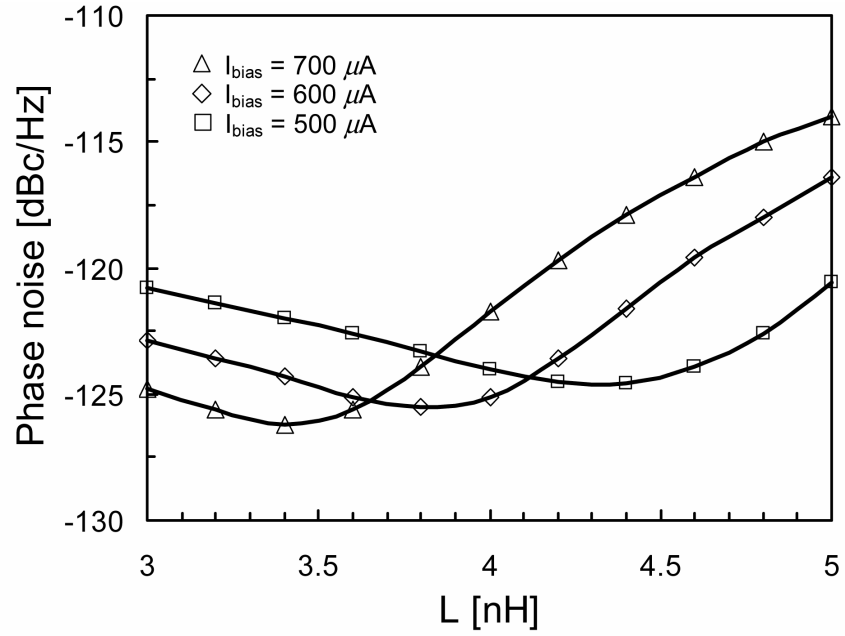

Fig. 3.3. *Phase noise vs. inductance for different bias currents (f_0 = 1.5 GHz, offset freq. = 1 MHz, Q_L = 14).*

Indeed, optimum oscillation amplitude can be obtained with a lower (higher) inductance by increasing (decreasing) the bias current. However, a higher bias current improves VCO phase noise performance.

In conclusion, the phase noise exhibits a critical dependency from the oscillation amplitude. Since the oscillation amplitude is given by

$$V_{osc} = \frac{4}{\pi} I_B \cdot R_p = \frac{4}{\pi} I_B \cdot (\omega_0 Q_L L) \tag{3.3}$$

[43], the variation of the oscillation amplitude with frequency due to R_P must be carefully taken into account for the optimization of phase noise performance in wideband design.

Consider now that coarse tuning is implemented by using a switched-capacitor array or an inductive technique, which splits the targeted tuning range in two sub-bands. For the switched-capacitor technique, the deviation from the optimum oscillation amplitude due to the frequency variation is larger, since the tank inductance is fixed (see equation 3.3). Instead, with the inductive coarse tuning technique, an optimum inductance value can be selected in each sub-band thus providing a lower variation of the oscillation amplitude within the overall tuning range. Therefore, for a fixed bias current and a given varactor gain, the inductive coarse tuning technique provides small phase noise variation although the capacitive coarse tuning approach exhibits a lower degradation of the tank quality factor. Of course, the amplitude variation in the capacitive coarse tuning can be compensated by varying the bias current, but this produces an increase in the power consumption. Finally, the major advantage of the capacitive coarse tuning technique is that the targeted tuning range can be easily split in several sub-bands allowing low-gain varactor to be used.

3.1.3 Tuning range

Fig. 3.4 shows the schematic of a *LC* tank, including two series-connected varactors, C_{VAR}, a switched-capacitor, C_{sw}, and a generic variable inductor, L, which can be implemented by using any of the above mentioned techniques (i.e., series-connected and shunt-connected switched-inductors, transformer-based tank, magnetically-coupled switched-inductors).

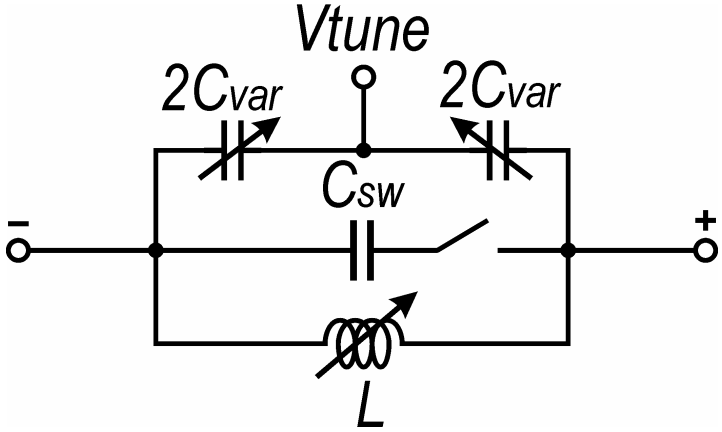

Fig. 3.4. *Schematic of a* LC *tank adopting capacitive and/or inductive coarse tuning techniques.*

Consider that coarse tuning is provided only through the switched capacitor and the targeted tuning range is split in two sub-bands. Neglecting the parasitic capacitances, the sub-band extremities can be expressed as

$$f_{h,h} = \frac{1}{2\pi\sqrt{LC_{VARh}}} \qquad f_{h,l} = \frac{1}{2\pi\sqrt{LC_{VARl}}} \tag{3.4a}$$

$$f_{l,h} = \frac{1}{2\pi\sqrt{L\left(C_{VARh} + C_{sw}\right)}} \qquad f_{l,l} = \frac{1}{2\pi\sqrt{L\left(C_{VARl} + C_{sw}\right)}} \tag{3.4b}$$

where C_{sw} is the capacitance of the switched capacitor and C_{VARh}, C_{VARl} are the equivalent capacitances of the series-connected varactors, which set the higher and lower sub-band extremities, respectively.

In the higher band, the fractional tuning range is given by

$$TR_h = 2 \cdot \frac{f_{h,h} - f_{h,1}}{f_{h,h} + f_{h,l}} = 2 \cdot \frac{\sqrt{\frac{C_{VARl}}{C_{VARh}}} - 1}{\sqrt{\frac{C_{VARl}}{C_{VARh}}} + 1} \tag{3.5}$$

while in the lower band is

$$TR_l = 2 \cdot \frac{f_{l,h} - f_{l,1}}{f_{l,h} + f_{l,l}} = 2 \cdot \frac{\sqrt{\frac{C_{VARl} + C_{sw}}{C_{VARh} + C_{sw}}} - 1}{\sqrt{\frac{C_{VARl} + C_{sw}}{C_{VARh} + C_{sw}}} + 1} \tag{3.6}$$

Assuming that C_{sw} is set to provide perfectly adjacent sub-bands, (i.e., $f_{h,l} = f_{l,h}$), from (3.4a) and (3.4b) it follows that C_{VARl} is equal to $C_{VARh}+C_{sw}$. Equation (3.6) can be re-written as

$$TR_l = 2 \cdot \frac{\sqrt{2 - \frac{C_{VARh}}{C_{VARl}}} - 1}{\sqrt{2 - \frac{C_{VARh}}{C_{VARl}}} + 1} \tag{3.7}$$

The ratio between C_{VARh} and C_{VARl} sets univocally the tuning range in the higher band, as can be deduced in (3.5). As a consequence TR_l is finally given by

$$TR_l = 2 \cdot \frac{\sqrt{2 - \left(\frac{2 - TR_h}{2 + TR_h}\right)^2} - 1}{\sqrt{2 - \left(\frac{2 - TR_h}{2 + TR_h}\right)^2} + 1} \tag{3.8}$$

Equation (3.8) accounts for the reduction of the fractional tuning range in the lower band due to the insertion of the switched capacitor.

Consider now that coarse tuning is achieved by means of the variable inductor. Also in this case, the targeted operating band is split in two sub-bands and the parasitic capacitances are neglected. In the higher band the inductance is set to L_h and we have

$$f_{h,h} = \frac{1}{2\pi\sqrt{L_h C_{VARh}}} \;;\; f_{h,l} = \frac{1}{2\pi\sqrt{L_h C_{VARl}}} \Rightarrow \frac{f_{h,h}}{f_{h,l}} = \sqrt{\frac{C_{VARl}}{C_{VARh}}} \tag{3.9}$$

whereas in the lower band the inductance is set to L_l and we have

$$f_{l,h} = \frac{1}{2\pi\sqrt{L_l C_{VARh}}} \;;\; f_{l,l} = \frac{1}{2\pi\sqrt{L_l C_{VARl}}} \Rightarrow \frac{f_{h,h}}{f_{h,l}} = \sqrt{\frac{C_{VARl}}{C_{VARh}}} \tag{3.10}$$

Equations (3.9) and (3.10) indicate that the ratio between sub-band frequency extremities is constant. As a result, the fractional tuning range from the higher to the lower band does not change with the variation of the tank inductance.

The variation of the equivalent tank inductance usually involves the introduction of a parasitic capacitance, which must be taken into account for a fairly comparison with the switched-capacitor coarse tuning approach. In this case, equation (3.10) becomes

$$\begin{aligned} &f_{l,h} = \frac{1}{2\pi\sqrt{L_l (C_{VARh} + C_{PAR})}} \;;\; f_{l,l} = \frac{1}{2\pi\sqrt{L_l (C_{VARl} + C_{PAR})}} \\ &\Rightarrow \frac{f_{h,h}}{f_{h,l}} = \sqrt{\frac{C_{VARl} + C_{PAR}}{C_{VARh} + C_{PAR}}} \end{aligned} \tag{3.11}$$

where C_{PAR} is the parasitic capacitance.

The fractional tuning range in the lower band is

$$TR_l = 2 \cdot \frac{f_{l,h} - f_{l,l}}{f_{l,h} + f_{l,l}} = 2 \cdot \frac{\sqrt{\frac{C_{VARl} + C_{PAR}}{C_{VARh} + C_{PAR}}} - 1}{\sqrt{\frac{C_{VARl} + C_{PAR}}{C_{VARh} + C_{PAR}}} + 1} \tag{3.12}$$

By expressing C_{PAR} as $C_{PAR} = \xi \cdot C_{sw}$, equation (3.12) can be re-written as

$$TR_l = 2 \cdot \frac{\sqrt{\frac{1 + \xi - \xi\left(\frac{2 - TR_h}{2 + TR_h}\right)^2}{(1 - \xi)\left(\frac{2 - TR_h}{2 + TR_h}\right)^2 + \xi}} - 1}{\sqrt{\frac{1 + \xi - \xi\left(\frac{2 - TR_h}{2 + TR_h}\right)^2}{(1 - \xi)\left(\frac{2 - TR_h}{2 + TR_h}\right)^2 + \xi}} + 1} \tag{3.13}$$

Equations (3.8) and (3.13) are plotted in Fig. 3.5 as a function of TR_{h}. The inductive coarse tuning technique provides better performance compared with the switched-capacitor approach provided that C_{PAR} is lower than C_{sw}. The tuning range improvement is more evident for higher value of TR_{h}. If C_{PAR} is equal to C_{sw}, identical tuning range performance is provided.

Fig. 3.6 shows the percent reduction of TR_{l} compared with TR_{h}.

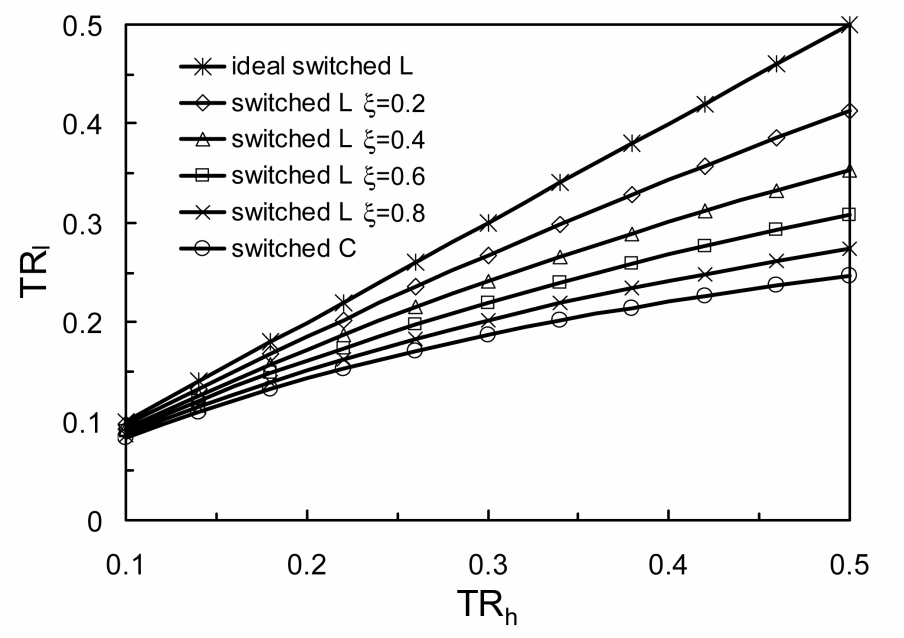

Fig. 3.5. *TR_l as a function of TR_h for switched-capacitor and switched-inductor techniques.*

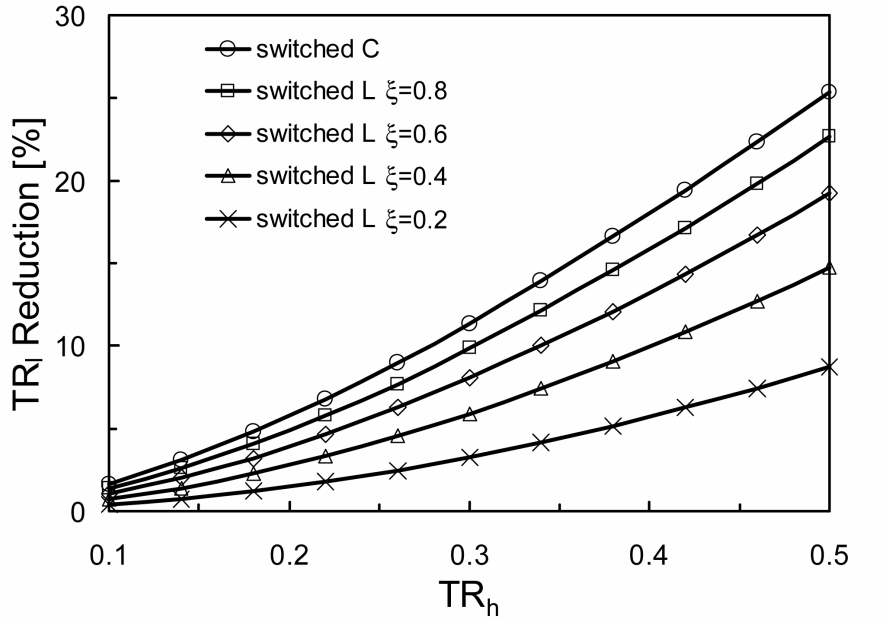

Fig. 3.6. TR_l *reduction vs.* TR_h.

3.2 Shunt-connected switched-coupled inductors

As discussed in the previous section, the inductive coarse tuning techniques can provide phase noise optimization and robust start-up condition without increasing power consumption in the lower portion of the tuning range. However, the main drawback of the inductive coarse tuning techniques is related to a higher degradation of the overall tank quality factor compared with the switched-capacitor approach. Moreover, the additional parasitic capacitance introduced by the variable inductor must be minimized to preserve the tuning range. Therefore, the technique adopted for the variable inductance implementation represents a critical design issue. Actually, both resistive and capacitive parasitics must be carefully considered to make effective the potentially higher performance of the inductive coarse tuning approach with respect to the switched-capacitor one.

Fig. 3.7 shows the schematic of the proposed variable inductor.

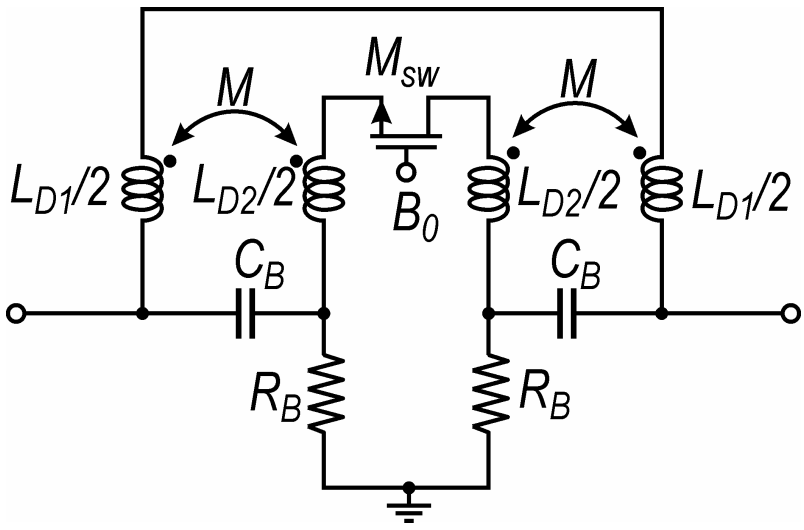

Fig. 3.7. *Schematic of the proposed variable inductor.*

It consists of two mutually-coupled differential inductors (L_{D1}, L_{D2}), which are shunt-connected with AC coupling by means of a NMOS transistor

(M_{sw}). Switch M_{sw} is biased to GND through R_B resistors.

Assuming an ideal overlap between the sub-bands, the following identity holds

$$L_{eq} = \frac{imag\left[Z_{eq}(j\omega)\right]}{\omega} = L_{D1}\frac{C_{VARl}}{C_{VARh}} = L_{D1}\left(\frac{2+TR_h}{2-TR_h}\right)^2 \tag{3.14}$$

where Z_{eq} is the impedance of the shunt-connected mutually-coupled inductors with the switch on.

Therefore, the ratio between L_{eq} and L_{D1} univocally defines TR_h. Considering capacitors C_B shorted at the operating frequency and neglecting the switch resistance, Z_{eq} can be expressed as

$$Z_{eq}(j\omega) = \frac{R_{D1}R_{D2} - \omega^2(L_{D1}L_{D2} - k^2L_{D1}L_{D2}) + j\omega\left(L_{D1}R_{D2} + L_{D2}R_{D1}\right)}{R_{D1} + R_{D2} + j\omega\left(L_{D1} + L_{D2} - 2k\sqrt{L_{D1}L_{D2}}\right)} \tag{3.15}$$

where R_{D1} and R_{D2} are the series loss resistances of the integrated spirals and k is the mutual coupling coefficient.

According to equation (3.15), for a given frequency and inductance L_{D1}, L_{eq} and hence TR_h, is a function of both L_{D2} and k. Fig. 3.8 reports the TR_h and the ratio between the equivalent quality factor of the shunt-connected inductors, Q_{eq}, and the quality factor of L_{D1} (Q_{D1}). The curves were calculated assuming R_{D1}=R_{D2} and neglecting the switch resistance. When inductor L_{D2} is shunt-connected with L_{D1}, a substantial improvement of the quality factor is achieved. Moreover, defined a TR_h target, a proper combination of L_{D2} and k must be chosen to maximize the quality factor provided by the shunt-connected mutually-coupled inductors.

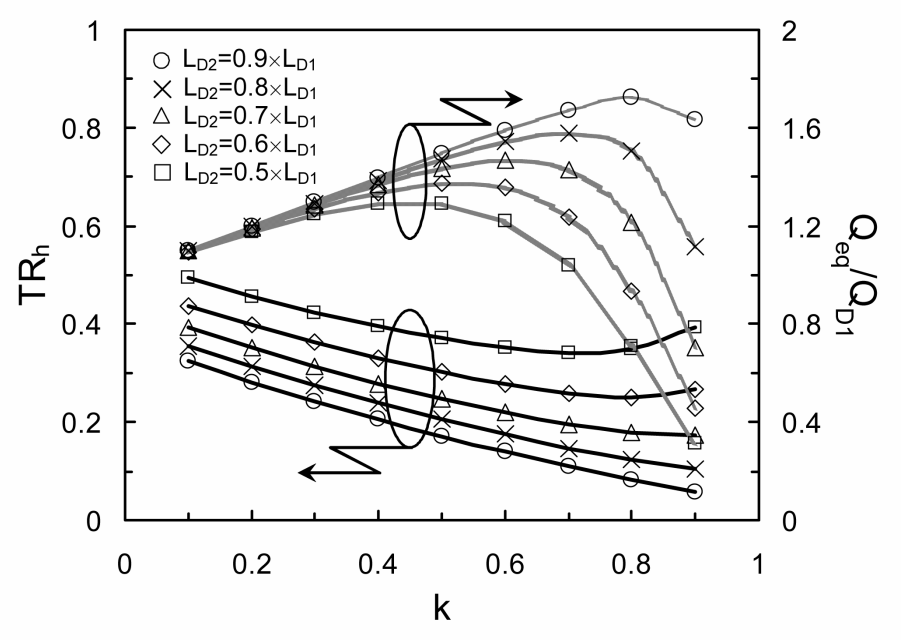

Fig. 3.8. *TR_h and Q_{eq}/Q_{D1} vs. k.*

Fig. 3.9 reports the ratio between the switch on-resistance R_{sw} and R_{D2} which makes Q_{eq} equal to Q_{D1}.

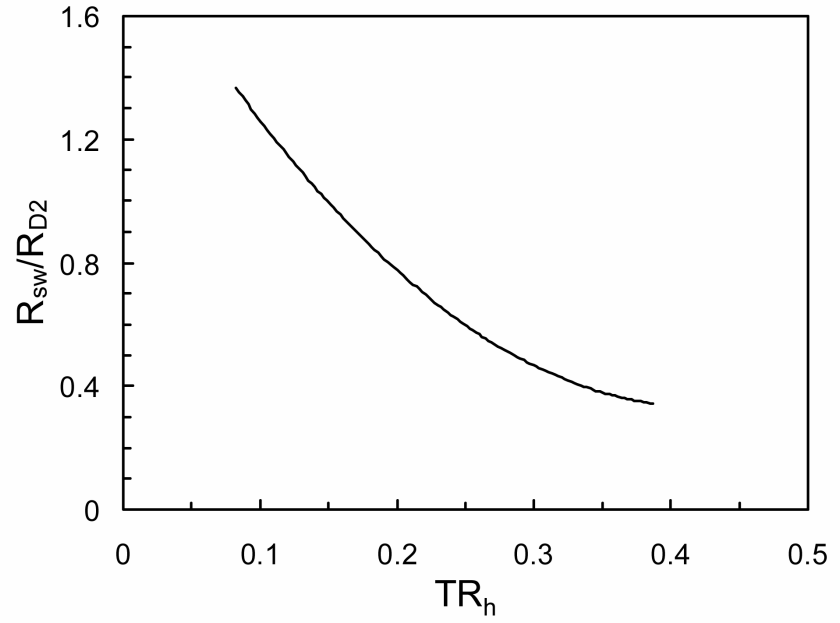

Fig. 3.9. *Ratio between* R_{sw} *and* R_{D2} *for which* $Q_{eq}=Q_{D1}$.

The curve was estimated by considering for each value of TR_h the optimum combination of L_{D2} and k which maximizes L_{eq}. Fig. 3.9 shows that high values of R_{sw} with respect to R_{D2} can be tolerated without loosing the advantage in terms of Q enhancement provided by the proposed topology. Therefore, the detrimental effect of the switch resistance on the quality factor is mitigated by the shunt connection. AC-coupled inductors are adopted to minimize the switch resistance, R_{sw}, thus avoiding the use of complementary switch solution or very large transistors [36]. Indeed, the switch is implemented by means of a NMOS transistor with source/drain biased to ground. As a result, the gate-source voltage of transistor M_{sw} is equal to the supply voltage and a low $R_{sw}C_{par}$ product is achieved at advantage of both tuning range and phase noise performance.

3.3 Varactor configuration

Wide tuning range along with low phase noise is one of the main issues in the design of wideband sub-μm CMOS *LC* VCOs. Indeed, a low supply voltage dictates the use of varactors with steep *C(V)* characteristic (i. e., with high gain) to achieve wide tuning range. On the other hand, a high gain degrades phase noise performance due to the AM-to-PM conversion mechanism [46].

Accumulation mode MOS varactors have been extensively employed in wideband VCOs [33] [47]. In these varactors, the capacitance variation is achieved within a small range of the control voltage. As a consequence, the VCO gain (K_{VCO}), defined as the derivative of frequency with respect to the tuning voltage, exhibits a high ratio between its maximum and average values. Phase noise and tuning range optimization is achieved by minimizing this ratio and maximizing the K_{VCO} average value, respectively.

Fig. 3.10 shows the proposed varactor configuration.

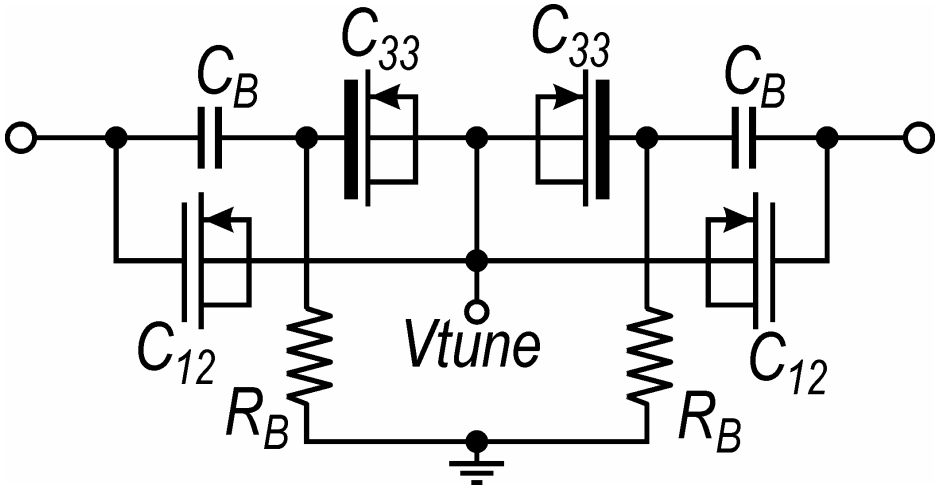

Fig. 3.10. *Proposed varactor configuration.*

The topology was properly designed to provide a high average K_{VCO} along with minimization of its peak value. The varactor is implemented by connecting in parallel thin (C_{12}) and thick (C_{33}) oxide accumulation mode devices, which are biased at different voltages. K_{VCO} optimization is hence achieved by adopting a distributed bias technique [48] and by exploiting the different *C(V)* characteristic of the thin and thick oxide varactors. Indeed, thick oxide varactors exhibit a gentle variation of the capacitance compared with the thin oxide ones. The two different *C(V)* characteristics can be combined and properly shifted by adopting different gate bias voltages. Moreover, the overall *C(V)* characteristic can be further optimized by properly weighting the capacitance provided by each different varactor. With the proposed technique, K_{VCO} optimization is provided by only using the naturally available bias points (GND for the thick oxide varactors and V_{DD}-V_{SGPMOS} for the thin oxide varactors) minimizing the bias circuitry. As a consequence, the phase noise performance is less affected by the varactor bias resistances [48]. Finally, it is worth noting that a reduction of supply voltage, and thus of tuning

control voltage, slightly affects the overall *C(V)* characteristic since it involves the region where the varactor capacitance exhibits a minimum variation (i.e., low V_{TUNE} value for thin oxide varactor and high V_{TUNE} value for thick oxide varactor). As a consequence, VCO tuning range performance is preserved.

3.4 VCO design

Fig. 3.11 shows the schematic of the proposed VCO, which adopts a cross-coupled complementary topology.

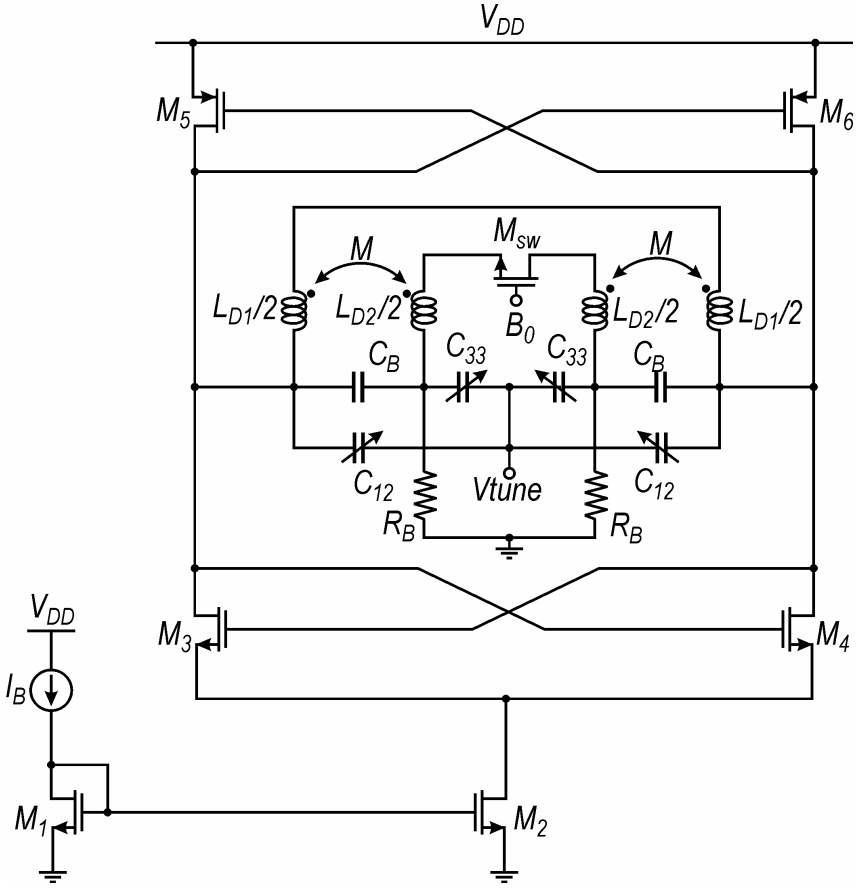

Fig. 3.11. *Complete VCO with the proposed* LC *tank.*

This solution guarantees robust start-up with lower bias current with respect to NMOS-only VCO but exhibits higher parasitic capacitances, which

impact the tuning range. However, the oscillation amplitude of the complementary VCO can be twice as large as the NMOS-only VCO for the same bias current. Therefore, the tank inductance of the complementary VCO that provide phase noise optimization is half. As a consequence, larger varactors for better tuning range can be adopted. Of course, the ratio between the varactor capacitance and the overall tank parasitic capacitance definitively determines which topology provides the best tuning range performance. The main contribution to the overall tank parasitic capacitance for the NMOS-only VCO is given by both the gate-source capacitances of the NMOS transistors and the inductor parasitic capacitance. For the complementary VCO, the contribution of the gate-source capacitances of the PMOS cross-coupled transistors must be added, but the inductor parasitic capacitance is lower due to the lower inductance. The inductor parasitic capacitance depends on the operating frequency. Indeed, at low operating frequencies, large tank inductances are usually adopted to reduce power consumption, as mentioned above.

An accurate evaluation was performed of the two topologies using a conventional *LC* tank with thick oxide accumulation mode MOS varactors and setting equal transconductance gain and bias current of the two circuits. The conclusion was that the complementary topology in our technology exhibits better tuning range with operating frequencies lower than 2 GHz. Therefore, we selected the complementary topology.

According to the VCO in Fig. 3.11, the channel width and the multiplicity of the cross-coupled transistors, M_3-M_4 and M_5-M_6, were set by considering a trade-off between start-up condition and tuning range. Each NMOS transistor consists of 10 shunt-connected minimum-length devices with a 10-μm width. The PMOS transistors were set two times larger than NMOS ones. The overall parasitic capacitance of the two cross-coupled pairs

is around 500 fF. Large devices with long channel length (1 μm) were adopted for the current mirror M_1-M_2 since it affects the phase noise performance at low offset frequency [46].

The layout of the shunt-connected switched-coupled inductors is shown in Fig 3.12. The geometrical parameters of the two inductors were properly set according to the design guidelines highlighted in Fig. 3.8. At this aim, electromagnetic simulations were extensively performed using ADS Momentum [49]. Each spiral was implemented using the top thick metal layer available in the adopted CMOS process. The width and spacing of the spirals are 15 μm and 3 μm, respectively. Inductor L_{D1} is a four-turn coil with an inner radius of 84 μm. Inductor L_{D2} is a two-turn coil with an inner radius of 190 μm. L_{D2} was placed concentrically outside L_{D1}.

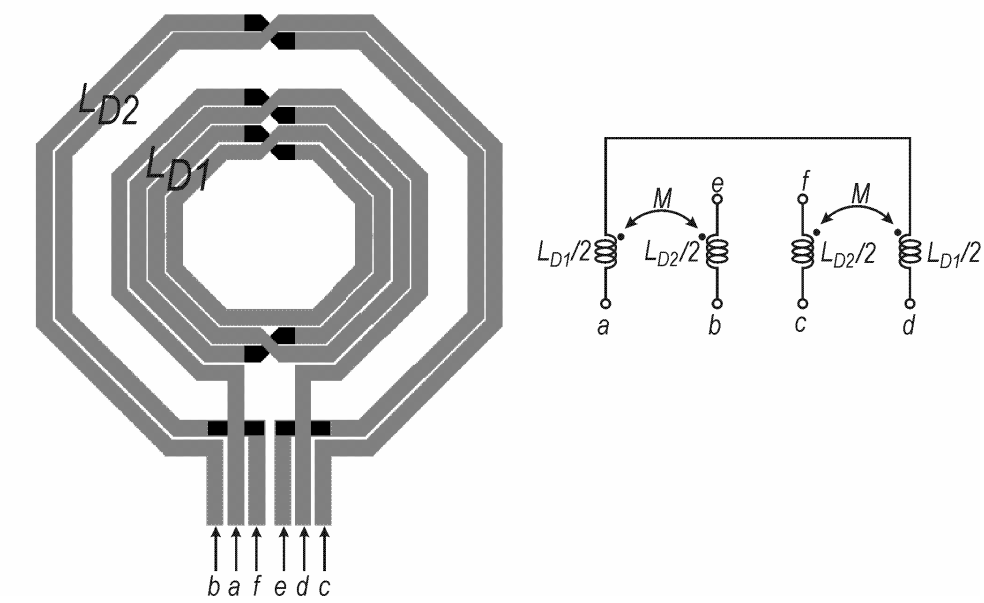

Fig. 3.12. *Layout and electrical model of the switched-coupled inductors.*

Fig. 3.13 reports the simulated inductance values, whereas Fig. 3.14 reports the simulated quality factor values.

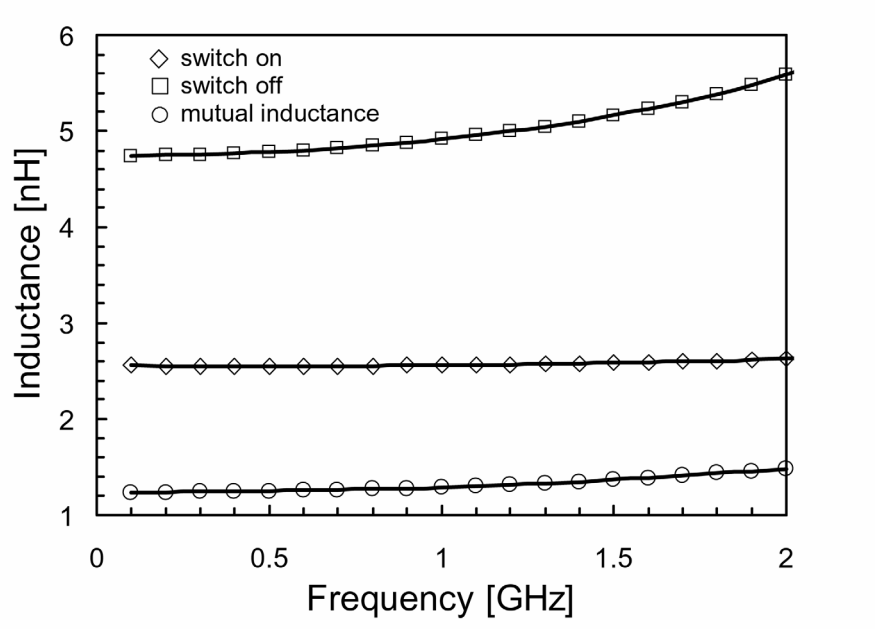

Fig. 3.13. *Tank inductance.*

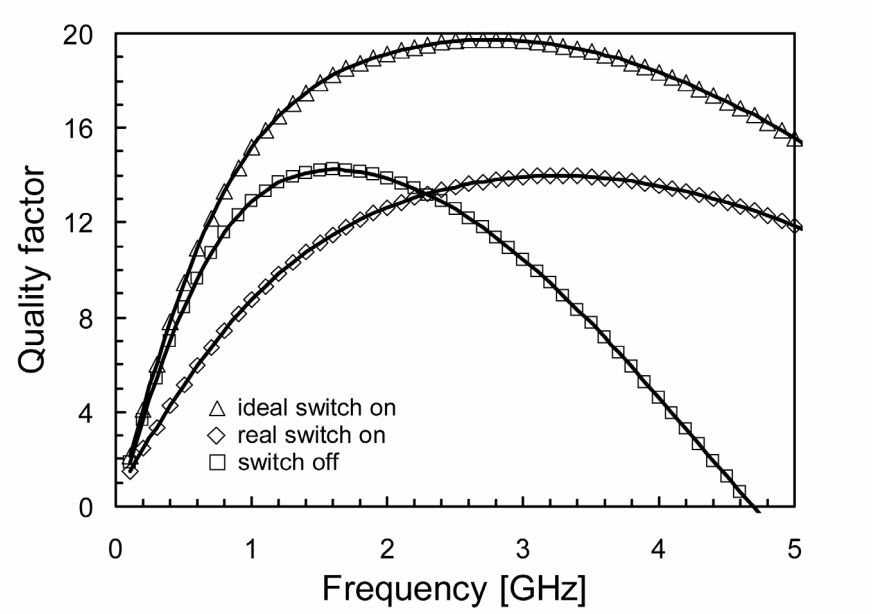

Fig. 3.14. *Quality factors of the switched-coupled inductors.*

When the switch is off the inductance is 4.7 nH (i.e, equal to L_{D1}) and the quality factor is around 14 in the band of interest (1.2-1.5 GHz). The

equivalent inductance with the switch on is instead 2.5 nH with L_{D2} equal to 3.3 nH. Therefore, instead of the simple shunt value of 1.9 nH the equivalent inductance is enhanced by a factor 1.3 due to the mutual coupling. This means less silicon area and parasitic capacitances with respect to the simple shunt connection [36]. The coupling factor k between the spirals is 0.36. Considering an ideal switch, the quality factor of the shunt-connected coupled inductors in the band of interest (1.5-1.9 GHz) would have been around 18.

Actually, by implementing the switch with 6 shunt-connected minimum length NMOS transistors with a 4-μm width, resistance R_{on} is 2 Ω and the quality factor of the coupled inductor is around 12. When the switch is on, inductor L_{D2} is differentially driven and hence the overall parasitic capacitance of the equivalent tank inductor is lower [50]. This capacitance is 253 fF and 122 fF with the switch off and on, respectively. Minimal length and minimal width varactors were employed to optimize the quality factor. Fig. 3.15 shows the *C(V)* characteristics of the varactors along with the overall ones.

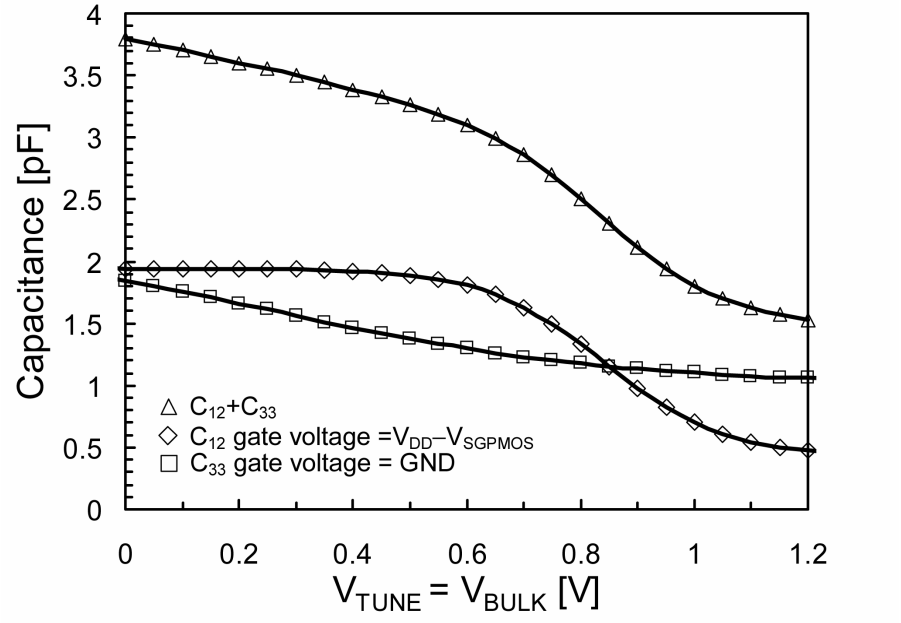

Fig. 3.15. C(V) *varactor characteristics.*

The average and maximum capacitance variation of the overall varactor configuration is 1.88 pF/V and 4 pF/V, respectively. In the higher band, these values correspond to average and peak K_{VCO} values of 450 MHz/V and 850 MHz/V, respectively. By using only thin oxide varactors, the same K_{VCO} average value is provided with a maximum K_{VCO} of 1.1 GHz/V. Therefore, the K_{VCO} peak value was reduced by 25%. The overall quality factor of the varactor configuration is higher than 100 in the whole tuning range.

Finally, 10-pF metal-insulator-metal capacitors (C_B) and 10-kΩ varactor bias resistors were adopted for AC-coupling varactors and inductors. The value of varactor bias resistors has been chosen as compromise between two different constrains. A low value resistor affects the quality factor of the LC tank, whereas a high value resistor increases phase noise resistor contribution.

Chapter 4

Design of a 0.6-mW wideband auto-calibrated I/Q generator

Generation of LO in-phase/quadrature (I/Q) signals is a key issue in modern highly-integrated transceivers. Indeed, accurate I/Q signals are needed in low-IF receivers to provide high image rejection [21] and in zero-IF receivers to avoid signal distortion [20], which can greatly affect BER. Moreover, the current trend towards wideband and ultra low-power systems makes more challenging the generation of accurate LO I/Q signals.

Several techniques have been proposed to implement quadrature signals [52]-[68]. Typically are generated by using polyphase filters based on RC-CR phase shifters [52]-[54] or by dividing by 2 the LO signal by means of a master-slave flip-flop [55]-[57]. Other commonly adopted approaches are based on quadrature cross-coupled *LC* VCOs [58]-[63] or injection-locked ring oscillators [64]. To obtain accurate I/Q signals with respect to process, voltage, and temperature (PVT) variations, auto-calibrated I/Q generators are implemented by using a feedback control based on delay-locked loops (DLL), which detects and properly corrects the phase error [54]-[57] [65]-[68].

A quadrature generation based on master-slave flip-flops has been chosen to comply with the transceiver proposed in chapter 2, whose operating frequency range from 300 MHz to 960 MHz. However, due to the low-power consumption, statistical simulations showed that the quadrature phase error of the I/Q signals at 1 GHz produced by a master-slave divider can exceed 5° in

worst case conditions. Taking into account for other circuitry in the I/Q signal path (i.e., limiters and buffers), the overall error reaches 12°. Moreover, the phase error depends on both temperature and power supply variations. On the other hand, the phase error of the *IQ* mixer and analog base-band circuits is lower than 2.5° thanks to the chosen low IF frequency. This error is manly due to process mismatches and shows a low dependence on temperature and power supply. This means that the stability of the phase error with respect to temperature and power supply as well as the dependence on the operating frequency have to be faced in the LO side.

In view of these remarks, the proposed I/Q generator has been provided with a feedback control based on auto-calibration DLLs. The adopted phase correction technique is able to independently control the quadrature and duty cycle of the generated signals. The target specification of the LO I/Q generator before calibration is to reduce the maximum phase error to less than 2° and provide accuracy with respect to frequency, temperature, and power supply, to make possible simple digital calibration during the manufacture test. Of course, a digital calibration in the I/Q generator has to be considered to compensate for the overall quadrature phase error of the receiver including the residual LO error itself. The final target for the receiver is a quadrature phase error lower than 1° to be compliant with an image rejection ratio higher than 40 dB under PVT and frequency variations. Of course, an additional compensation of mixer and base-band gain errors due to process mismatches could be required to fulfill the image rejection specification.

It is worth mentioning that a highly-accurate LO I/Q generator (i.e., a phase error lower than 1°) before calibration would be useless, given the phase error of the I/Q mixer and analog base-band, and the consequent need for digital calibration. On the other hand, a digital calibration alone during manufacturing would not be able to guarantee accuracy without a mechanism of stabilization of the phase error against temperature and power supply

variations [69] [70].

The current consumption of the proposed I/Q generator is kept lower than 0.5 *m*A from a 1.2-V power supply.

The chapter consist of two Sections. Section 4.1 reports the description of the basic building block of the I/Q generator, that are the phase tunable divider and the phase tunable amplifier. Section 4.2 presents the implementation details of the proposed I/Q generator.

4.1 Phase-tunable divider and limiting amplifier

The architecture of the I/Q generator is shown in Fig. 4.1.

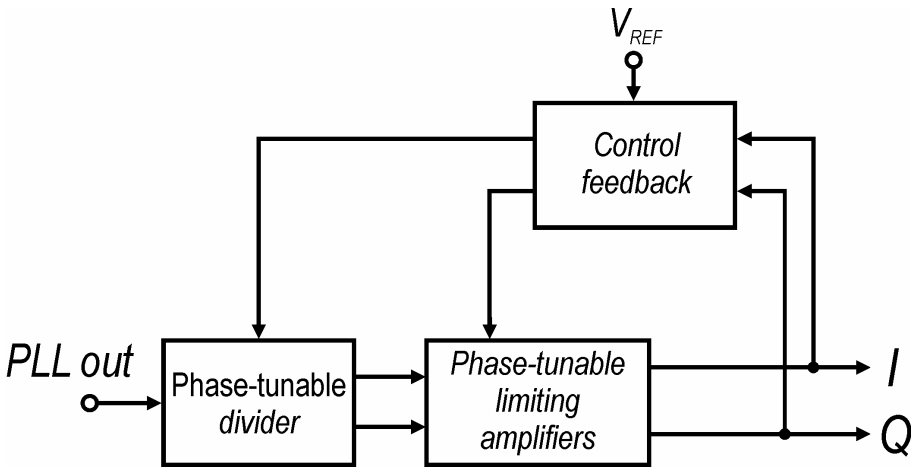

Fig. 4.1. *Architecture of the I/Q generator.*

The quadrature correction is performed through a control feedback, which detects the quadrature error and properly drives the divider and limiting amplifier.

The phase-tunable divider and the phase-tunable limiting amplifier represent the core circuits of the I/Q generator since they provide an efficient way to control the phase of the I/Q signals.

4.1.1 Phase-tunable divider

The schematic of a phase-tunable divider is shown in Fig. 4.2a.

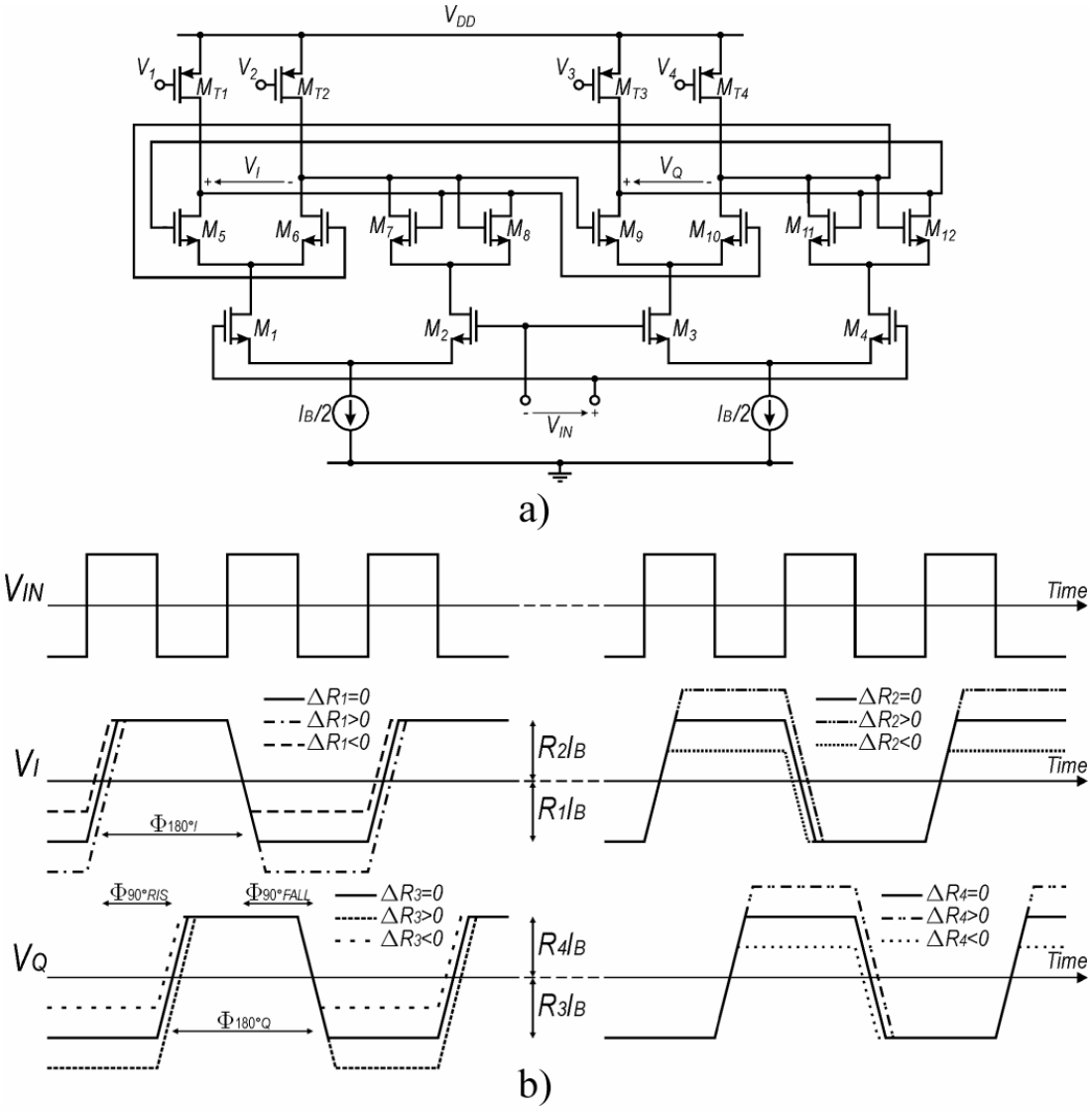

Fig. 4.2. *Phase-tunable divider. a) Schematic. b) Clock and output waveforms.*

The phase shift of the quadrature signals are performed by tuning the load resistances, which are implemented by means of the triode-biased PMOS transistors M_{T1}-M_{T4}. The load resistances variation is obtained through the gate voltages V_1, V_2, V_3, V_4. Fig. 4.2b shows the quadrature differential output

waveforms V_I and V_Q. The low logic level of V_I is determined by the channel resistance R_1 of M_{T1}, whose variation ΔR_1 due to V_1 allows a time shift of the zero-crossing that occurs during the rising edge of V_I. On the other hand, the high logic level of V_I is determined by the channel resistance R_2 of M_{T2}, whose variation ΔR_2 due to V_2 allows a time shift of the zero-crossing during the falling edge of V_I. Similarly, the variations of the channel resistances of M_{T3} and $M_{T4,}$ R_3 and R_4, due to V_3 and V_4 control the zero-crossing shift that occurs during rising and falling edges of V_Q, respectively. The zero-crossing shift results in a phase shift at the output of limiting amplifier. Therefore, the phase shift between rising and falling edges of V_I and V_Q can independently be controlled by means of voltages V_1, V_3 and V_2, V_4, respectively.

Thanks to the same mechanism, the duty cycle of the I and Q waveforms is determined by voltages V_1, V_2 and V_3, V_4, respectively.

It is worth noting that the difference among the *RC* time constants of the divider loads was verified to be a second-order effect, which slightly affects the phase control.

To maximize the phase variation of the quadrature signals, voltages V_1, V_3 and V_2, V_4 are assumed differential. Therefore, it can be written

$$\begin{aligned} V_1 &= V_{CM1} + \frac{\Delta V_{G1}}{2} \\ V_2 &= V_{CM2} + \frac{\Delta V_{G2}}{2} \\ V_3 &= V_{CM1} - \frac{\Delta V_{G1}}{2} \\ V_4 &= V_{CM2} - \frac{\Delta V_{G2}}{2} \end{aligned} \tag{4.1}$$

From equations (4.1), the gate control voltages can be defined as

$$
\begin{aligned}
V_{1,3} &= V_1 - V_3 = \Delta V_{G1} \\
V_{2,4} &= V_2 - V_4 = \Delta V_{G2} \\
V_{1,2} &= V_1 - V_2 = V_{CM1} - V_{CM2} + \frac{1}{2}(\Delta V_{G1} - \Delta V_{G2}) \\
V_{3,4} &= V_3 - V_4 = V_{CM1} - V_{CM2} - \frac{1}{2}(\Delta V_{G1} - \Delta V_{G2})
\end{aligned}
\tag{4.2}
$$

Modelling I and Q rising and falling edges as capacitive charge/discharge transients, the variations of the phase differences between I and Q rising and falling edges, $\Phi_{90°\mathrm{RIS}}$ and $\Phi_{90°\mathrm{FALL}}$, respectively, and the variations of the duty cycle of I and Q, $\Phi_{180°\mathrm{I}}$ and $\Phi_{180°\mathrm{Q}}$, respectively (see Fig. 4.2b), can be expressed as a function of the gate voltages $V_{\mathrm{i,j}}$ of equations (4.2)

$$
\begin{aligned}
\Delta\Phi_{90°RIS} &\cong 2\pi f\left(\Delta R_3 I_B - \Delta R_1 I_B\right)\frac{C_p}{I_B} = -\frac{2\pi f C_p}{\kappa_p\left(W/L\right)_{1-4}\left(V_{DD} - V_B - V_{TH}\right)^2}V_{1,3} \\
\Delta\Phi_{90°FALL} &\cong 2\pi f\left(\Delta R_4 I_B - \Delta R_2 I_B\right)\frac{C_p}{I_B} = -\frac{2\pi f C_p}{\kappa_p\left(W/L\right)_{1-4}\left(V_{DD} - V_B - V_{TH}\right)^2}V_{2,4} \\
\Delta\Phi_{180°I} &\cong 2\pi f\left(\Delta R_2 I_B - \Delta R_1 I_B\right)\frac{C_p}{I_B} = -\frac{2\pi f C_p}{\kappa_p\left(W/L\right)_{1-4}\left(V_{DD} - V_B - V_{TH}\right)^2}V_{1,2} \\
\Delta\Phi_{180°Q} &\cong 2\pi f\left(\Delta R_4 I_B - \Delta R_3 I_B\right)\frac{C_p}{I_B} = -\frac{2\pi f C_p}{\kappa_p\left(W/L\right)_{1-4}\left(V_{DD} - V_B - V_{TH}\right)^2}V_{3,4}
\end{aligned}
\tag{4.3}
$$

where C_p is the capacitance of the divider output nodes, I_B is the bias current of the divider, f is the I/Q signal frequency, V_B is the common bias voltage of differential signals $\mathrm{V_{i,j}}$.

I and Q waveforms are univocally set by three of the four equations in (4.1)-(4.3). Indeed, only three equations are independent. For instance, by controlling the phase difference between the rising and falling edges of I and Q and the duty cycle of I, the duty cycle of Q is given.

Differential voltage $V_{1,3}$ sets the phase difference between V_I and V_Q

rising edges, while differential voltage $V_{2,4}$ sets the phase difference between V_{I} and V_{Q} falling edges. Therefore, the quadrature of V_{I} and V_{Q} is determined by ΔV_{G1} and ΔV_{G2} whereas the duty cycle correction can independently be performed from the quadrature control by varying the common mode voltage of $V_{1,2}$ and $V_{3,4}$, (i.e., V_{CM1} with respect to V_{CM2}) according to equations (4.2).

4.1.2 Phase-tunable limiting amplifier

To improve the variation range of quadrature control voltages $V_{1,3}$ and $V_{2,4}$, the duty cycle control can be done in limiting amplifiers. Fig. 4.3 shows the schematic of a phase-tunable limiting amplifier and sketches its operation.

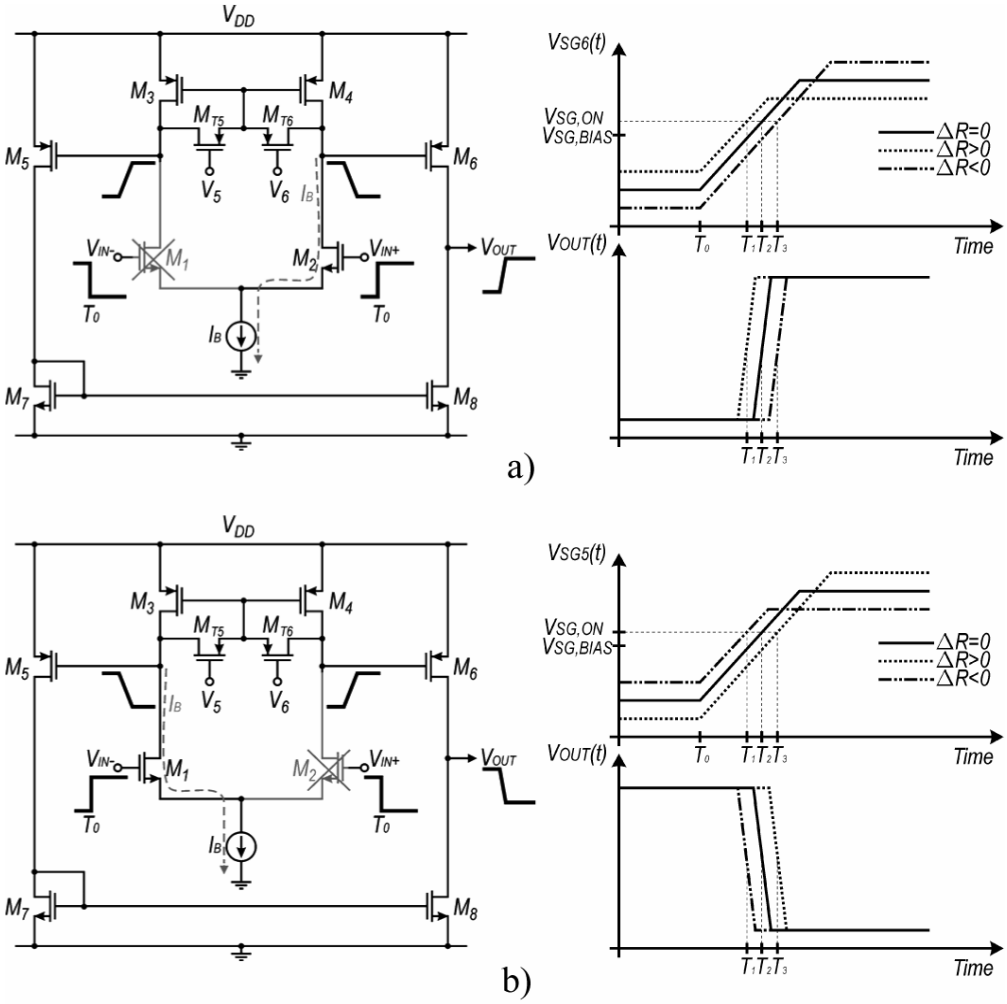

Fig. 4.3. *Phase-tunable divider. a) Schematic. b) Clock and output waveforms.*

The input stage is a differential stage loaded by transistors M_3, M_4 and triode-biased MOS transistors M_{T5} and M_{T6}. To stabilize the drain voltages of M_1-M_4, a common mode feedback is performed by connecting the common node of M_{T5} and M_{T6} to the common gate of M_3, M_4. A second stage made up of transistors M_5-M_8 performs further gain and SCL to CMOS conversion (i.e., limiting operation).

Considering a large-amplitude differential input signal $V_d=V_{IN+}-V_{IN-}$, the value of V_{SG5} and V_{SG6} can be expressed by the following equations

$$V_{SG5}=\begin{cases} V_{SG5,LOW} \cong V_{SG,BIAS}-\dfrac{1}{2}R_5 I_B & V_d>0 \\ V_{SG5,HIGH} \cong V_{SG,BIAS}+\dfrac{1}{2}R_5 I_B & V_d<0 \end{cases} \tag{4.4}$$

$$V_{SG6}=\begin{cases} V_{SG6,HIGH} \cong V_{SG,BIAS}+\dfrac{1}{2}R_6 I_B & V_d>0 \\ V_{SG6,LOW} \cong V_{SG,BIAS}-\dfrac{1}{2}R_6 I_B & V_d<0 \end{cases} \tag{4.5}$$

where $V_{SG,BIAS}$ is the source-gate bias voltage of transistors $M_{3\text{-}6}$, R_5 and R_6 are the channel resistances of M_{T5} and M_{T6}, and I_B is the bias current of the limiting amplifier. In a first approximation, we have considered negligible the drain resistances of transistors M_1-M_4.

MOS resistances R_5 and R_6 are controlled by gate voltages V_5 and V_6. Assuming $V_{5,6}=V_5-V_6$ a differential signal, also R_5 and R_6 vary in a differential manner, i.e. $R_5=R_{CM}+\Delta R/2$ and $R_6=R_{CM}-\Delta R/2$. Variation ΔR modifies the source-gate voltage transient of transistors M_5 and M_6 as shown in Fig. 4.3. If we name $V_{SG,ON}$ the source-gate voltage of M_5 and M_6 which causes output logic switching, the time to reach $V_{SG,ON}$ and hence the moment of the output logic transitions will depend on ΔR.

When input signal V_d is high (see Fig. 4.3a), a lower (higher) R_6 that is $\Delta R>0$ ($\Delta R<0$) increases (reduces) $V_{SG6,LOW}$, thus reducing (increasing) the time required to M_6 to achieve $V_{SG,ON}$. As a consequence, the rising edge of the output voltage is anticipated (delayed).

When input signal V_d is low (see Fig. 4.3b), a higher (lower) R_5 that is $\Delta R>0$ ($\Delta R<0$) reduces (increases) $V_{SG5,LOW}$, thus increasing (reducing) the time required to M_5 to achieve $V_{SG,ON.}$ As a consequence, the falling edge of the output voltage is delayed (anticipated).

In conclusion, considering a large-amplitude square-wave input signal V_d, a positive (negative) ΔR increases (reduces) the duty cycle of the output square waveform.

For a symmetrically designed limiting amplifier, the switching value $V_{SG,ON}$ has to be equal for both positive and negative logic levels. Rising and falling edges of transistors M_5 and M_6 are approximately determined by slew-rate transitions. The pulse width variation, $\Delta\Phi_{180°}$, of V_{OUT} is given by

$$\Delta\Phi_{180^\circ} \cong 2\pi f\left(\Delta R_5 I_B - \Delta R_6 I_B\right)\frac{C_p}{I_B} = \frac{2\pi f C_p}{\kappa_p\left(W/L\right)_{5,6}\left(V_{DD} - V_{SG,BIAS} - V_B - V_{TH}\right)^2}V_{5,6} \quad (4.6)$$

where C_p is the overall capacitance at the gate node of transistors M_5 and M_6 and V_B is the bias voltage of differential signal $V_{5,6}$.

It is worth mentioning that the adopted technique is based on three independent control loops, which work simultaneously to provide quadrature signals with a 50% duty cycle. Therefore, this approach does not exhibit stability problems and does not require sequential or iterative calibration [54] [66].

4.2 I/Q generator implementation

The detailed block diagram of the proposed I/Q generator is shown in Fig. 4.4.

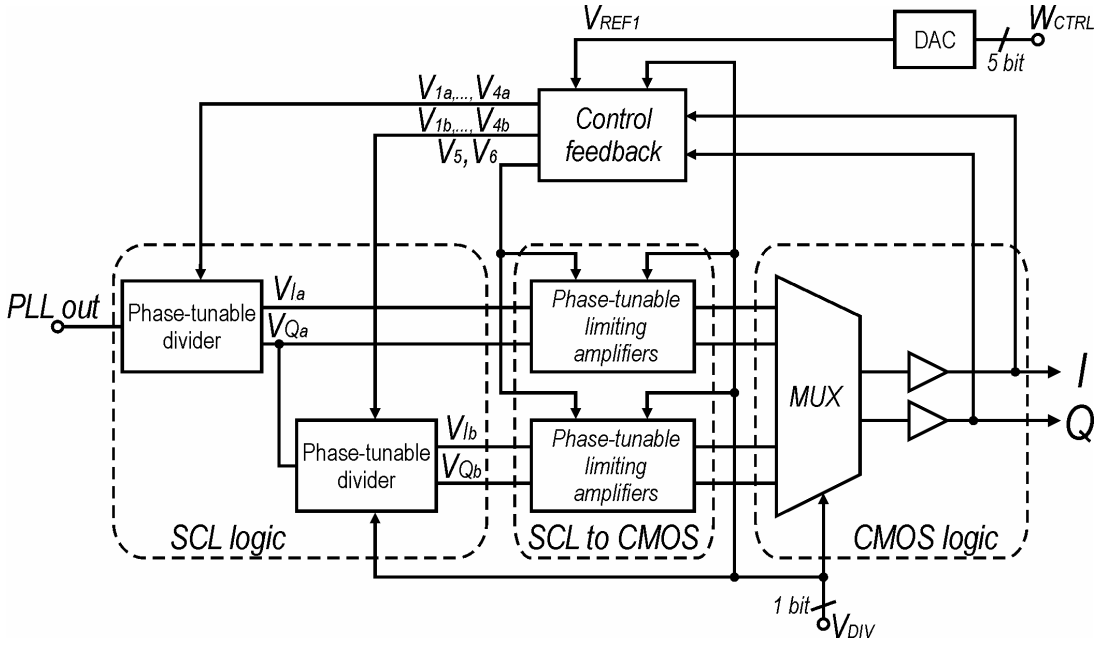

Fig. 4.4. *Block diagrams of the I/Q generator.*

The proposed generator exploits the phase-tunable dividers for the quadrature correction and the limiting amplifiers to control the duty cycle. Control voltages V_1-V_4 in Fig. 4.4 are named V_{1a}-V_{4a} or V_{1b}-V_{4b} when they drive the first or second divider, respectively. A switch matrix manages V_{1a}-V_{4a} and V_{1b}-V_{4b} according to the division factor of the I/Q generator.

The circuit is made up of the cascade of two source-coupled logic (SCL) dividers to divide by-2 or by-4 the VCO output signal. Each divider is followed by two limiting amplifiers for the I and Q paths, which perform the SCL-to-CMOS logic level conversion to minimize the power consumption of multiplexer and buffers.

The divide-by-2 or by-4 operating mode is selected by means of the

control bit V_{DIV}. In the divide-by-2 operating mode, the second divider and the related limiting amplifiers are turned off, whereas in the divide-by-4 operating mode the cascade of the two dividers is enabled and the limiting amplifiers related to the first divider are turned off.

A multiplexer controlled by V_{DIV} selects the proper input signals. The multiplexer output signals were properly buffered to drive the RX/TX mixers.

To symmetrically arrange the I and Q paths of the first divider, a non-biased replica of the second SCL divider was connected to V_{Ia} in Fig. 4.4.

The control feedback circuit detects the phase errors at the buffers output and generates the control signals for the dividers and/or the limiting amplifiers. The reference voltage of the control feedback circuit is provided by a 5-bit resistor-ladder digital-to-analog converter (DAC).

4.2.1 Phase-tunable divider and limiting amplifier

The design of the phase-tunable dividers is the more challenging aspect in the implementation of the I/Q generator. The design issues are exacerbated because of the low-power consumption and the wide operating frequency range.

The variation of the load MOS resistances in Fig. 4.2 has to be high enough to correct the quadrature error under PVT tolerances. On the other hand, the proper circuit operation sets an upper and a lower limit to the MOS resistance values. Indeed, the output time constant in a frequency divider must be sufficiently lower than the signal period [71] [72], and hence the load resistance cannot exceed a maximum value. Additionally, a minimum value of load resistance must be guaranteed for the switching of the divider latching pairs.

In order to set optimal transistor and MOS resistor dimensions for a low-power I/Q generator capable of correcting the quadrature phase error in worst case conditions, proper design arrangements were adopted and extensive

simulations were carried out under PVT variations.

The channel width of transistors M_5-M_{12} in Fig. 4.2 was set about two times the channel width of M_1-M_4 to guarantee a safe drain-source DC value to M_1-M_4 for correct circuit operation. On the other hand, the channel width of transistors M_5-M_{12} was set by considering that a larger device provides safe divider operation with a lower signal swing, but increases the output time constant, thus limiting operating frequency. All transistors use the minimum channel length (L=100*n*m) to minimize parasitic capacitances.

The tail current I_B determines the maximum operating frequency but also the power consumption. The minimum value which guaranteed correct operation up to 1 GHz was 88 μA and 44 μA for the first and the second divider, respectively.

Table I summarizes the adopted values for the divider design parameters.

TABLE I
DIVIDERS DESIGN PARAMETERS

	Value	
Parameter	First divider	Second divider
I_B	88μA	44μA
$M_{1\text{-}4}$ channel width	480*n*m	240*n*m
$M_{5\text{-}12}$ channel width	960*n*m	600*n*m
$M_{T1\text{-}T4}$ channel width	350*n*m	220*n*m

By using the parameter values in Table I and gate voltages for M_{T1}-M_{T4} from 35 to 335 *m*V, MOS load resistances range from 5 kΩ to 10 kΩ and from 13 kΩ to 20 kΩ for the first and second divider, respectively. These resistance variations provide a phase shifting of around 6° for rising and falling edges at 1 GHz. The common mode value of the gate voltages was set to 185 *m*V.

Finally, the phase-tunable limiting amplifier provide a duty cycle control within 15° while drawing a current of 70 μA at 1 GHz. The design of the limiting amplifiers is less critical since highly-accurate control of the duty cycle of the I/Q signals is not required. The only important aspect is power consumptions that is determined by the operating frequency and the load capacitances.

4.2.2 Control feedback circuit

The detailed block diagram of the control feedback circuit is shown in Fig. 4.5.

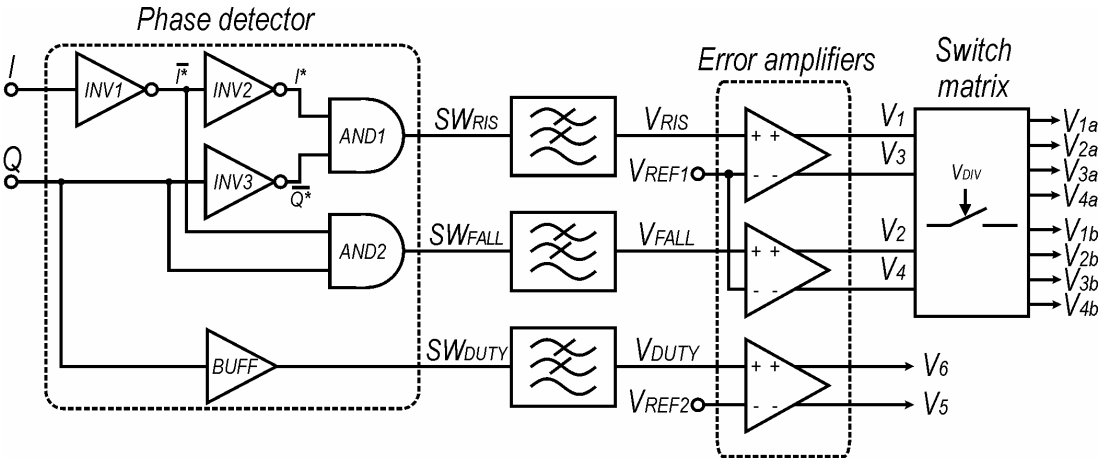

Fig. 4.5. *Block diagram of the control feedback circuit.*

The overall control feedback circuit is made up of three loops (i.e., RIS, FALL, and DUTY loop). The RIS and FALL loops control the phase-tunable dividers whereas the DUTY operate with the phase-tunable limiting amplifiers. Each loop is driven by the phase detector and includes a low-pass filter and an error amplifier.

The phase detector outputs, SW_{RIS}, SW_{FALL}, and SW_{DUTY} are square-wave signals whose duty cycle is proportional to the rising/falling edge differences between I and Q, and to the duty cycle of I/Q, respectively. Signal

SW_{DUTY} is a buffered version of signal I. Since high accuracy is not required, I or Q can be selected for the duty cycle control.

The low-pass filter provides a DC output signal proportional to the duty cycle of its square-wave input signal.

An error amplifier compares the filter output with the reference voltage and produces a differential control voltage for dividers or limiting amplifiers. It also provides proper loop gain to compensate for PVT variations. Each error amplifier is a simple differential stage with resistive load. Diode-connected transistors are adopted in the RIS, FALL, and DUTY error amplifiers to limit their output voltage swing. This in turn limits the load MOS resistance variation in dividers and limiting amplifiers, thus guaranteeing proper operation of the I/Q generator at the start-up.

The phase detector exploits simple digital gates to detect rising and falling edge differences, as shown in Fig. 4.5. Signal SW_{RIS} is performed by the AND of a buffered version of I, I*, and the negated of Q, Q_{NEG}*. Signal SW_{FALL} is produced by the AND of Q and the negated of I, I_{NEG}*. Fig 4.6 highlights the phase detector signals waveform.

The positive time slots of signals RIS and FALL, Δt^*_{RIS} and Δt^*_{FALL}, provide the rising and falling edge differences, respectively, and account for the gate delays. They are given by

$$\begin{aligned} \Delta t_{RIS}{}^* &= \Delta t_{RIS} - \mathrm{T}_{pLH,INV2} - \mathrm{T}_{pHL,INV1} + \mathrm{T}_{pHL,INV3} \\ \Delta t_{FALL}{}^* &= \Delta t_{FALL} - \mathrm{T}_{pLH,INV1} \end{aligned} \tag{4.7}$$

where $T_{pLH,INV1}$, $T_{pLH,INV2}$ and $T_{pHL,INV1}$, $T_{pHL,INV3}$ are the low-to-high and high-to-low propagation delays of inverter INV_1, INV_2 and INV_1, INV_3, respectively.

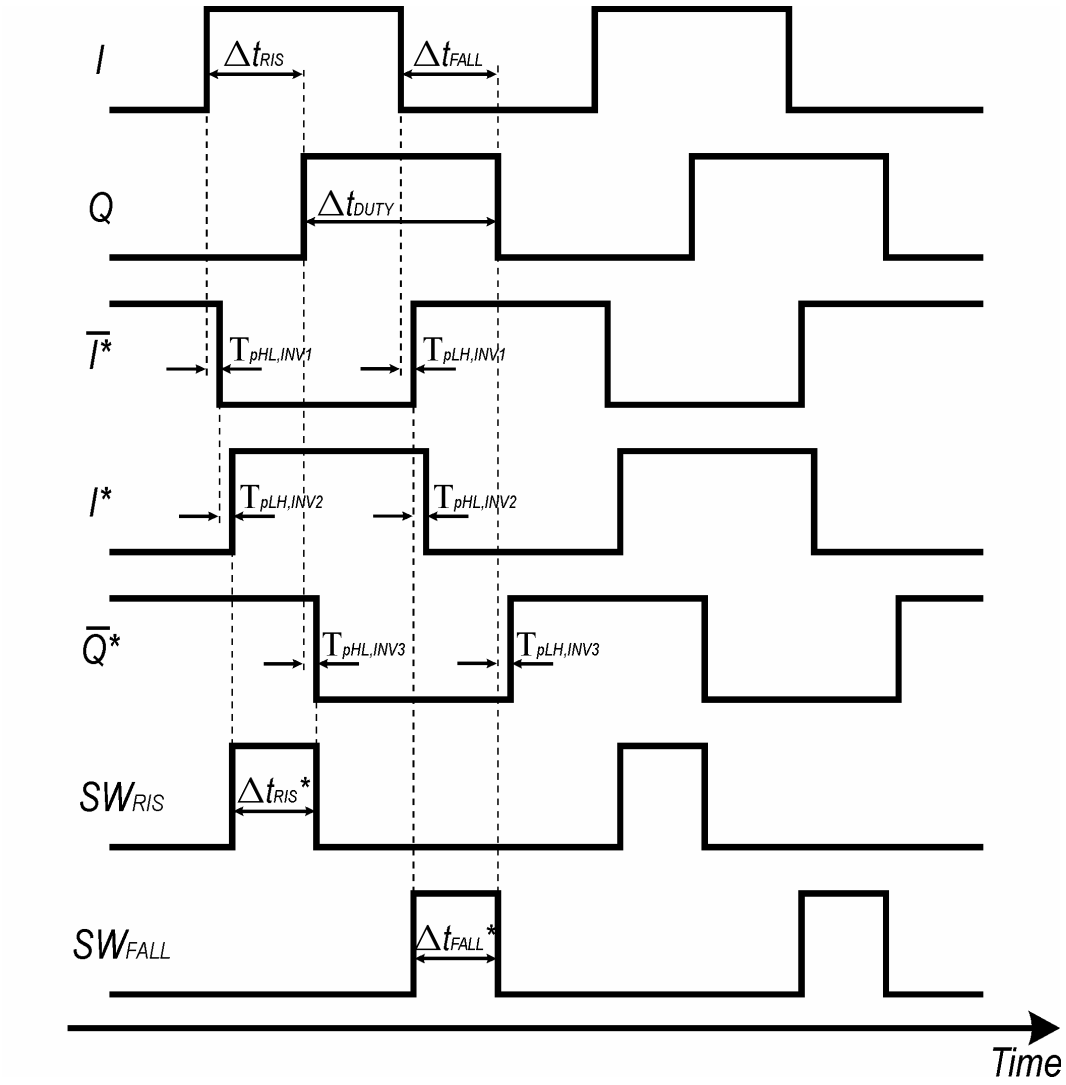

Fig. 4.6. *Phase detector waveforms.*

The phase detector uses minimum size gates to make low the propagation delay and hence the phase error. Moreover, by making $T_{pLH,INV1}=T_{pLH,INV2}$ and $T_{pHL,INV1}=T_{pHL,INV3}$, the phase error in Δt^*_{RIS} and Δt^*_{FALL} due to the propagation delays is nominally equal and can be compensated during calibration. Finally, assuming matched AND gates they do not affect phase error.

Considering ideal I/Q signals and phase detector, output signals SW_{RIS}/SW_{FALL} and SW_{DUTY} are square-wave signals with a 25% and 50% duty

cycle, respectively. Therefore, the ideal DC values at the filter outputs for RIS/FALL and DUTY loops are equal to $V_{DD}/4$ and $V_{DD}/2$, respectively. This means that the gain factor of the phase detector/low-pass filter is 3.3 mV/° (i.e., $V_{DD}/360°$) assuming a 1.2-V power supply.

This phase variation with voltage is low enough to make negligible the phase noise contribution of the I/Q generator compared with the PLL phase noise, even considering the power supply noise of a typical voltage regulator.

Reference voltage V_{REF1} of RIS and FALL loops is set by a 5-bit digital to analog converter, which is used for the digital calibration. The DAC converter is based on a resistor string connected to V_{DD}. The nominal value of V_{REF1} is then $V_{DD}/4$. Reference voltage V_{REF2} is instead fixed and its value is $V_{DD}/2$.

The last block of the control feedback circuit is the switch matrix, which connects V_{ia} to V_i (i=1-4) or to the common mode voltage (i.e.,185 mV) in case of divide-by-2 or divide-by-4 operating mode, respectively. Instead, voltages V_{ib} that drive the second divider are always connected to V_i. On the other hand, the voltages V_5 and V_6 (i.e., differential signal $V_{5,6}$) of the DUTY loop amplifier control the duty cycle by driving the phase-tunable limiting amplifiers.

As previously mentioned, the low-pass filters extract the DC component of their input signal. They also provide closed-loop stability to the control feedback loops by making a dominant pole compensation. The high-frequency poles are instead due to the error amplifiers.

From the RIS and FALL loops, the open-loop gain can be calculated as

$$OL_{gain,RIS-FALL} = G_{EA} \cdot G_{DIV} \cdot G_{PD+LPF} \tag{4.8}$$

where G_A is the gain of the error amplifier, G_{DIV} is the phase-voltage gain factor of the phase-tunable divider, G_{PD+LP} is the gain factor of the phase

detector along with the low-pass filter. The values of G_{EA}, G_{DIV}, and G_{PD+LPF} are 36 V/V, 66 °/V, and 3.3 *m*V/°, respectively, which means an overall loop gain around 18 dB.

The dominant pole frequency was set to 200 kHz to guarantee a phase margin higher than 70° with a unity-gain bandwidth around 3 MHz.

Chapter 5

Measurement results

This chapter presents the experimental characterization of the proposed frequency synthesizer. It was fabricated in a TSMC 90-*n*m CMOS technology, which features six metal layers plus a thick top one. Fig. 5.1 shows a microphotograph of the chip, which occupies a core area of 0.9×0.9 mm^2 excluding bond pads.

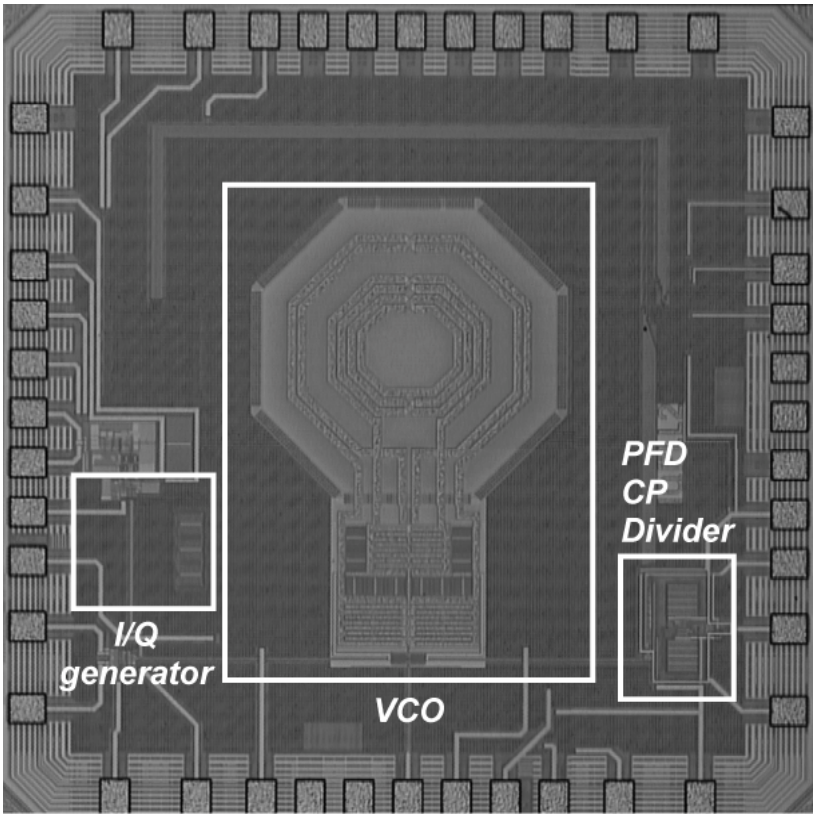

Fig. 5.1. *Die microphotograph.*

The performance of VCO and I/Q generator are presented in Sections 5.1 and 5.2, respectively. A summary of the frequency synthesizer performance can be found in Section 5.3.

5.1 VCO experimental characterization

The measurements were performed locking the VCO with the PLL. The loop-bandwidth was set very low (2-kHz) to make negligible further PLL phase noise contributions in the overall tuning range. An on-chip output buffer provides differential-to-single ended conversion and drives the 50-Ω instrumentation load. It consists of a cascade of three differential stages. The last stage employs 50-Ohm load resistor providing an output power of around −8 dBm. The spectrum analyzer is connected to one output of the output differential stage. Phase noise measurements were carried out by using Agilent E4440A spectrum analyzer.

The measured and simulated tuning range is reported in Fig. 5.2.

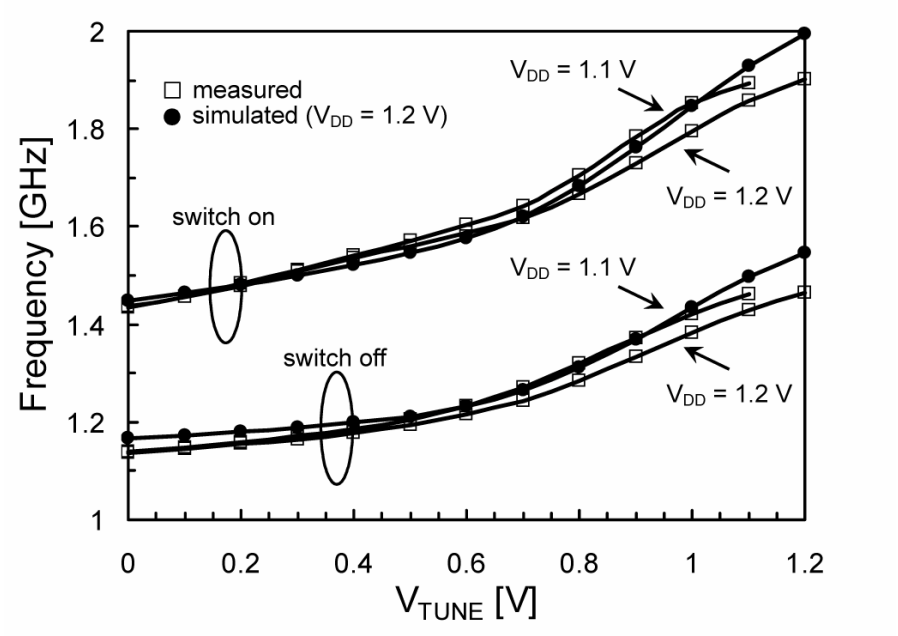

Fig. 5.2. *Simulated and measured VCO tuning range.*

The circuit exhibits a tuning range of 51% from 1.13 GHz to 1.9 GHz with a tuning voltage ideally ranging from 0 to 1.2 V. Simulations show very good agreement with measurements. A small reduction on K_{VCO} can be observed with respect to simulations in the 0.7-1.2V voltage range. Tuning range measurements were also carried out with a 1.1-V power supply. A tuning range reduction as low as 10 MHz was observed in both cases of switch on and off.

The phase noise performance at 100-kHz and 1-MHz offset frequencies over the supported tuning range is reported in Figs. 5.3 and 5.4, respectively.

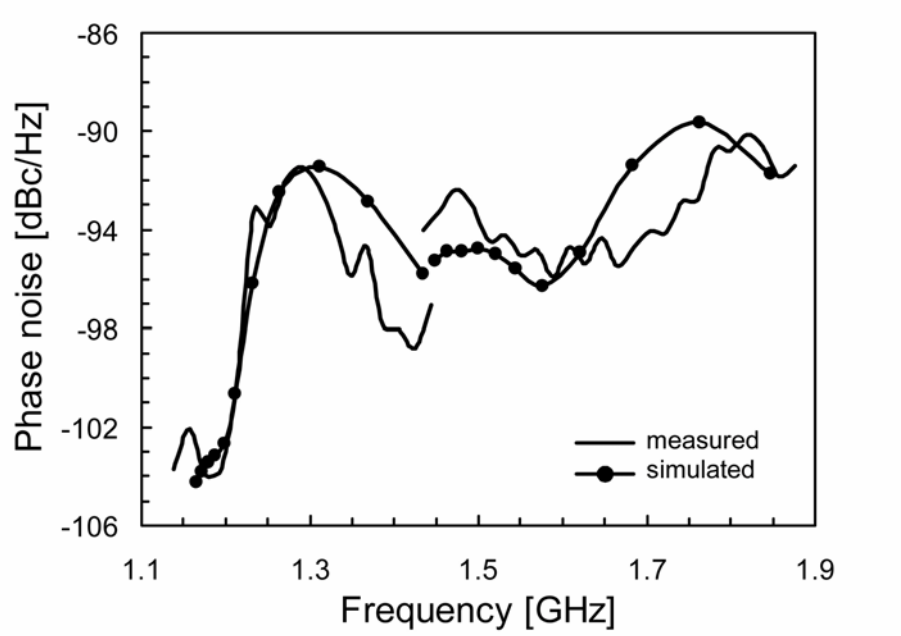

Fig. 5.3. *Simulated and measured phase noise at 100-kHz offset.*

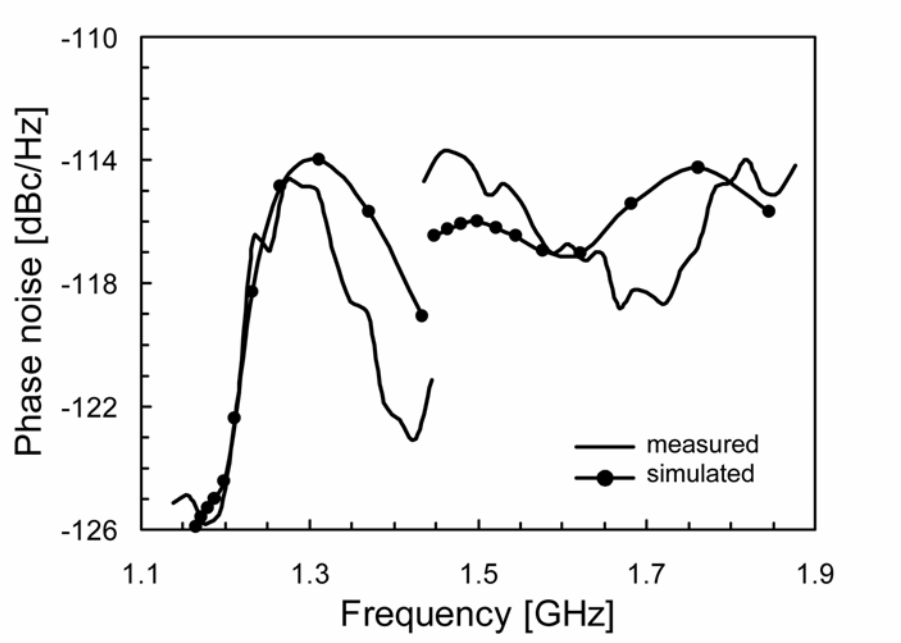

Fig. 5.4. *Simulated and measured phase noise at 1-MHz offset.*

At 100-kHz offset frequency the phase noise is better than −90 dBc/Hz. The best performance of −104 dBc/Hz is achieved with a 1.19-GHz carrier frequency. At 1-MHz offset frequency the phase noise is better than −114 dBc/Hz. Again, the best performance of −126 dBc/Hz is achieved with a 1.19-GHz carrier frequency. Simulated results show an excellent agreement with measurements. The simulated worst phase noise performance in the 1.5-1.9 GHz range is due to the higher simulated K_{VCO}. This result perfectly agrees with the tuning range curves of Fig. 5.2. Moreover, the PLL phase noise contribution is also confirmed negligible.

The worst phase noise performance at lower and higher band is around the same. This means that the design at lower and higher frequency bands was properly balanced by means of an accurate design of switched inductors. Despite phase noise is exacerbated by AM-to-PM effects enhanced by the high varactor gain, the worst phase noise performance of the proposed circuit is

comparable with most of previously reported works [33]-[34] [37] [40]-[41].

The phase noise plot with 1.3-GHz and 1.7-GHz carrier frequencies are reported in Figs. 5.5 and 5.6, respectively. The VCO performance was tested in the 1.1-1.3V power supply range without showing significant variations. The circuit draws a bias current of 0.88 *m*A from a 1.2-V supply voltage.

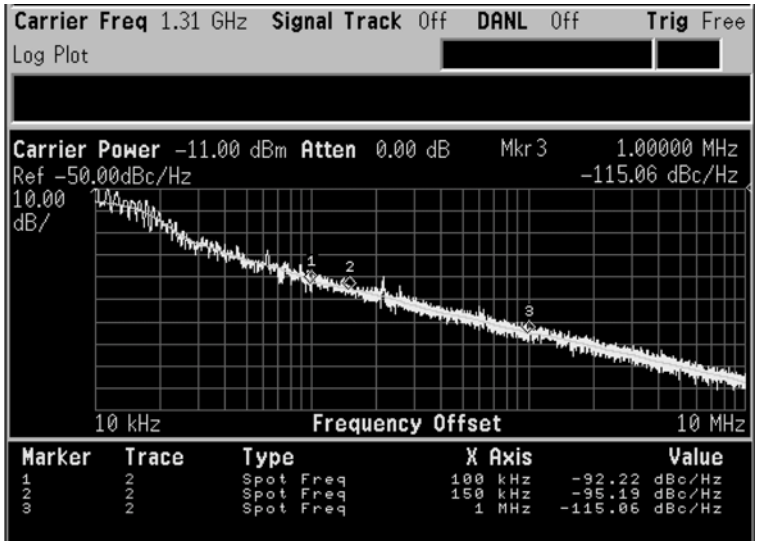

Fig. 5.5. *Phase noise for a 1.3 GHz carrier frequency.*

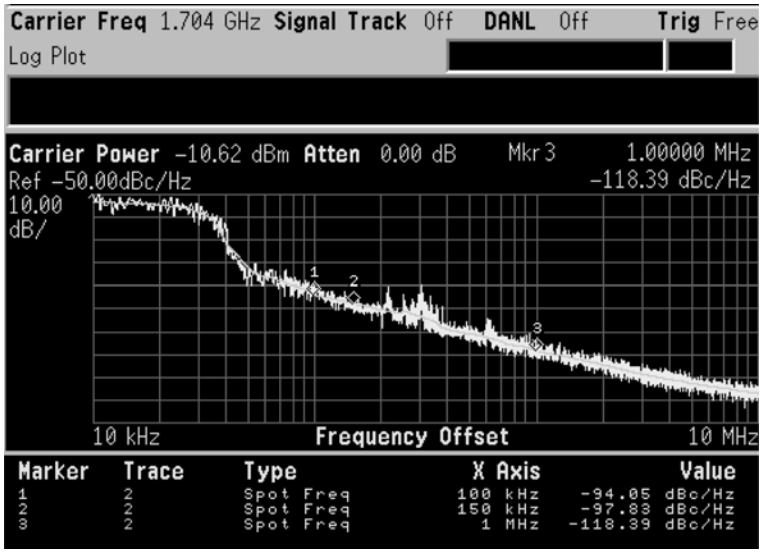

Fig. 5.6. *Phase noise for a 1.7 GHz carrier frequency.*

Table I summarizes the VCO measured results.

TABLE I
VCO MEASUREMENT SUMMARY

Technology	CMOS 90-nm
Supply voltage [V]	1.1 ÷ 1.2
Current consumption [mA]	0.88
Mininum oscillation frequency [GHz]	1.13
Maximum oscillation frequency [GHz]	1.9
Phase noise at 100-kHz offset (1.13-1.9 GHz) [dBc/Hz]	–90 ÷ –104
Phase noise at 1-MHz offset (1.13-1.9 GHz) [dBc/Hz]	–114 ÷ –126
VCO area [mm^2]	0.5

The performance of the proposed circuits is compared with the state-of-the-art wideband VCOs in Table II. To this aim, the power-frequency-tuning-normalized (PFTN) figure of merit (FOM) is used, which was introduced in [42] and defined as

$$PFTN = 10\log\left[\frac{k_B T}{P_{diss}}\left(\frac{f_{\max} - f_{\min}}{\Delta f}\right)^2\right] - L(\Delta f) \tag{5.1}$$

where k_B is the Boltzmann's constant, T is the absolute temperature, P_{diss} is the circuit power consumption, f_{max} and f_{min} are the maximum and minimum oscillation frequencies, respectively, and $L(\Delta f)$ is the phase noise at Δf offset frequency. Despite the very low-power consumption, the VCO achieves an outstanding PFTN of 10. It is worth noting that this performance is provided with a fixed bias current and without any current adjustment [49]. For this

reason, the worst PFTN performance, which is –2.1, is lower than [34]. However, the proposed VCO guarantees a power consumption which is up to six times lower than the mentioned implementations.

TABLE II
VCO PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE ART

Ref.	Technology	Supply voltage [V]	Current consumption [mA]	Tuning voltage [V]	Tuning range [GHz]	Phase noise (1-MHz) [dBc/Hz]	PFTN
[33]	SOI CMOS 130-nm	1	2 ÷ 3	0 ÷ 1.4	3.06 ÷ 5.61 (59%)	–114.6 ÷ –120.8	5.9 ÷ 10.3
[34]	CMOS 180-nm	1.5	1.67 ÷ 6.67	0 ÷ 1.5	1.14 ÷ 2.46 (73%)	–126.5	5 ÷ 8.5
[37]	CMOS 130-nm	1	1 ÷ 8	0 ÷ 1	3.4 ÷ 7 (69%)	–101 ÷ –119	–9.7 ÷ 14.8
[40]	CMOS 90-nm	1.2	6 ÷ 20	-	3.2 ÷ 6.4 (66%)	–104 ÷ –115	–15.9 ÷ –4.7
[41]	CMOS 130-nm	1.5	2.9 ÷ 6.1	1.5	1.3 ÷ 6 (129%)	–112 ÷ –120	4 ÷ 13.5
[42]	CMOS 250-nm	1.8	1 ÷ 10	0 ÷ 4	1.94 ÷ 2.55 / 3.6 ÷ 4.8 (51%)	–116 ÷ –122	–4.6 ÷ –1.5
This work	CMOS 90-nm	1.2	0.88	0 ÷ 1.2	1.13 ÷ 1.9 (51%)	–114 ÷ –126	–2 ÷ 10

5.2 I/Q generator experimental characterization

The measurements were performed using a software, which was properly developed within LabView, using a PC to drive the I/Q generators and the measurement instrumentations, i.e. a Vector Signal Generator and an Oscilloscope. An on-chip double-balanced Gilbert-type mixer was adopted to accurately measure the I/Q phase error as shown in Fig. 5.7.

A phase-modulated low-frequency sine waveform is produced at the mixer output by selecting I or Q as mixer LO signal. The selection is performed by means of the enable bit *E* that controls digital tri-state buffers and inverters. The difference between the phase of the sine waveforms at the mixer output produced by selecting I and Q provides the I/Q generator phase

measurements, which are only affected by the mismatches of tri-state buffers and inverters.

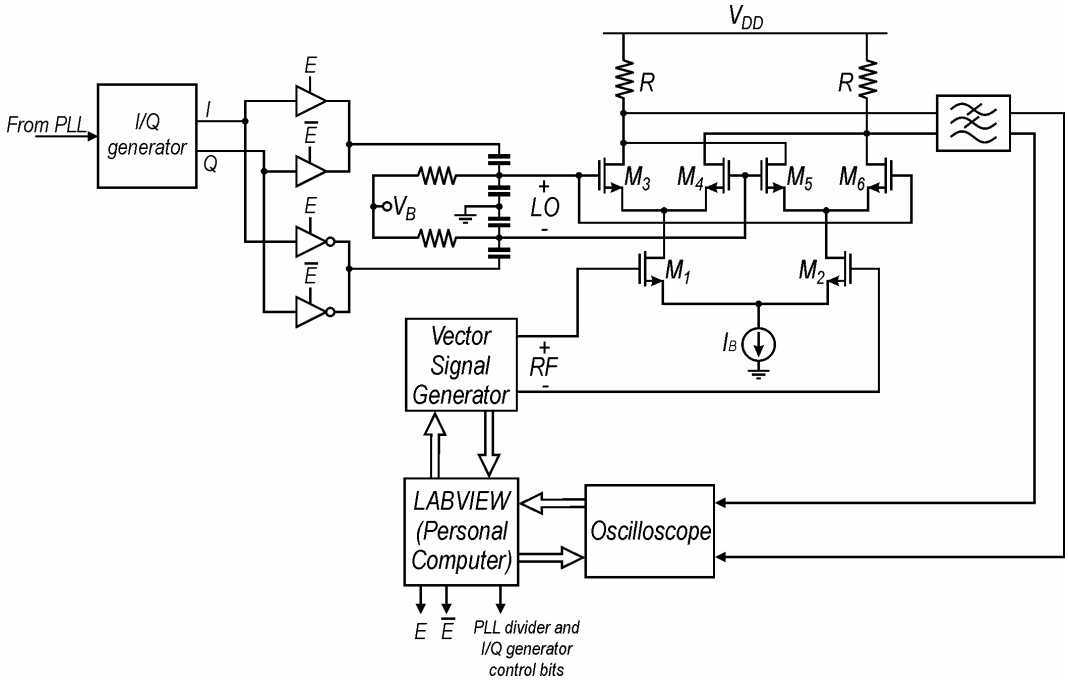

Fig. 5.7. *Test circuit setup.*

Extensive measurements were carried out on several chip samples. The measured phase difference of the I/Q signals at center frequency of the two transceiver operating bands (i.e., 300-470 MHz and 780-960 MHz) before digital calibration is shown in Fig. 5.8 for 40 chip samples. The compensation performed by the DLLs makes the absolute error lower than 2° from a maximum open-loop simulated error of about 12°.

It is worth mentioning that, given the 1.2-1.9 GHz VCO tuning range, the I/Q generator is able to provide also the 600-780 MHz band, although this band was not employed in the proposed transceiver.

Fig. 5.9 and Fig. 5.10 show the I/Q phase as a function of the signal frequency for the lower and higher bands, respectively, and for three power supply values.

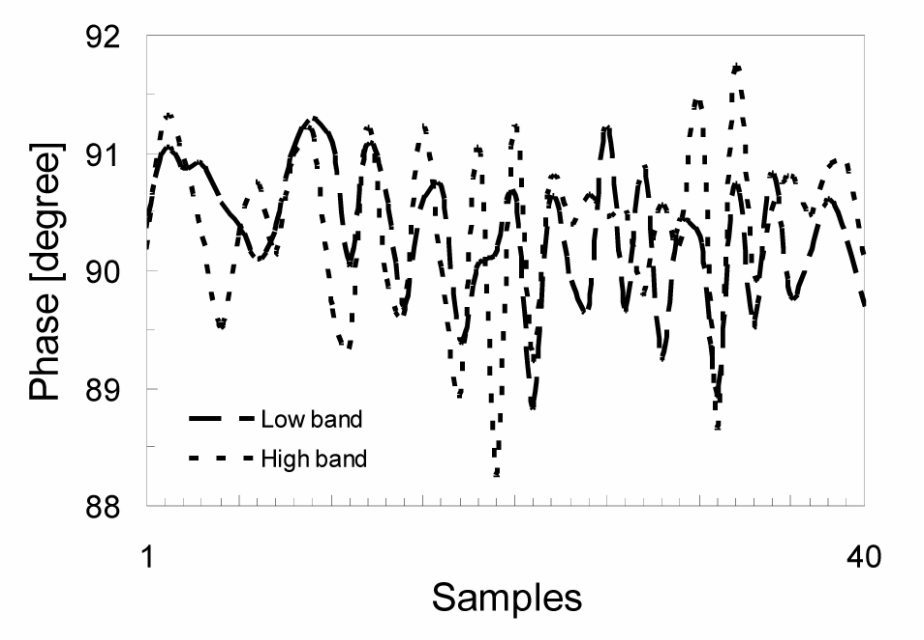

Fig. 5.8. *I/Q phase for 40 chip samples at 390 MHz (low band) and 870 MHz (high band).*

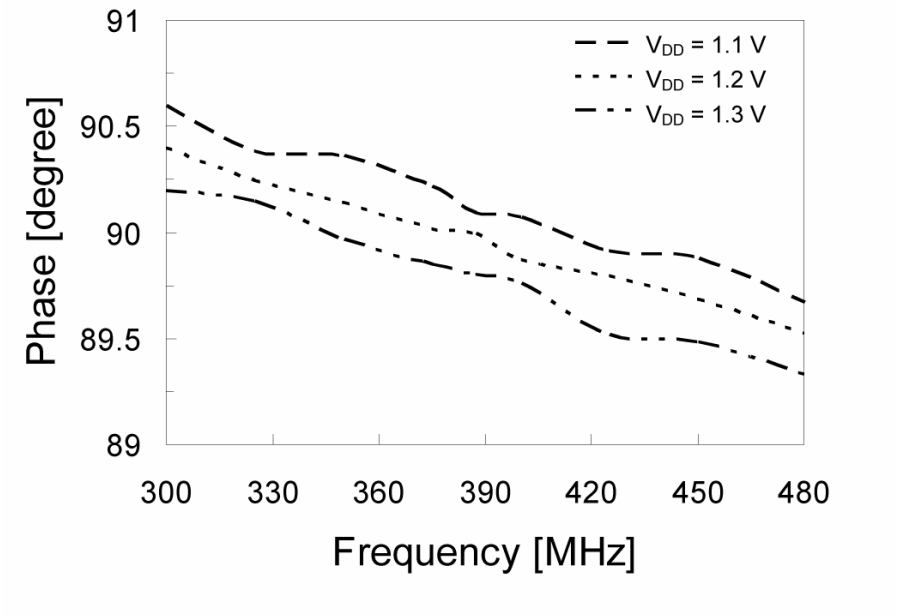

Fig. 5.9. *I/Q phase vs. operating frequency in lower band.*

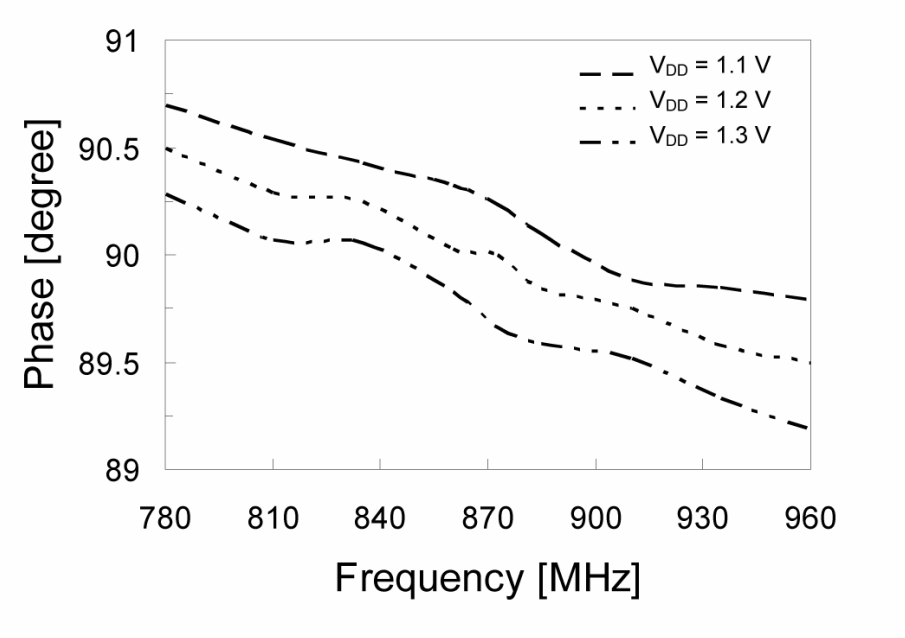

Fig. 5.10. *I/Q phase vs. operating frequency in higher band.*

Figs. 5.9 and Fig. 5.10 demonstrate that by setting the DAC word that cancels the phase error at the center frequency of each band, the phase error within both bands is kept lower than 0.5°. The estimation of this two calibration digital words can be done during manufacturing.

Figs. 5.9 and 5.10 also show the error induced by the power supply variation, which manly affects the time response of the phase detector circuit. The phase error is kept as low as 0.2° for a power supply variation from 1.1 to 1.3 V, which is a typical constrain for a voltage regulator drift.

The performance of the I/Q generator with respect to the temperature variation from –40° to 85°C is depicted in Fig. 5.11 and shows a phase error variation as low as 0.3°.

Therefore, the overall I/Q phase error is lower than 1° for all the operating frequencies taking into account temperature and power supply variations provided that two calibration digital words are set at nominal operating conditions (i.e., 27°C and 1.2 V) during manufacture test.

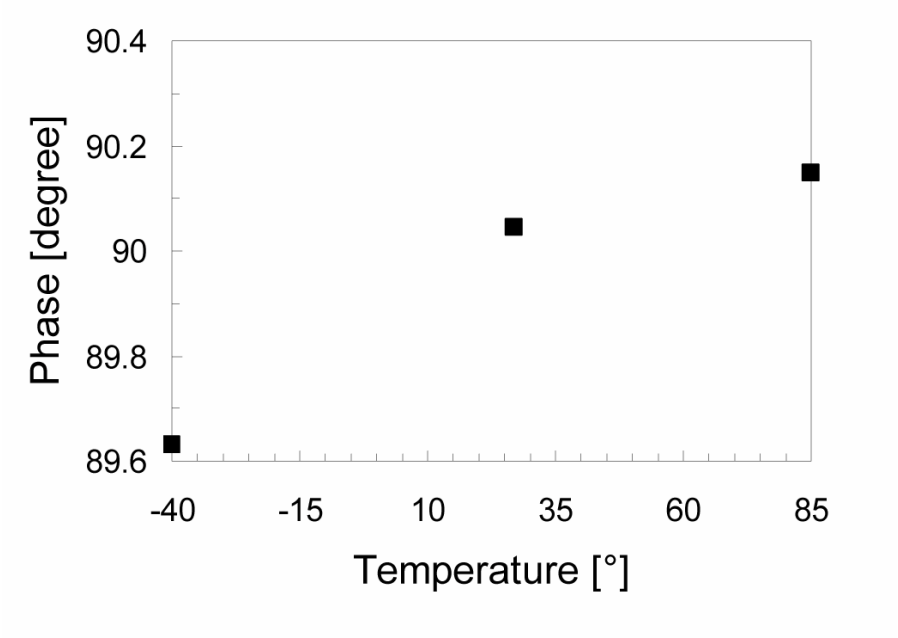

Fig. 5.11. *I/Q phase vs. temperature for 3 samples at 870 MHz.*

Finally, to show the correction capability of the I/Q generator by digital calibration, the phase difference at 870 MHz as a function of the 5-bit DAC control word is plotted in Fig. 5.12.

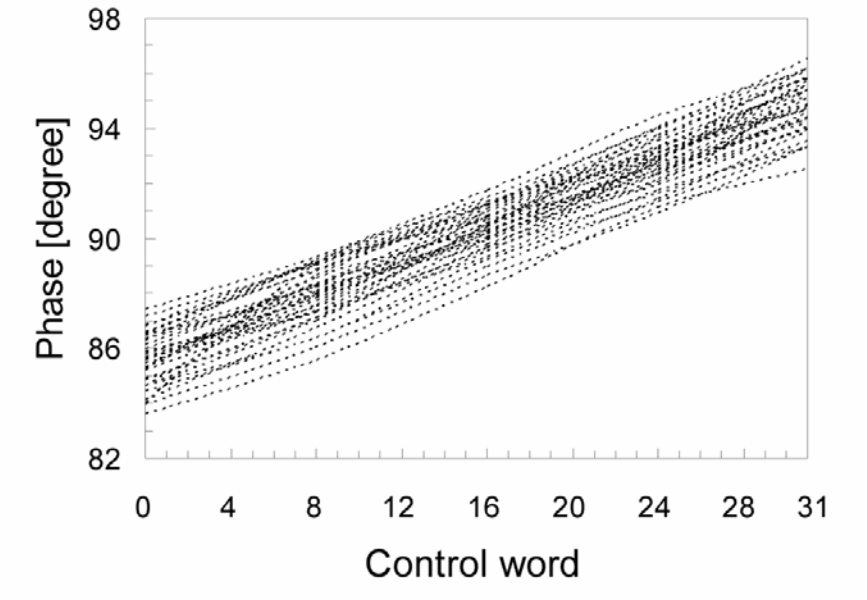

Fig. 5.12. *I/Q phase vs. DAC word for 40 chip samples at 870 MHz.*

The I/Q generator exhibits a phase correction capability of 4.5° with a resolution of 0.3°, which allows compensation of both its phase error and an additional phase error of about 2.5° due to the receiver circuitry. Of course, the digital correction capability can be further enhanced by increasing the DAC bit number in case of higher phase errors in the receiver circuits.

Table III shows a performance comparison among the proposed I/Q generator and some of the most significant previous published solutions.

TABLE III
I/Q GENERATOR PERFORMANCE AND COMPARISON WITH LITERATURE

Ref.	Technology	Supply voltage [V]	Current consumption [mA]	Operating frequency [GHz]	I/Q phase variation [°]				Auto-calibrated generator
					statistical measures	versus frequency	versus temperature	versus supply	
[54]	BiCMOS 0.25-μm	2.5	5	2.4÷2.5 5.15÷5.85	-	< 2 < 2	-	-	yes
[57]	BiCMOS 1-μm	3	2.6	0.04÷0.5	-	< 0.5	-	-	yes
[62]	CMOS 0.18-μm	1.8	10 [a]	1.7÷2.035	< 0.6	-	-	-	no
[64]	BiCMOS 0.25-μm	3	5	2.65÷2.75	< 0.7	-	-	-	no
[66]	Bipolar	3	8	0.4÷0.7	-	< 1	-	-	yes
This work	CMOS 90-nm	1.2	0.5	0.3÷0.47 0.78÷0.96	< 1.3 < 1.8	< 0.5 [b]	0.3 [c]	0.2 [d]	yes

a. including QVCO
b. estimating two calibration words within the operating band
c. temperature variation from –40 to 85 °C
d. supply variation from 1.1 to 1.3 V

The measurements versus both temperature and power supply variations are usually not reported. In some cases the problem in not faced at all, in other cases it can be implied that temperature and power supply effects are compensated by (on field) calibration [54] [56] [57] [65]-[68]. Moreover, only few papers provide statistical measurements. Specifically, [62] and [64] show a better phase statistical error but at the cost of a current consumption that is 10 and 20 times higher, respectively, than that of the proposed solution. Of course, increasing current greatly reduces the impact of process mismatches

and hence the quadrature phase error, but such a high current consumption cannot meet the requirements of WSN applications. [62] and [64] do not report the error versus frequency. Finally, the proposed circuit is the only solution that allows very simple calibration to be achieved during manufacture testing with only two 5-bit digital words while providing temperature and power supply stability.

5.3 Frequency synthesizer performance

The block diagram of the frequency synthesizer is shown following

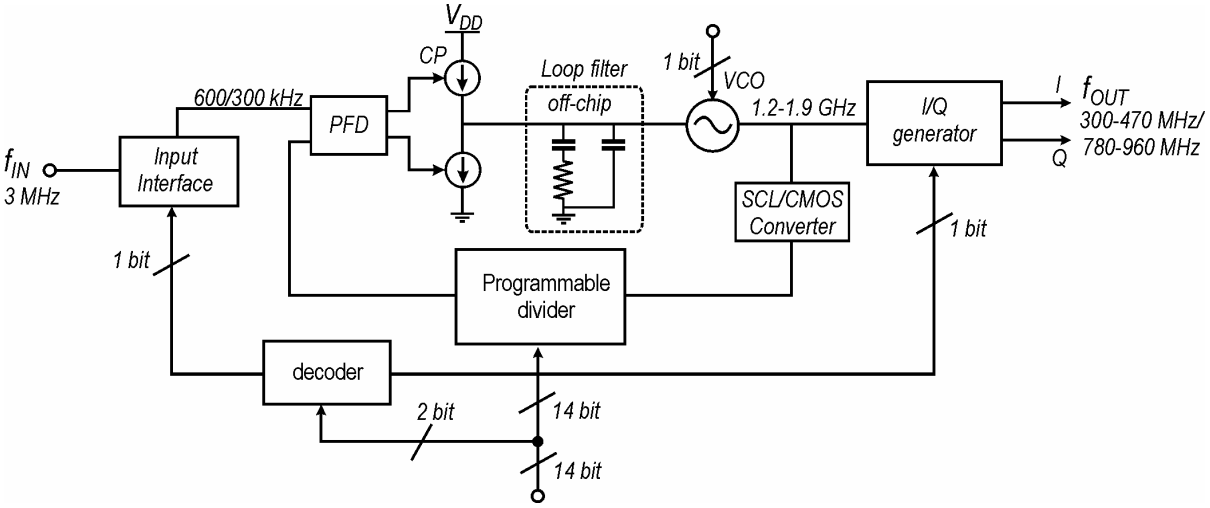

Fig. 5.13. *Frequency synthesizer block diagram.*

As explained in chapter 3 the VCO provides two sub-bands, which are the 1.2-1.5 GHz and the 1.5-1.9 GHz. The operating LO bands are obtained dividing the VCO output by means of the I/Q generator, which was inserted out of the PLL loop. The 300-470 MHz band is obtained dividing by 4 both VCO bands, whereas the 780-960 MHz band is obtained dividing by 2 the VCO higher band. The PLL reference is 600-kHz in case of 300-470 MHz band, whereas is 300-kHz in case of 780-960 MHz band.

Fig. 5.14 shows the measured PLL phase noise at 300-kHz offset frequency as a function of the VCO output frequency. The phase noise is better than –97 dBc/Hz for all the supported channels. Considering the division by-2 or by-4 performed by the I/Q generator, the phase noise of the LO signal is 6 dB or 12 dB better. As a consequence, the phase noise targeted by the transceiver specifications at 300-kHz offset frequency (see chapter 2) is achieved.

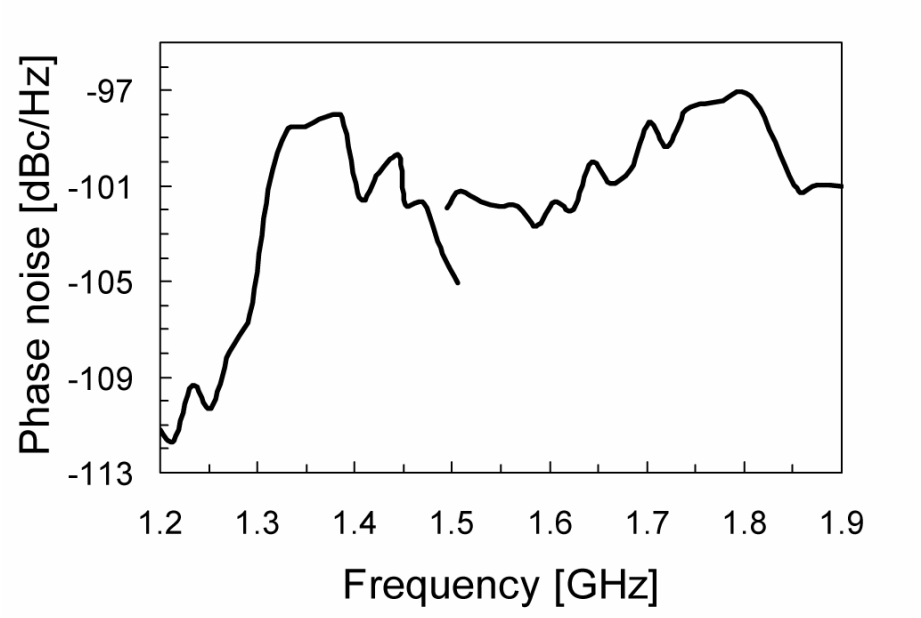

Fig. 5.14. *PLL phase noise vs. VCO carrier frequency (300-kHz offset frequency).*

Fig. 5.15 shows the measured PLL spur rejection at the VCO output. The PLL spurs are lower than –48 dBc in the 780-960 MHz band, in which the PLL reference is 300-kHz. On the other hand, in the 300-470 MHz band, in which the PLL reference is 600-kHz, a spur rejection improvement of 10-15 dB was measured.

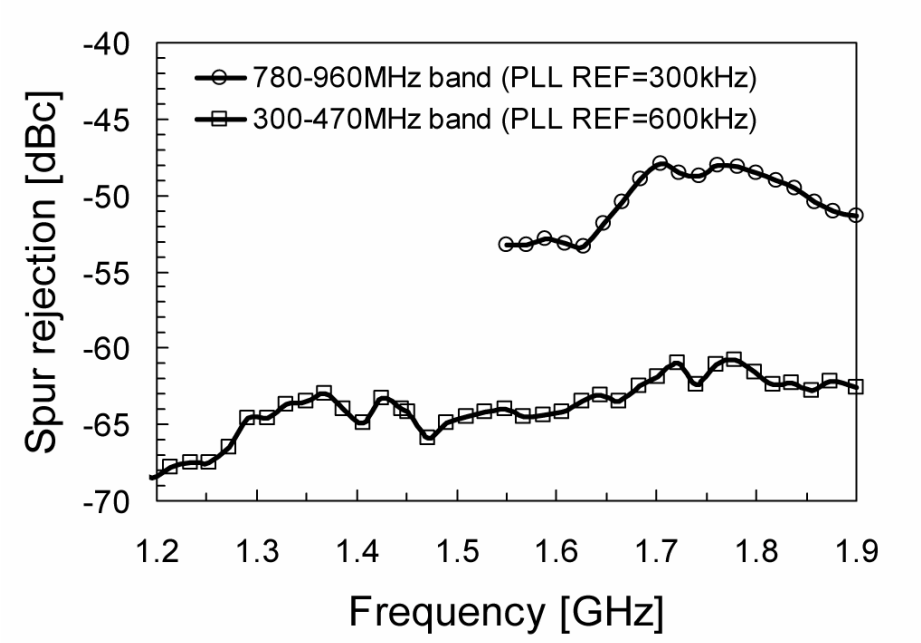

Fig. 5.15. *Spur rejection.*

The settling behavior of the PLL was characterized switching periodically the reference frequency. Fig. 5.16 shows the VCO control voltage during the loop settling for a 50-MHz frequency step of the output signal. Fig. 5.16 also reports the estimated channel frequency deviation during the settling, which is defined as the absolute value of the difference between the LO target frequency and the actual LO frequency normalized with respect to the channel bandwidth (i.e., 200 kHz). Setting a channel frequency deviation of 20%, the settling time is around 350 μS.

As shown in Fig. 5.17, the PLL guarantees a settling time lower than 400 μS for all the supported channels.

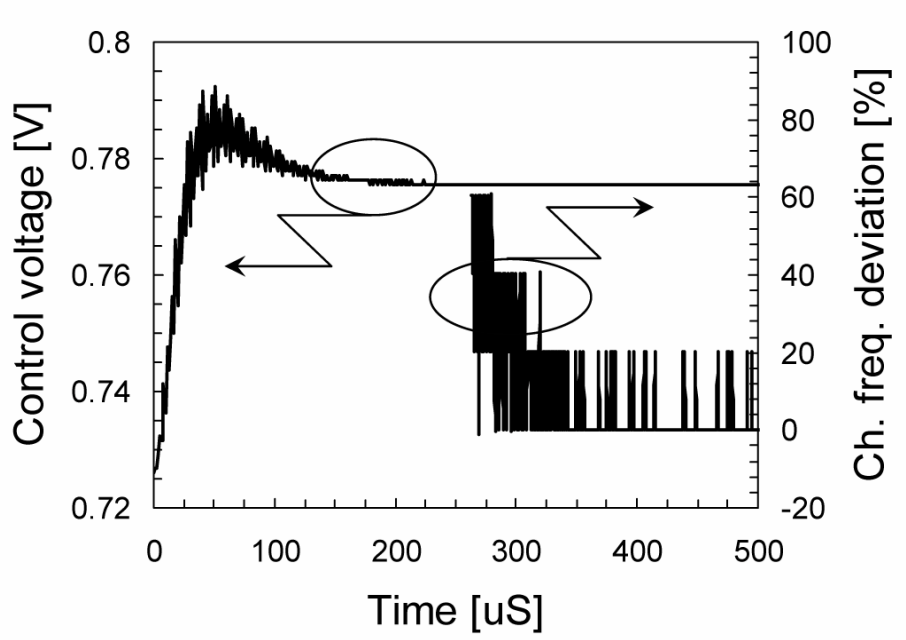

Fig. 5.16. *Settling time (VCO frequency = 1.644 GHz, 50 MHz output step).*

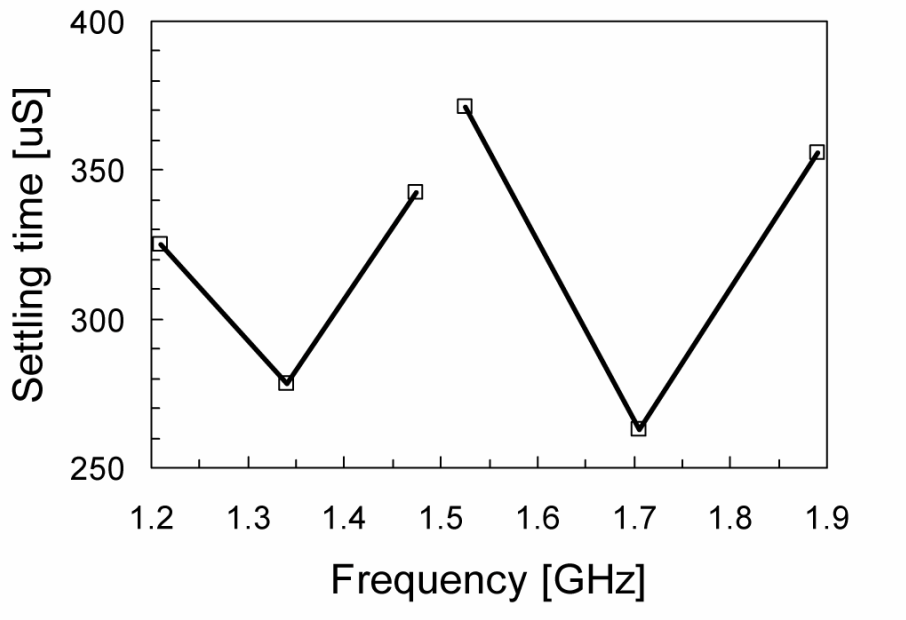

Fig. 5.17. *Settling time vs. VCO carrier frequency.*

The PLL and the I/Q generator draw 1.3 mA and 0.5 mA, respectively, from a 1.2-V supply. The VCO core is the most power-hungry part of the PLL drawing 0.9 mA.

Table IV summarizes the frequency synthesizer measured performance in the two bands of interest, thus demonstrating the agreement with the transceiver specifications drawn in chapter 2.

TABLE IV
SUMMARY OF THE FREQUENCY SYNTHESIZER
MEASURED PERFORMANCE

Technology	CMOS 90-*n*m
Frequency	300-470 MHz / 780-960 MHz
RF Channel spacing	150 kHz
Phase noise	< –103 dBc/Hz (300-kHz offset freq.)
LO quadrature phase error (after digital adjustment)	< 1°
Spurious rejection	< 48 dBc
Settling time	< 400 μS
Supply voltage	1.2 V
Current consumption	1.8 mA

Conclusions

This thesis has presented a CMOS frequency synthesizer usable for low data-rate sub-GHz transceivers. The proposed frequency synthesizer generates highly-accurate quadrature signals in the 300-470 MHz and 780-960 MHz bands, thus covering the operating frequencies mainly used for Wireless Sensor Network applications.

Excellent performance in terms of phase noise, spur rejection, and quadrature accuracy are achieved while ensuring low-power consumption and wideband operation. These results have been obtained thanks to both proper design and innovative circuit topologies. In particular, novel solutions have been proposed for the most critical circuits of the frequency synthesizer, i.e. the Voltage Controlled Oscillator and the I/Q signals generator.

The Voltage Controlled Oscillator exploits an innovative integrated LC tank based on shunt-connected switched-coupled inductors and a proper varactors configuration.

The quadrature generator employs a novel feedback technique based on phase-tunable circuits to control the I/Q signals phase. The generator ensures a phase error as low as 1° considering process, temperature, power supply, and operating frequency variations, by only performing a digital calibration during the manufacture testing.

Finally, the experimental results demonstrate the suitableness of the proposed frequency synthesizer for high-performance and high-flexibility direct conversion or low-IF transceivers for Wireless Sensor Network applications.

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Journal

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Patent

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