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GIORGIO MAIELLARO

ANALOG AND DIGITAL CIRCUITS IN A COMPLEMENTARY ORGANIC TFT TECHNOLOGY ON FLEXIBLE SUBSTRATE

PH.D. THESIS

TUTOR:
PROF. G. PALMISANO
COORDINATOR:
PROF. L. FORTUNA

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Giorgio Maiellaro

Publications

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Abstract

During the last decades, organic semiconductor technology on flexible substrate is attracting the interest of both academia and industrial communities since it is considered a very promising alternative to silicon technology in those applications where low cost, flexibility, and capability to cover large surfaces are required. The great advantage of organic thin-film transistor (OTFT) technology is the direct fabrication of circuits on low-cost plastic foils by using both low processing temperatures and printing methods that guarantee cost-efficient production. Several applications were faced by using OTFTs, such as flexible displays, RFID tags and organic processors. Such technologies also allow the integration on the same substrate of different kinds of organic sensors (i.e., light, temperature, pressure, humidity, pH, biosensors, etc.) in order to implement fully-integrated flexible organic smart sensors.

Despite these interesting developments, most OTFT processes still feature only p-type transistors, while very few complementary OTFT (C-OTFT) platforms have been

developed. Of course, the availability of a reliable process flow featuring both p-type and n-type transistors is now of utmost importance to advance in industrial applications development. Indeed, complementary organic technology would allow the implementation of complex digital circuits with higher yield and lower current consumption, as well as an increased reliability in mixed analog/digital circuits.

Research efforts on organic electronics have been mainly addressed towards digital circuits, while there is still a serious lack of significant results in the analog field. This lacuna hampers the advance towards the implementation of fully-integrated mixed-signal organic systems, including analog front-ends, signal conditioning, and/or analog-to-digital conversion (i.e., RFIDs, smart sensors, etc.).

In this thesis work analog and digital basic building blocks (i.e., inverters, static and dynamic logic gates, static and dynamic flip-flops, ring oscillator, differential gain stage, and rectifier/envelope detector) fabricated using a fully-printed organic complementary technology on flexible substrate are presented. The performance of the rectifier/envelope detector are explored up to 13.56-MHz thus demonstrating that adopted technology is suitable for the implementation of a flexible organic RFID tag.

Moreover, design of complex analog building blocks (i.e. folded-cascode transconductance amplifier, 2-stage OTA, stacked-mirror OTA and switched-capacitor comparator) are also faced since the research on complementary organic analog circuits is still at very beginning and they are essential for enabling the implementation of fully-integrated mixed-signal systems (i.e., smart sensor interfaces, wireless communication systems, etc.). The measured performance of the single-stage folded-cascode transconductance amplifier is the best-in-class for complementary OTFT technologies on flexible substrate.

Finally, design and experimental results of the first fully-integrated flexible organic light sensor are also presented.

Chapter 1

1.1 Introduction

Organic electronics is an emerging technology field that is attracting the interest of both academia and industrial communities. Recent advances in organic electronics open new perspectives on developing much cheaper technologies for manufacturing electronic circuits and systems. Key to these new developments is the performance of organic thin-film transistors. Organic technology cannot achieve the performance of the silicon-based technologies in a relatively short time but it is expected to become suitable for designing complex electronic circuits and systems. Many researchers and companies are focused on development of new technologies, circuits and complex systems based on organic materials.

Organic semiconductor technology is expected to be able to create innovative applications and it is considered to be a new class of electronics with a huge market potential.

The processing characteristics and performance of FOLAE (Flexible Organic Large-Area Electronics) technology so far

show that it can be used for exiting or novel applications requiring large-area coverage, flexibility, and low temperature processing and low manufacturing cost. Moreover, large-area organic electronics will become “invisible”. Thanks to all these characteristics the new products could be integrated in most of daily live consumer goods, such us clothing, cars, houses, packaging and many others.

According to a study conducted by the US marketing research institute IDTechEx in 2006, the global market for organic and printed electronics will grow from its current 1.18 billion US dollars to more than 40 times that, to a volume of 48.18 billion US dollars, within the next 10 years [1].

A long-term market evaluation is difficult to do for an emerging technology but this preliminary forecast of the market share clearly indicates a strongly positive trend for FOLAE technology, in particular for logic and memory segment.

The logic segment covers all the applications of electronic circuits made on flexible substrate by printing or printing like processes. The segment named “Plastic Electronics” includes high-volume markets such as: large-area sensing applications, Radio Frequency IDentification and intelligent tags, electronics circuits for entertainment and games.

The ability to integrate on the same organic substrate all the functionalities needed to realize a complex system is the differentiating advantage of flexible organic and large area electronics that will create new applications and markets. In the last decade several basic functionalities, such as backplane matrices, displays, light emission and detection, sensing, energy storage and circuits for RF-ID, etc., have been realized. However, electronic circuits needed to integrate complete systems are so complex that a hybrid implementation with silicon-based technologies is still required.

A first revolution in the flexible organic large area electronic field was brought around 2006 by the chemical companies which have developed and commercialized air stable p-type organic semiconductors. Based on these materials, mature technologies are suitable for display backplane matrices and to drive a specific actuator for example in flexible Braille displays [2].

Except for these specific applications, p-type only circuits show strong limitations in performance: intrinsic high operating voltages and low switching speeds; low noise margin and sensitivity to variability, hence low yield and no possibility to build circuits with complex functionality. These major drawbacks of p-type only circuits limit the possible

applications of organic large area electronics to low complexity digital circuits.

A new revolution for the organic technology is needed in order to make the ambitious market forecast became a reality. The complementary organic technology, also named “organic CMOS technology” is the key point for developing all applications that nowadays the p-type only technology does not permit. Indeed, organic CMOS technology will allow to reach higher complexity digital circuits with substantial high yield and at low operating voltage and will also allow the integration of analogue circuits that are required to address many of the potential electronics applications like sensors, actuators and radio frequency communication systems.

In the recent years, chemical companies such as POLYERA, BASF and many others, brought to the market the first generation of n-type organic semiconductors that are printable and air-stable, enabling the development of the complementary organic technology.

Scientific community must, however, still overcome huge technical challenges in order to develop a stable and reliable organic CMOS technology that could be transferred to industry environment and enable the new applications.

1.2 Research background

Organic TFTs have seen a large research and development effort in the past ten years as they can be processed at ambient temperature, starting from the soluble, ink-like materials. The reduced temperature budget and the thin-film approach enable:

- To manufacture electronics on basically any substrate, for instance flexible plastic films, making it possible to integrate electronics on cheap flexible surfaces.
- To cover large surfaces with electronics at an extremely low cost per unit area using simple and high throughput technologies like printing.

Research on organic electronics by many industrial and academic research groups focused on application like flexible displays [3], low cost identification tags or RF-ID tags [4], photovoltaic surfaces and cells [5], sensors [6], etc. Some of these efforts are now leading to real product, like roll-up displays (Polymer Vision) [7] and low-end radio frequency identification tags [8].

The advancement in the field of the organic semiconductor materials have been impressive [9], with state-of-the-art solution-processed p-type materials reaching mobility in order

of 1 [cm^2/V s] [10] and vacuum deposited p-type materials reaching 40 [cm^2/V s] [11].

Most of organic semiconductor investigated until now are p-type materials. N-type materials have received quite some attention in the last few years, with recent reports on high mobility (up to 0.85 [cm^2/V s]), printable and air-stable polymers [12] and air-stable oligomers [13].

The availability of p-type and n-type materials enables the development of technologies integrating complementary organic thin film transistors (BASF and POLYERA and other companies brought to the market the first generation of n-type organic semiconductor).

As for silicon technology, the availability of a technology which integrates complementary organic transistors allows:

- To design digital circuits with higher complexity (thanks to the higher noise margin) being much more robust to process and aging variations (>10000 OTFTs), which can be used in display drivers and microcontrollers.
- To produce low-consumption and low operating voltage logic (<5V) as demonstrate in [14] compatible with existing electronics and energy sources.
- To improve switching speed in digital circuits (0.1 – 0.25 μs).

- To design reliable analogue building blocks such as operational amplifiers, comparators, peak detectors and filtering stage that can be used for designing a more complex mixed-signal systems like A/D converter that enables the integration of electronics interface for sensors using the same organic technology.
- A further cost reduction by a higher level of integration; Si-based logic could be replaced by organic CMOS for some applications.
- Improved device performance (increased flexibility, robustness, etc.)

The better performance of complementary organic technology was already demonstrated in 2000 [15]. However, most efforts till now in complementary organic thin-film transistor technology have been concentrating on laboratory scale, shadow-mask based processed [16]. Only in recent year inkjet and potentially high-throughput printing techniques like roll-to-roll, gravure and flexo have been experimented to fabricate p-type and complementary organic thin-film transistors. [12] [17].

The chance to have a robust, reproducible and full-printing process flows for organic CMOS circuits have a strategic importance for the development of the meaningful industrial applications.

Nowadays it is possible to integrate digital circuits based on p-type only transistors at a complexity level of more than 1000 gates with reasonable yield; the organic CMOS technology can be able to increase the complexity by at least a factor of 10 enabling a relevant applications.

On the other hand, the progress in the field of analogue circuits and systems has been limited until now. This is mainly due to the heavy constrains posed by the state-of-the-art organic technology to the design analogue circuits:

- The lack of complementary transistors.
- Insufficient modeling for analogue purposes (i.e., accuracy, scaling, continuity and derivability of the simulated characteristics).
- Immature characterization and modeling of transistor variability and noise mechanisms.

1.3 Key applications

The key applications of organic semiconductor technology can be grouped in three major application areas:

1. Flat panel displays based on liquid crystal pixels
2. Low-end smart card and electronic identification tags
3. Sensors.

1.3.1 Low-end smart cards and electronic identification tags

The performance of OTFTs in terms of field-effect mobility, threshold voltage, operating voltage and yield are still limited respect to those of silicon-based counterparts (MOSFETs). However, the performance of the current organic semiconductor technology is sufficient to develop low-cost applications that require a limited switching speed such as intelligent ticket, card games and product packaging.

An integrated radio frequency identification (RFID) tag, which normally operates at 13.56 MHz, becomes a promising candidate for organic electronics. RFID tags are typically used in smart cards, tickets, library book labels, passport, laundry tags and many other applications.

The effective cost of organic RFID tags realized using a solution processing could be low enough to be competitive with that of bar codes while providing a lot of advantages offered by silicon-based version. Besides, making the organic RFID tag on plastic substrate it will be more flexible and thinner than those based on silicon.

Pentacene-based RFID circuits were presented by Baude et al. in 2003 [18]. The RFID circuits, without a rectification stage, were powered directly by RF and operated at 125 KHz.

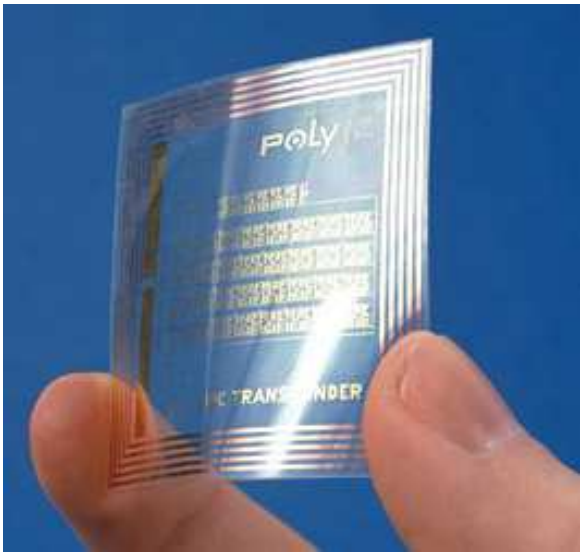

Fig.1.1. Flexible RFID tag fabricated by PolyIC.

In 2004, Subramanian et al. reported 135 KHz all-printed organic RFID tags using novel pentacene and oligothiophene precursors for p-type semiconductors and ZnO nanoparticles for the n-type semiconductor [19]. The first working 4-bit transponder based on organic complementary metal-oxide-semiconductor (CMOS) operating at carrier frequency of 13.56MHz was published by Blache et al. in 2009 [20]. The devices were fabricated on flexible polyester substrate and all the active layers of the device consisted of soluble organic molecules deposited by spin coating.

1.3.2 Sensors

A very important trend recently emerged in organic electronics is the development of sensors which can be used for food and environmental monitoring, intelligent lighting and bandage, medical diagnostics and home security as well.

Organic semiconductor offer many advantages in comparison with their inorganic counterparts, which make them particularly attractive for sensor applications. First, organic sensors can be manufactured at room temperature on flexible substrate with large-area coverage and using low-cost processes, an important attribute for disposable sensors and artificial skin. Second, their properties can be tuned by means of chemical synthesis.

A ion-selective (IS) FETs for pH monitoring using proton sensitive OTFT as a transducer was published by Bartic et al. in 2002 [21]. In 2004, Someya et al. reported a large-area flexible pressure sensor suitable for electronic artificial skin with organic transistors [22]. The organic transistors, which were integrated with a graphite-containing rubber pressure sensor layer form a very wide area structure, were used to realize a flexible AM, which was used to read out pressure image from the sensors. The device was electrically functional when it was wrapped around a cylindrical bar with a 2 mm radius. The chance to integrate OTFTs for chemical and

biological sensors, capable of detecting parts per billion anyalyte concentrations in water was demonstrated by Roberts et al. in 2008 [23]. Organic thin-film transistors, based on a thin, cross-linked gate dielectric and stable organic semiconductor, could be able to detect changes in pH and low concentrations of chemicals, i.e., trinitrobenzene, cysteine, methylphosphonic acid and glucose in water.

In order to exploit this new application domain advance the state-of-the-art of analogue circuits is needed. Indeed, analogue circuits are the basic building blocks for designing sensor interface, i.e., A/D converter. In this scenario, the availability of robust and reliable organic CMOS technology plays a crucial role for realizing the integration of a complete system, i.e. sensor and electronic interface on the same flexible substrate.

1.3.3 Flat panel displays

One of the key applications of organic semiconductor technology is the backplane for displays. To date, most backplane of AM LCDs and AM OLED displays are based on TFTs comprising hydrogenate amorphous silicon (a-Si:H) or low temperature poly silicon (LTPS) as the active layer. However, OTFTs (Organic Thin-Film Transistors) has several advantages over structures fabricated from inorganic

semiconductors: flexibility, large-area coverage and low-cost manufacture. These make OTFTs a promising candidate for inexpensive and flexible displays. For example, it is not possible to make AM LCDs based on a-Si:H TFTs on a transparent plastic substrate because of the relatively high processing temperature needed for a-Si:H deposition. However, OTFTs can be processed at room temperature and thus are compatible with flexible substrates. Furthermore, solution-processed OTFTs can enable low-cost large-area manufacturing approaches, such as those based on inkjet-printing and roll-to-roll processing, for large-area AM LCD of TVs.

Fig.1.2. 55-inch flexible OLED display developed by LG Electronics.

The first AM displays based on organic semiconductors was reported in 2000 by Philips Research [24]. In 2001, Rogers et al. reported an electrophoretic flexible display using a backplane based on OTFTs [25]. Following Rogers's report, many research groups have described OTFTs backplane in combination with electrophoretic display media and simple OLED pixels. Hong et al. have also shown the chance of an OTFT backplane with fairly large size and high resolution for AM LCDs in 2005 [26]. OLED TV and e-Book sales revenues may rise up to 140 % to 49 %, each year from 2008 to 2016, respectively [27].

1.4 Objectives of research activity

The content of this work addresses some of the objectives and issues in the field of organic semiconductor technologies that are highlighted by both academia and industrial communities.

In particular, the research activity was characterized by three different phases.

In the first phase, basic devices and test structures, i.e. OTFTs with different lengths, width and layout, inverters, logic gates, ring oscillators, differential gain stage etc., needed

for developing a robust and reliable complementary organic technology process, were designed and measured (Chapter 2).

In the second phase, more complex digital and analogue building blocks which allow the integration of complete systems were developed and tested (Chapter 3).

In the third phase the feasibility of a complete system was further investigated. Indeed, a fully-integrated flexible organic light sensor was designed and tested (Chapter 4).

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Chapter 2

2.1 Organic thin film transistor

The key component of organic electronics is the Organic Thin-Film Transistor (OTFT) that is a Field-Effect Transistor (FET) based on organic semiconductors and dielectrics. Traditionally, silicon has been the most widely used semiconductor material for fabrication of FET.

The interest of organic semiconductor has grown when the field-effect conduction in small organic molecules [1] and conjugated polymers [2] was demonstrated.

The first Organic Field-Effect Transistor (OFET) was reported in 1986 by Tsumara [3]. Since then, huge advances were made in development of new technology processes, materials and organic TFT structures.

The growing interest of industries towards organic electronics is mainly due to the possibility to fabricate OTFTs with very low-cost processes and materials on large-area and on flexible plastic substrate.

Despite in the last years great progress on development of organic TFTs was done, their performance is still lower than

the silicon-based transistor. The main limitations of organic TFTs respect to the silicon counterparts are due to the low charge carrier mobility, high threshold voltage, high supply voltage, low operating frequency, high process mismatch and low yield.

The first organic TFTs were p-type only due to the lack of a stable n-type organic semiconductor. The state-of-the-art solution-processed and vacuum-deposited p-type materials show a charge carrier mobility in the order of 1 [cm^2/V s] and 40 [cm^2/V s] respectively, as reported in [4] and [5].

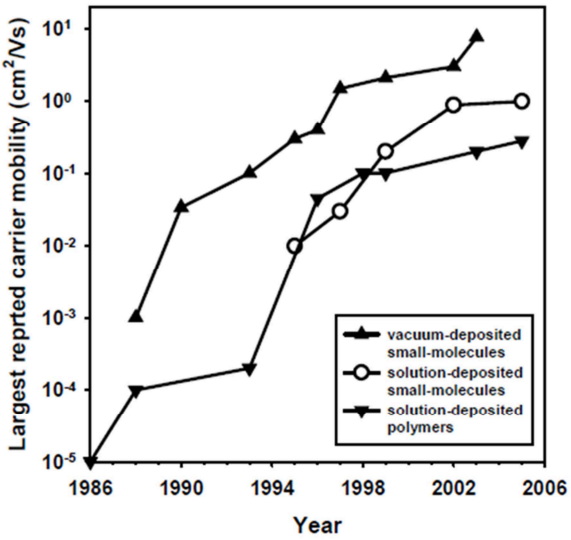


Fig. 2.1. Historic progress in the performance and maximum reported carrier mobility of organic TFTs [6].

In the last few years, a strong research activity was carried out towards the development of air-stable n-type polymers [7] and oligomers [8]. For the n-type semiconductor a charge carrier mobility up to 0.85 [cm^2/V s] was reported [7], [8].

Table 2.1 summarizes the three main parameters to be used when evaluating the performance of organic TFTs.

	[8] 2005		[9] 2012	
	p-type	n-type	p-type	n-type
Mobility [cm^2/V·s]	0.1	0.002	1.5	0.55
I_{ON}/I_{OFF} ratio	10^4	10^3	10^7	$>10^7$
Subthreshold Slope [V/decade]	0.6	1.4	2.4	1.2

Table 2.1. Main parameters of the complementary organic TFTs reported in [9] (2005) and [10] (2012), respectively.

The availability of a robust and reproducible complementary organic technology plays a crucial role for developing new industrial applications. Since, complementary organic technology allows the implementation of complex digital circuits with higher yield and lower current consumption, as well as an increased reliability in mixed analog/digital circuits. Indeed, mixed-signal circuits such as analog to digital converter are crucial to enable the integration of sensor interfaces or wireless communication systems.

2.1.1 Organic TFT operation

Organic field-effect transistor (OFET) is a three terminals device: drain, gate and source and it can be considered as a parallel plate capacitor. A schematic cross-section of OTFT is shown in Fig. 2.2. As can be shown the gate terminal is electrically insulated from semiconductor layer. When a voltage is applied between gate-source terminals (V_{GS}) charge carriers are accumulated at semiconductor/dielectric interface. Typically, organic FET works in accumulation regime rather than in inversion regime.

The drain-source current can flow both in the accumulation layer and in the bulk of semiconductor thanks to the mobile charges induced by doping.

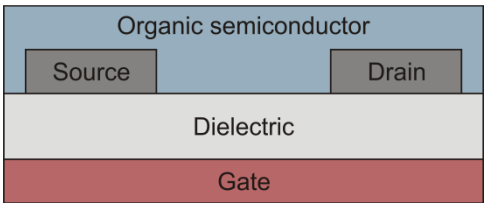


Fig. 2.2. Schematic cross-section of OTFT.

For a better understanding of organic transistor operation it is interesting to analyze the different current contributions at the different transistor operation regimes. For this reason, it is useful to define the meaning of the flat band voltage for a

MOS transistor before to proceed with the above-mentioned analysis.

The flat band voltage (V_{FB}) is the voltage value at which the electric field in the insulator is zero. In this case, the semiconductor energy bands are flat and hence transistor is in thermodynamic equilibrium condition.

As already said above, unlike to silicon MOS transistor, organic TFT works in accumulation region and hence no depletion region and inversion regime have to be created and so the threshold voltage is equal to the flat band voltage:

$$V_{TH} = V_{FB} \tag{2.1}$$

For a p-type OTFT, when $V_G < V_{FB}$, it is in accumulation regime. In this case, the total drain-source current (I_{DS}) is given by the sum of channel current and bulk current, as shown in Fig. 2.3. Moreover, bulk current is a function of drain-source voltage (V_{DS}) and it is independent from the gate-source voltage (V_{GS}). This physical effect limits the maximum achievable gain.

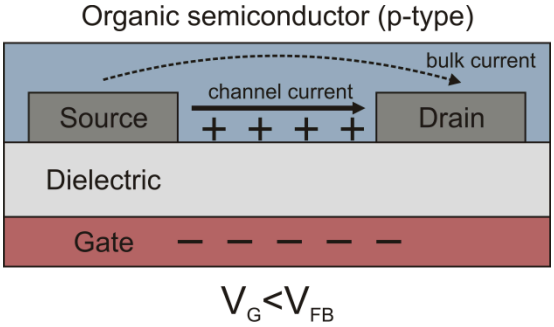


Fig. 2.3. OTFT in accumulation regime; total drain-source current is the sum of channel current and bulk current.

In the transition regime, when $V_G = V_{FB}$, the total drain-source current (I_{DS}) is mainly due to the bulk current, as shown in Fig. 2.4. In this operating condition, the transistor behavior is similar to that of a resistance.

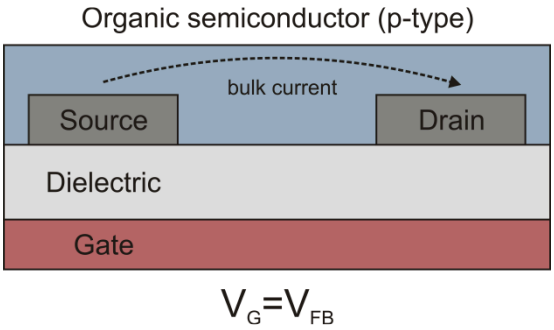


Fig. 2.4. OTFT in transition regime; bulk current represents the main contribution to the total drain-source current.

In the depletion regime, when $V_G > V_{FB}$, the transistor channel region is enhanced by the charge carriers with opposite sign as shown in Fig. 2.5.

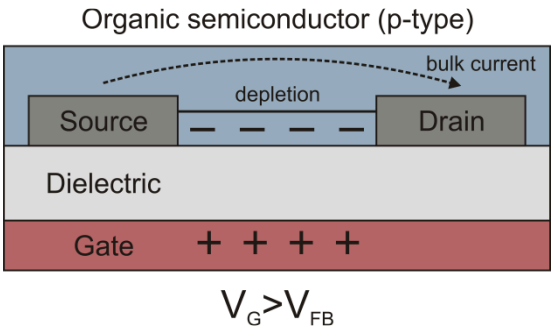


Fig. 2.5. OTFT in depletion regime; the drain-source current typically decreases by increasing the gate-source voltage.

The bulk current continues to flow between source and drain terminals and it decreases by increasing the gate voltage. There will be a gate voltage value for which no charge carriers will be present within semiconductor layer and thus no source-drain current will flow in the organic OTFT.

2.1.2 Electrical characteristic of organic TFT

In the first approximation, the classical characteristic equations of silicon MOS transistor can be used also for OTFT.

For $V_{DS} < (V_{GS}-V_{TH})$ transistor works in linear regime and the drain-source current is given by the following equation:

$$I_{DS(lin)} = \mu C_{OX} \frac{W}{L} \left[V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right] V_{DS} \tag{2.2}$$

Where V_{TH} is the threshold voltage, C_{OX} is the dielectric capacitance per unit area and μ is the charge carrier mobility.

For $V_{DS} > (V_{GS}-V_{TH})$ transistor works in saturation regime and the drain-source current is given by the following equation:

$$I_{DS(sat)} = \frac{1}{2} \mu C_{OX} \frac{W}{L} [V_{GS} - V_{TH}]^2 \tag{2.3}$$

In Fig. 2.6 is shown the typical output characteristics of a p-type OTFT.

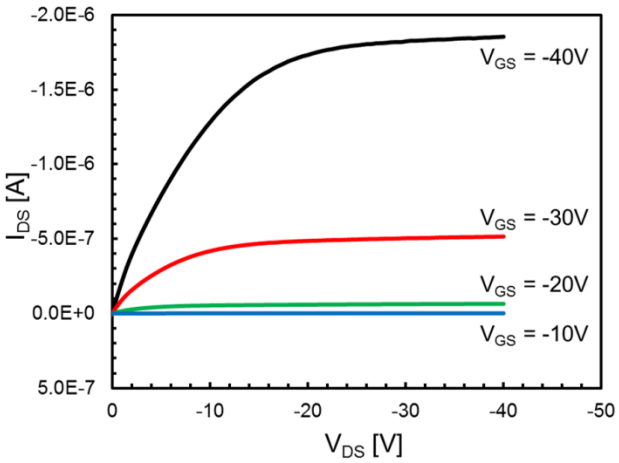


Fig. 2.6. Output characteristics of a p-type OTFT.

The charge carrier mobility is proportional to semiconductor conductivity, and is thus directly related to the performance of OTFT in terms of maximum operating frequency.

The charge carrier mobility is normally calculated in both linear and saturation regime. In linear regime (μ_{lin}), it can be estimated through the transistor transconductance value g_m calculated by differentiating the equation (2.2) and it is given by:

$$g_{m(lin)} = \left[\frac{\delta I_{DS}}{\delta V_{GS}}\right]_{V_{DS}=cost.} = \frac{WC_{OX}}{L}\mu_{lin}V_{DS} \tag{2.4}$$

Instead, in saturation regime the charge carrier mobility can be calculated by differentiating the equation (2.3) and it is given by the following expression:

$$\frac{\delta\left(\sqrt{I_{DS}}\right)}{\delta V_{GS}} = \sqrt{\frac{W C_{OX} \mu_{sat}}{2L}} \tag{2.5}$$

The charge carrier mobility in saturation region can be also evaluated from the plot of square-root of drain-source current versus the gate-source voltage. Moreover, the intercept point of this plot with x-axis provides a rough estimation of the threshold voltage as shown in Fig. 2.7.

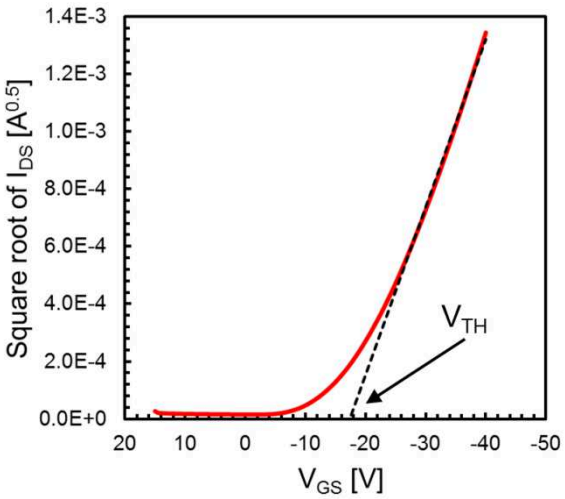


Fig. 2.7. Square-root of I_{DS} current versus V_{GS} voltage for a typical p-type OTFT.

It is important to notice that charge carrier mobility in OTFT is a function of gate voltage [11] [12]. According to the model reported in [11], applying a voltage between gate and source terminals charge carriers are induced in organic semiconductor and they are trapped in numerous traps and only a fraction of charge carriers contribute to current conduction. The relationship between mobility and gate-source voltage [11] is given by the following equation:

$$\mu = \mu_0 \left(\frac{V_{GS} - V_{TH}}{V_{AA}} \right)^{\gamma} \tag{2.6}$$

Where γ and V_{AA} are empirical parameter that can be extracted from the OTFT transfer characteristic and μ_0 is a constant.

Another important parameter for the OTFT is I_{ON}/I_{OFF} current ratio; it is defined as the ratio between the transistor current in accumulation mode and the transistor current in depletion mode. The I_{ON}/I_{OFF} current ratio is essential for evaluating the performance of OTFT when it is used as switch. Values as high as 10^7 were reported by recent OTFT technology [10], which are suitable for most applications.

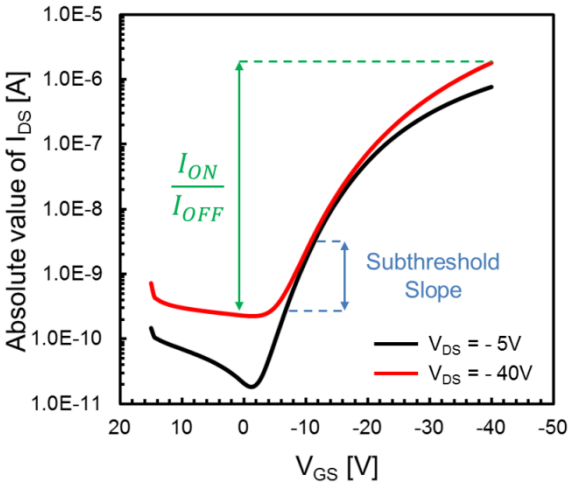


Fig. 2.8. Transfer characteristics of a p-type OTFT on logarithmic scale.

I_{ON}/I_{OFF} ratio and subthreshold slope (SS) can be extracted by the plot of drain-source current in saturation regime on a logarithmic scale versus the gate-source voltage as shown in Fig. 2.8.

Typically, the research activity on OTFT seeks to optimize two of the most important transistor parameters that are charge carrier mobility and I_{ON}/I_{OFF} ratio.

2.1.3 Organic TFT structures

Organic TFTs are basically made using only five layers, i.e. substrate, semiconductor layer, source/drain layer, dielectric layer and gate layer. Their performance is affected by both physical and chemical layer properties as well as from the order in which each layer is deposited on substrate.

Basically, there are four main organic TFT structures: Bottom Gate-Bottom Contact (BG-BC), Bottom Gate-Top Contact (BG-TC), Top Gate-Top Contact (TG-TC) and Top Gate-Bottom Contact (TG-BC). In all structures the Source/Drain electrode has to be in contact with organic semiconductor to inject and retrieve charge carriers and the gate layer has to be isolated from organic semiconductor by means of dielectric layer. Pros and cons of each structure are highlighted in the following sections.

2.1.3.1 Bottom Gate – Bottom Contact

It is the commonly used structure for fabricating OTFT since organic semiconductor is deposited without limit on previous steps, see Fig. 2.9. Source/drain and gate electrode can be made using photolithographic patterning. Instead, gate dielectric can be deposited using different methods, i.e. plasma-enhanced chemical vapor deposition, RF magnetron sputtering.

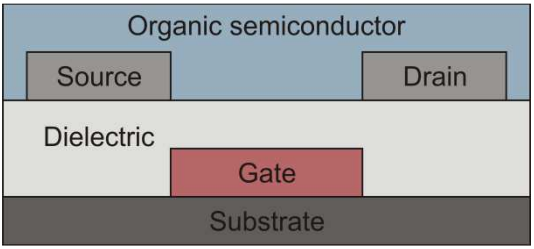


Fig. 2.9. Bottom Gate – Bottom Contact structure (BG-BC).

One of the main disadvantages of BG-BC structure is the large contact resistance due to the small effective area for charge injection into the transistor channel. Moreover, during organic semiconductor deposition its morphology is disrupted because it goes in contact with two different materials, i.e. gate dielectric and source/drain electrode, simultaneously. As a result, BG-BC structure is characterized by large source/drain contact barriers and contact resistance.

2.1.3.2 Bottom Gate – Top Contact

BG-TC structures (Fig. 2.10) typically show a lower contact resistance respect to the BC structure thanks to the larger effective area where charges are injected into the organic semiconductor. This area is equal to the overlap area of source/drain electrode with organic semiconductor.

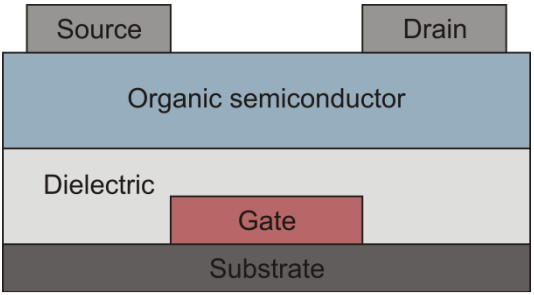


Fig. 2.10. Bottom Gate – Top Contact structure (BG-TC).

In this structure charge carriers that represent the transistor channel are induced on the opposite side respect to the source/drain electrodes. Thus, the charge carriers have to pass through an undoped highly resistive organic semiconductor layer. Mobility and threshold voltage of OTFTs made using this configuration may show a dependence on the thickness of the organic semiconductor layer.

Moreover, a photolithographic patterning cannot be made on organic semiconductor since organic semiconductor can be damaged; this means that source/drain electrodes have to be deposited using techniques with a lower resolution limiting the minimum transistor channel length.

2.1.3.3 Top Gate – Top Contact

This structure (Fig. 2.11) is not used because it is affected to a large contact resistance due to the small effective area in

which charge carriers are injected into the organic semiconductor for creating the transistor channel.

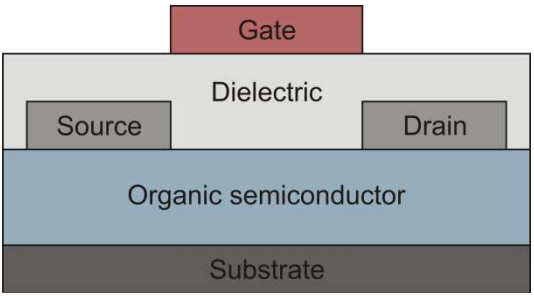


Fig. 2.11. Top Gate – Top Contact structure (TG-TC).

In this configuration, source/drain electrodes and gate dielectric are deposited on organic semiconductor layer. For this reason gate dielectric construction cannot be made using physical deposition methods such as sputtering due to the damages on organic semiconductor layer caused by the energetic ion during deposition. Moreover, for the same reason, photolithography techniques cannot be used for fabrication of source/drain electrodes.

In this structure gate dielectric encapsulate the organic semiconductor protecting it from oxygen and air exposure that can cause the degradation of organic semiconductor.

2.1.3.4 Top Gate – Bottom Contact

In this structure (Fig. 2.12) gate dielectric and gate electrode encapsulate organic semiconductor layer protecting it from any degradation processes.

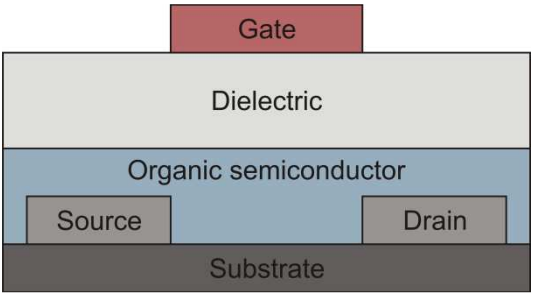


Fig. 2.12. Top Gate – Bottom Contact structure (TG-BC).

On the other hand, there are many challenges that have to be overcome during the integration of this structure.

As first thing, gate dielectric and gate electrode have to be fabricated on organic semiconductor layer avoiding any damages to the organic material.

As second thing, any vertical interconnections between gate and source/drain electrodes have to be made through the organic semiconductor and hence fabrication processes that do not damage organic material have to be used.

As third thing, the deposition of gate dielectric on organic semiconductor can damage or unintentionally dope it by affecting on the performance of OTFT in terms of I_{ON}/I_{OFF} ratio.

TG-BC structure is characterized by a low contact resistance because the effective area for injecting of the charge carriers into the organic semiconductor is quite large; source/drain electrodes are embedded into the organic material.

High resolution and integration of organic TFT can be achieved because photolithographic pattering can be used for fabricating gate and source drain electrodes.

2.2 Fully-printed organic complementary technology on flexible substrate

Circuits and systems reported in this thesis work were fabricated using the fully-printed complementary organic technology on flexible substrate developed by CEA-LITEN, Grenoble, France [10] [13-15].

Circuits fabrication is carried out on 11 cm x 11 cm flexible substrate, see Fig. 2.13. The organic complementary thin-film transistors (C-OTFT) are implemented in a top-gate bottom-contact multi-finger structure with a minimum

channel width (W) and length (L) of 140 µm and 5 µm, respectively. The technology process also features metal-insulator-metal (MIM) capacitors with a specific capacitance of 20 pF/mm^2, which are built by using source/drain metal layer, gate dielectric layer and gate metal layer. Thanks to an additional process step, resistors with a sheet resistance of 35 kΩ/sq can also be integrated by screen-printing a carbon-ink after the organic semiconductor deposition and before the screen-printing of gate metal layer.

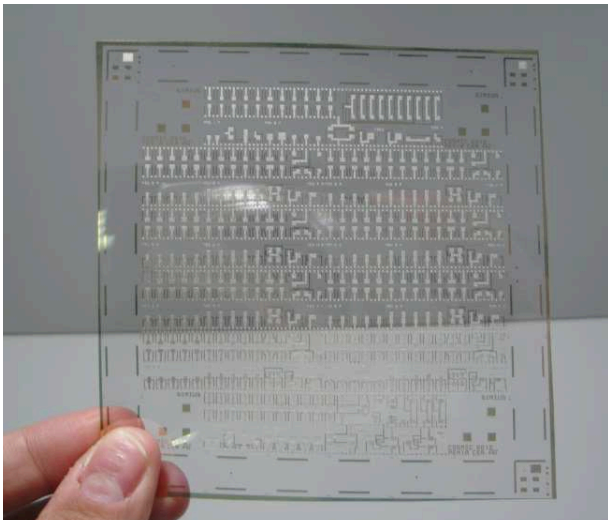


Fig. 2.13. Picture of 11 cm x 11 cm flexible foil with fully-printed OTFTs and digital and analog CMOS basic building blocks.

The OTFT cross-section and a microphotograph of an OTFT with a W=2000 µm and L=20 µm are shown in Figs. 2.14 and 2.15, respectively.

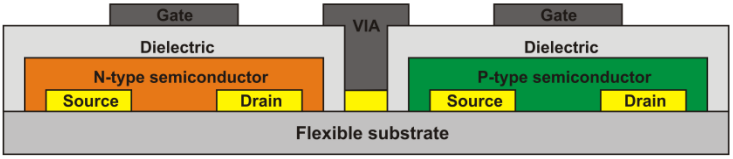


Fig. 2.14. Transistor cross-section of the fully-printed organic complementary technology on flexible substrate developed by CEA.

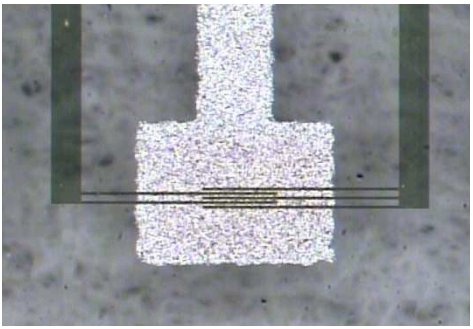


Fig. 2.15. Microphotograph of a multi-finger OTFT with a W=2000 µm and L=20 µm fabricated by CEA.

The fabrication process is characterized by few steps, see Fig. 2.16. It starts from a 125 µm thick polyethylene-naphtalate (PEN) foil that is a robust and flexible substrate. The first step consists of a sputtering of a 30 nm gold layer

that is then patterned using photolithography or laser ablation processes for realizing the source/drain electrodes as well as the first metal layer for interconnection.

N-type organic semiconductor is deposited before the p-type one. In the second step, the deposition of n-type organic semiconductor is preceded by the deposition of the Self-Assembled Monolayer (SAM) useful for the optimization of the electron injection in the Lowest Unoccupied Molecular Orbital (LUMO) [16]. The n-type organic semiconductor is patterned by means of printing method leading to create a final thickness in the range from 50 nm to 200 nm.

In the third step, a cleaning process with O_2 UV free plasma during 180 s is carried out in order to prepare the p-type area and the substrate for the deposition of SAM and p-type organic semiconductor. Also in this case, p-type material has a thickness in the range from 50 nm to 200 nm.

In the fourth step, the common fluoropolymer dielectric (CYTOP) that is the gate dielectric is deposited using the screen-printing technique on top of both semiconductors. The dielectric layer is then annealed reaching a final thickness of 750 nm. At the end, the gate electrodes and the second metal layer for interconnection are fabricated using a silver-ink conductor paste that is screen-printed and annealed at 100 °C.

In Fig. 2.16 is shown a simplified and schematic view of the fabrication process steps.

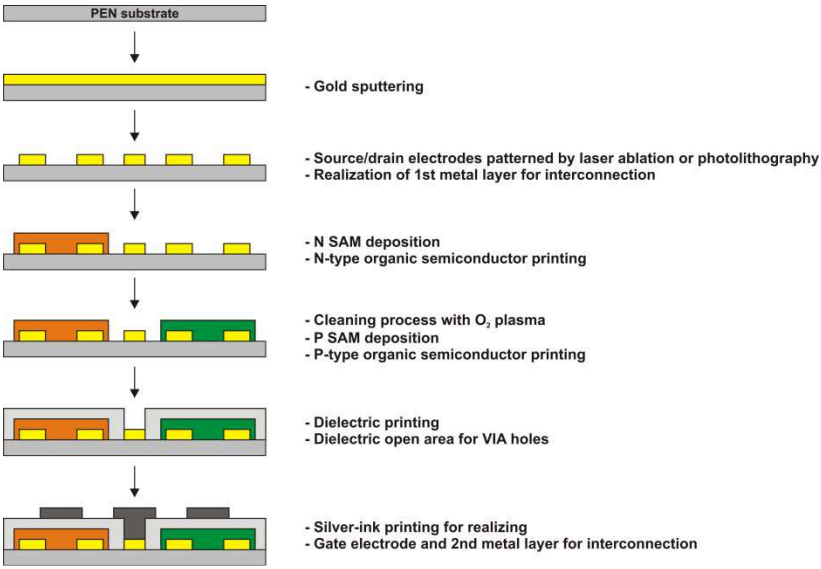


Fig. 2.16. Schematic view of the fabrication process steps of the fully-printed complementary organic technology on flexible substrate developed by CEA.

Two different process generations (GEN1 [13] and GEN2 [10], respectively) were developed by CEA-LITEN. The process flow above described refers to the latest process GEN2 that shows better performance respect to the GEN1 thanks to an additional optimization step based on a cleaning process with O_2 UV free plasma for a time of 180 s. As

clearly reported in [10], the optimization process guarantees better stability and repeatability of transistor's performance as well as a higher process yield.

Table 2.2 summarizes the measured electrical characteristics of both p-type and n-type OTFT, fabricated using GEN2 process flow, with a channel width and channel length of 2000 µm and 20 µm, respectively.

	p-OTFT	n-OTFT
μ_{SAT} [$cm^2/V \cdot s$]	1.5	0.55
I_{ON}/I_{OFF} ratio	10^4	$2 \cdot 10^5$
Subthreshold Slope [V/decade]	4	2
$V_{TH(SAT)}$ [V]	-22	18

Table 2.2. Measured electrical characteristics of both p-type and n-type OTFT with W=2000 µm and L=20 µm.

Output and transfer characteristics of GEN2 p-type and n-type transistors with channel width and length of 2000 µm and 20 µm are reported in Figs. 2.17, 2.18, 2.19 and 2.20, respectively.

A dedicated compact transistor model was developed for this technology [17]. This model is physically based and can describe both n-type and p-type OTFTs. The electrical

characteristics of transistor are basically modeled as a series of an “ideal transistor” and a reverse biased Schottky diode.

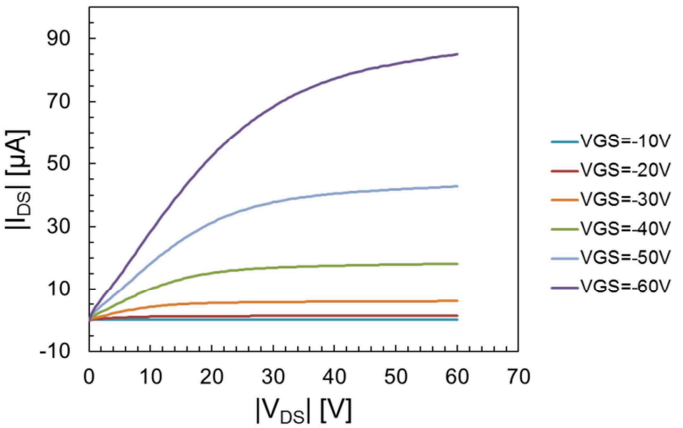


Fig. 2.17. Output characteristics of p-type OTFT with channel width and length of 2000 μm and 20 μm, respectively.

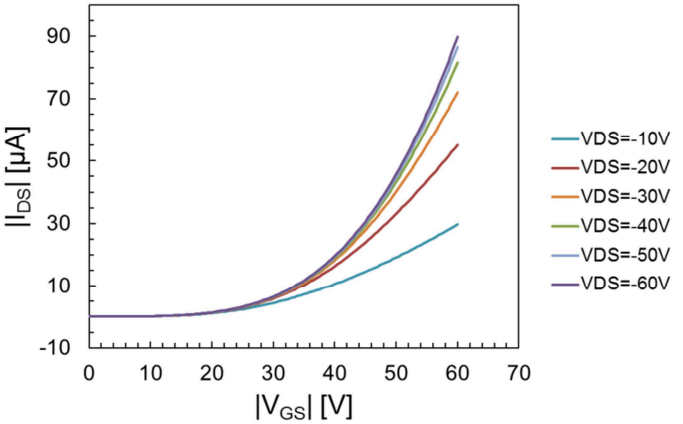


Fig. 2.18. Transfer characteristics of p-type OTFT with channel width and length of 2000 μm and 20 μm, respectively.

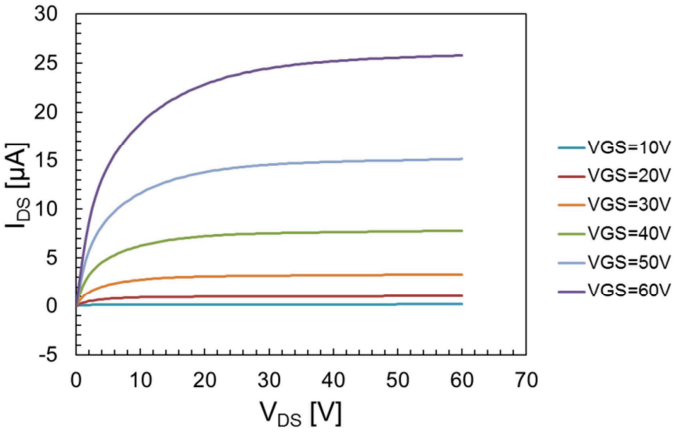


Fig. 2.19. Output characteristics of n-type OTFT with channel width and length of 2000 μm and 20 μm, respectively.

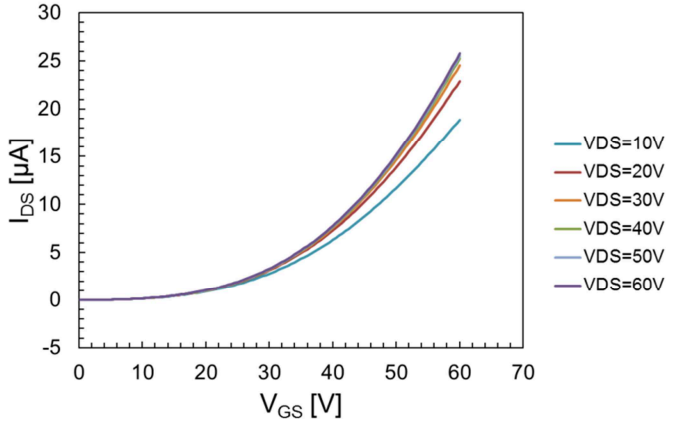


Fig. 2.20. Transfer characteristic of n-type OTFT with channel width and length of 2000 μm and 20 μm, respectively.

2.3 Digital and analog basic building blocks

Several digital and analog basic building blocks were designed using OTFT manufactured in a fully-printed complementary organic technology on flexible substrate. The main technology characteristics were already presented in the previous paragraph (¶ 2.2).

Circuits design was carried out by taking advantage of the dedicated transistor model in [17].

In the following section, measurements of seven stage ring oscillator and fully-static logic gates such as inverters, NAND gate and J/K flip-flop are reported. Moreover, measured results of first dynamic NAND gate and positive edge triggered TSPC D flip-flop are also presented.

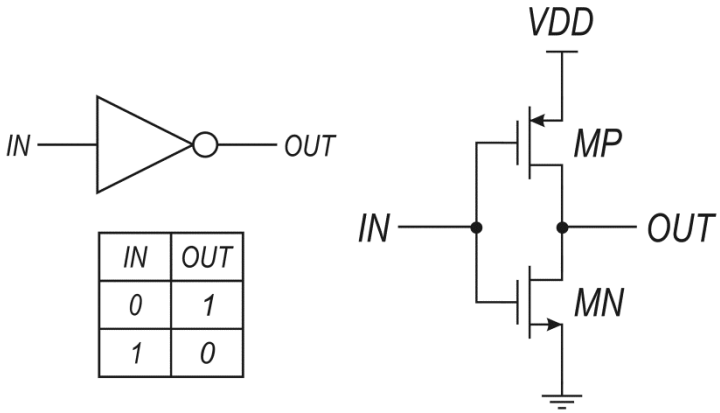
Finally, measurements of differential gain stage with active load and a complete characterization of simple rectifier/envelope detector up to 13.56-MHz are also discussed.

2.3.1 Static CMOS inverter and NAND gate

Most of the published organic logic gates were fabricated using only p-type OTFTs. They are mainly based on ratioed logic architecture in which the pull-down network is made up of a diode-connected p-type transistor or by using a zero-V_{GS}

load [18]. Moreover, a new design logic named *PMOS-only Pre-Discharge* logic was also proposed in [19] to implement logic functions. It uses mostly p-type OTFTs based on principles of dynamic logic.

The availability of complementary technology that integrate both p-type and n-type OTFTs allows implementation of static CMOS logic gates that show better performance in terms of power dissipation, noise margin as well as less required area for integration respect to the ratioed logic gates.



IN	OUT
0	1
1	0

Fig. 2.21. Symbol, truth table and schematic of a static CMOS inverter.

The CMOS inverter is the nucleus of all digital design since the electrical behavior of more complex digital circuits such as logic gates, adders, multipliers and microprocessors can be almost completely derived by extrapolating the results obtained from it.

Symbol and schematic of a static CMOS inverter are shown in Fig. 2.21.

Static CMOS inverters with fixed transistor channel length and three different p-type and n-type transistor channel width ratios were designed. Table 2.3 shows the transistor sizing of all designs; the transistor channel length and the minimum channel width were fixed at 20 µm and 500 µm, respectively.

Transistor sizing - Inverters		
Description	$(W/L)_P$ [µm/µm]	$(W/L)_N$ [µm/µm]
Inverter (1:1)	500/20	500/20
Inverter (1:2)	500/20	1000/20
Inverter (1:4)	500/20	2000/20

Table 2.3. Transistor sizing of the static CMOS inverters.

Inverter (1:1) was designed by using the same channel width for both p-type and n-type transistors. Inverter (1:2) was designed by fixing the channel width of p-type and n-type transistor at 500 µm and 1000 µm, respectively. Finally,

inverter (1:4) was designed by fixing the channel width of p-type and n-type transistors at 500 µm and 2000 µm, respectively.

Layout picture and photograph of the three designed and measured inverters are shown in Fig. 2.22.

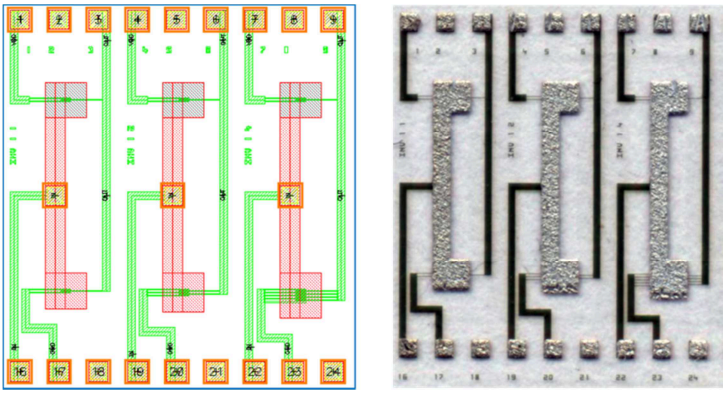


Fig. 2.22. Layout picture and photograph of the static CMOS inverters.

The layout was arranged by using only two metal layers for interconnection and by taking the p-type and n-type transistors at the minimum distance according to the technology design rules for minimizing the area consumption.

Measurements were performed in air at ambient temperature/pressure conditions. All dc measurements were

performed on foil by means of a probe station and a semiconductor parameter analyzer.

Fig. 2.23 reports the measured input/output characteristics of the three inverters at two different supply voltages, 20 V and 40 V, respectively.

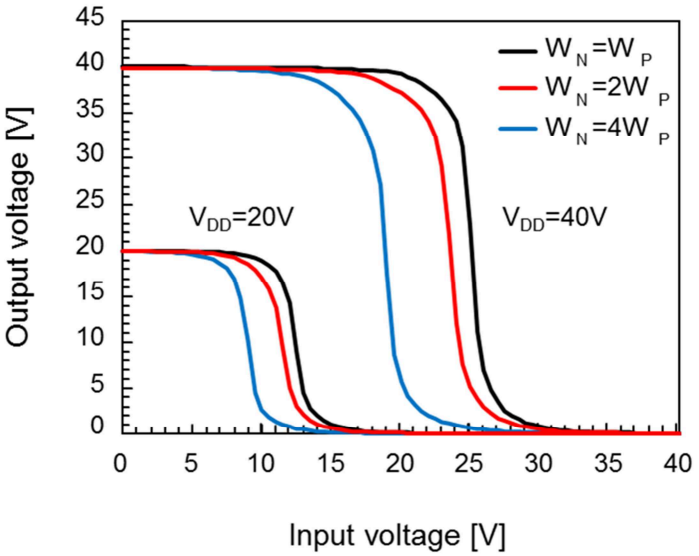


Fig. 2.23. Input-output characteristics of the three inverters at two different supply voltages.

It is advisable to balance the driving capability of both p-type and n-type transistors when designing static CMOS inverter. A good balance ensures a symmetric input/output characteristic that means that invert switching threshold

voltage is equal to one half of supply voltage. A symmetric input/output characteristic also guarantees a better noise margin performance of the logic gate.

Measurement results reported in Fig. 2.23 demonstrate that the CMOS inverter made using n-type transistor wider to the p-type transistor shows a symmetric input/output characteristic respect to the other ones.

The switching threshold voltage of a static CMOS inverter is given by the following equation (2.7):

$$V_M = \frac{V_{DD} + \sqrt{\frac{\mu_N \left(\frac{W}{L}\right)_N}{\mu_P \left(\frac{W}{L}\right)_P}} \cdot V_{THN} - |V_{THP}|}{1 + \sqrt{\frac{\mu_N \left(\frac{W}{L}\right)_N}{\mu_P \left(\frac{W}{L}\right)_P}}} \tag{2.7}$$

According to the equation (2.7) the channel width ratio between n-type and p-type transistor has to be chosen to compensate the differences between two type transistors in terms of charge carrier mobility and threshold voltage for having a symmetric input/output characteristic.

Since in the adopted complementary organic technology the measured charge carrier mobility of the p-type organic

semiconductor (1.5 cm^2/V s) is greater than the n-type organic semiconductor (0.55 cm^2/V s), equation (2.7) and the experimental results demonstrate that for a robust design it is needed to increase the channel width of the n-type transistor respect to the p-type transistor in order to have a balanced current capability and a symmetric input/output characteristic.

The voltage gain of CMOS inverter can be extracted from its input/output characteristic. Fig. 2.24 shows the voltage gain of the three inverters for a supply voltage of 40 V. Static CMOS inverters have a voltage gain as high as 20 (26 dB).

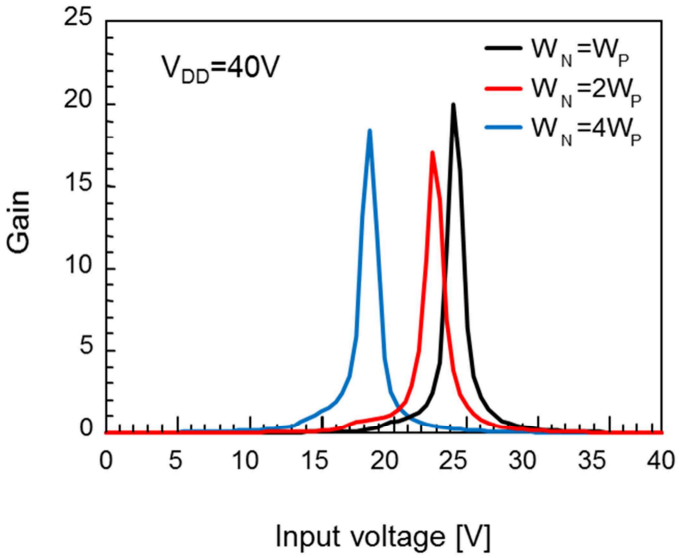
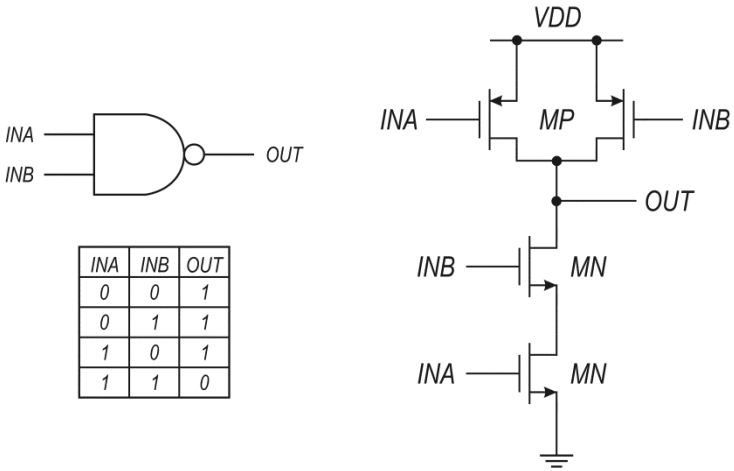


Fig. 2.24. Gain vs. input voltage of the three CMOS inverters for a supply voltage of 40 V.

Inverters with equal or higher gain were already reported in [20 - 22] but they were not fabricated using fully-printed technology that typically ensures a low manufacturing cost.

A static CMOS NAND gate was also designed and tested. Fig. 2.25 shows symbol, truth table and schematic of a static CMOS NAND gate.



INA	INB	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 2.25. Symbol, truth table and schematic of a static CMOS NAND gate.

NAND gate was designed considering the equivalent inverter gate and assuming that the charge carrier mobility ratio between p-type and n-type transistor was 2. The transistor sizing of NAND gate is reported in Table 2.4.

Transistor sizing – NAND gate	
Description	W/L [µm/µm]
MN	2000/20
MP	500/20

Table 2.4. Transistor sizing of the static CMOS NAND gate.

The layout picture and photograph of the NAND gate are shown in Fig. 2.26.

Also in this case the NAND gate layout was arranged by using only two metal layers for interconnection and by taking the p-type and n-type transistor at the minimum distances according to the technology design rules.

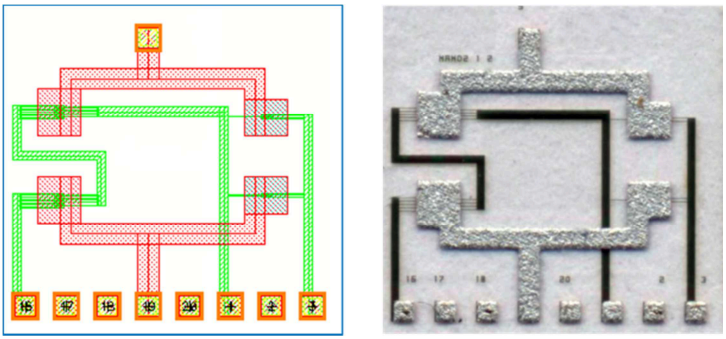


Fig. 2.26. Layout picture and photograph of the static CMOS NAND gate.

NAND gate was tested in air at ambient temperature/pressure condition. The dc measurement was performed on foil by using a probe station and a semiconductor parameter analyzer.

Supply voltage was set at 40 V; dc characteristic was measured fixing one input (input B) at high value (40 V) and sweeping the other one from 0 to 40 V. The measured dc characteristic is shown in Fig. 2.27. It demonstrates the correct functionality of NAND gate.

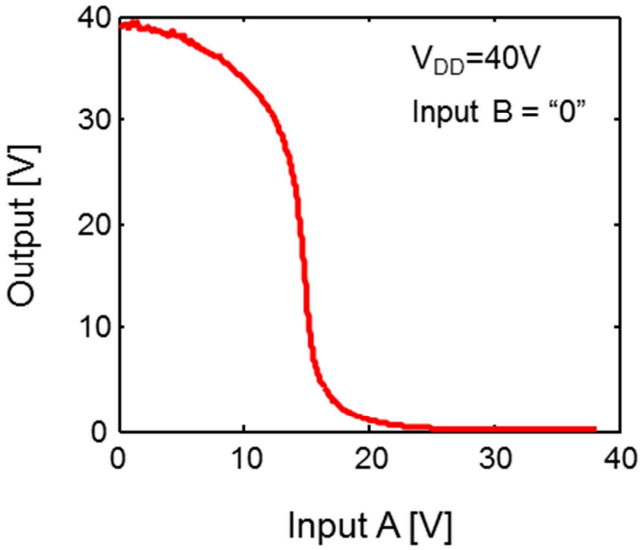


Fig. 2.27. Measured dc characteristic of the static CMOS NAND gate.

2.3.2 7-stage CMOS ring oscillator

For comparing the performance of different technologies, circuits or logic design style the propagation delay is mostly used. The propagation delay of a gate defines how quickly it responds to a change at its input. It expresses the delay experienced by a signal when passing through a gate. The propagation delay is measured between the 50% transition points of the input and output waveforms.

It is easy to understand that for comparing performance of different technologies a standard way to measure the propagation delay is needed.

Ring oscillator is the standard circuit used for measuring the propagation delay. It consists of an odd number of inverting stage connected in a circular chain. Due to the odd number of inversions it does not have a stable operating point and thus oscillates. The oscillation frequency is given by the following equation (2.8):

$$f_{OSC} = \frac{1}{2 \cdot N \cdot t_D} \tag{2.8}$$

Where N is the number of inverting stages and t_D is the propagation delay of each inverting stage. Moreover, the sum of fall and rise time of the inverting stage must be smaller

than the period of oscillation ($T_{OSC}=2 \cdot N \cdot t_D >> t_f + t_r$) in order to be sure that the circuit oscillate. For this reason, typically ring oscillator is made using at least five inverting stages.

A CMOS ring oscillator was designed using the cascaded of seven stage of static CMOS inverter made with equally sized p-type and n-type organic thin-film transistor. The ring oscillator schematic and transistor sizing are reported in Fig. 2.28 and Table 2.5, respectively.

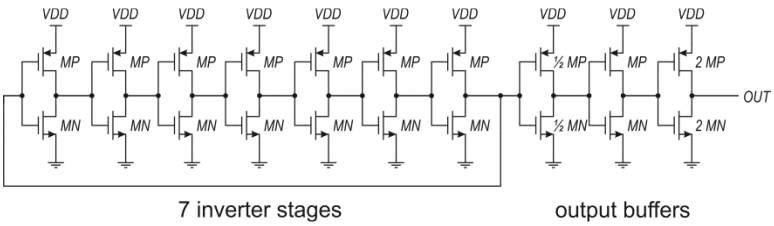


Fig. 2.28. Schematic of the 7-stage CMOS ring oscillator.

Transistor sizing – 7 stages ring oscillator		
Description	$(W/L)_N$ [µm/µm]	$(W/L)_P$ [µm/µm]
Inverter stage	1000/20	1000/20
Output buffer (1/2)	500/20	500/20
Output buffer (1)	1000/20	1000/20
Output buffer (2)	2000/20	2000/20

Table 2.5. Transistor sizing of the 7-stage CMOS ring oscillator.

A three stages tapered output buffer was also integrated in order to avoid the loading effect introduced by the lab equipment during the experimental characterization.

The layout picture and photograph of 7-stage ring oscillator are shown in Figs. 2.29 and 2.30, respectively.

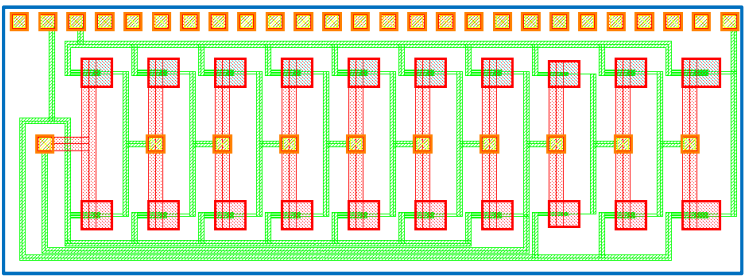


Fig. 2.29. Layout picture of the 7-stage CMOS ring oscillator.

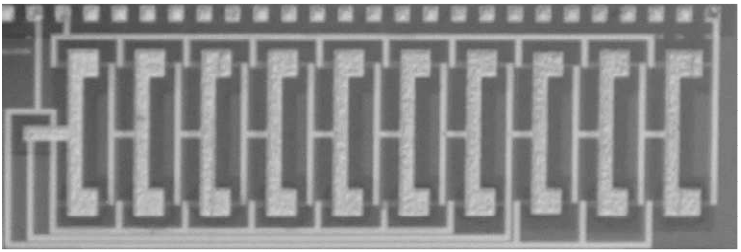


Fig. 2.30. Photograph of the 7-stage CMOS ring oscillator.

Ring oscillator layout was arranged by using only two metal layers for interconnection and by taking p-type and n-

type transistors at minimum distance allowed by technology design rules.

Ring oscillator was tested on foil and in air at ambient temperature/pressure condition. During the experimental characterization the ring oscillator was supplied by using two different voltage values, 40 V and 20 V, respectively. For a supply voltage of 40 V the measured oscillation frequency was 1.2 kHz that corresponds to a propagation delay per stage of 60µs, as shown in Fig. 2.31. Instead, for a supply voltage of 20V the measured oscillation frequency was 200 Hz that corresponds to a propagation delay per stage of 350 µs, as shown in Fig. 2.32.

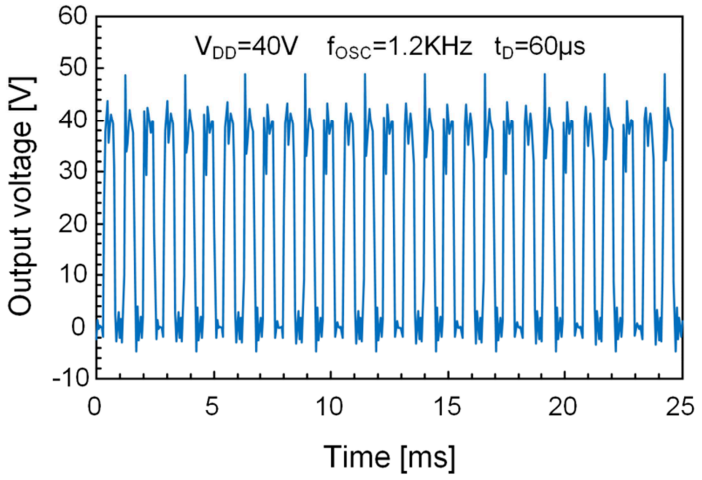


Fig. 2.31. Output waveform of the 7-stage CMOS ring oscillator at a supply voltage of 40 V.

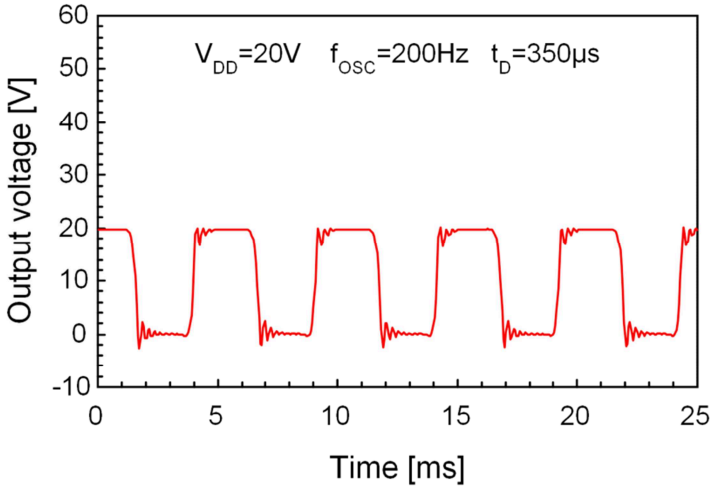


Fig. 2.32. Output waveform of the 7-stage CMOS ring oscillator at a supply voltage of 20 V.

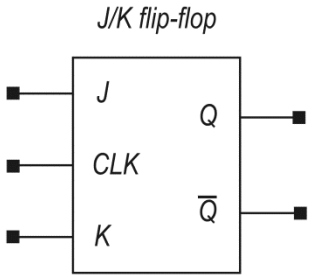
The variation of the oscillation frequency respect to the supply voltage is produced by the variation of the propagation delay of a static CMOS inverter that is inversely proportional to the supply voltage. As expected in both cases the output signal is a rail-to-rail signal.

The 7-stage CMOS ring oscillator reported in [13] was fabricated using the first generation (GEN1) of CEA-LITEN organic complementary technology. It shown an oscillation frequency of 70 Hz (t_D = 1 ms) and 16 Hz (t_D = 4.5 ms) for a supply voltage of 40 V and 20 V, respectively.

The measured ring oscillator was shown better performance thanks to the use of optimized materials and fabrication process that ensure higher charge carriers mobility for both p-type and n-type transistors as well as better stability and repeatability of transistor performance. Since the propagation delay of a logic gate is inversely proportional to the charge carrier mobility a higher value of mobility guarantees a higher operating frequency of the OTFT and thus of the logic gates. The achieved results are also better than that presented in [23 - 26] even though the supply voltage is much higher (i.e., 40 V against 2 V).

2.3.3 Static CMOS J/K flip-flop

A more complex digital circuit such as static CMOS J/K flip-flop was also designed. Its symbol and truth table is reported in Fig. 2.33.



J	K	Q	$\overline{Q}$	Q_{n+1}
0	0	Q	$\overline{Q}$	Q_n
0	1	0	1	0
1	0	1	0	1
1	1	$\overline{Q}$	Q	$\overline{Q}_n$

Fig. 2.33. Symbol and truth table of a static CMOS J/K flip-flop.

The static CMOS J/K flip-flop was implemented adopting the classical solution that employs four static CMOS NAND gates, as depicted in Fig. 2.34.

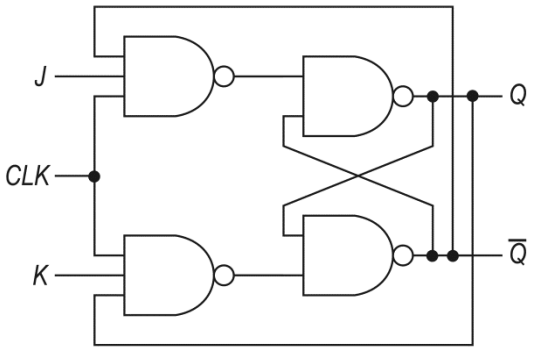


Fig. 2.34. Schematic of a static CMOS J/K flip-flop implemented using three and two inputs NAND gate.

Two and three inputs NAND gates were designed by using a fully static approach and assuming that the charge carrier mobility ratio between p-type and n-type transistor was 2. For the sake of clarity, their schematics at transistor level and transistor sizing are shown in Fig. 2.35 and Table 2.6, respectively.

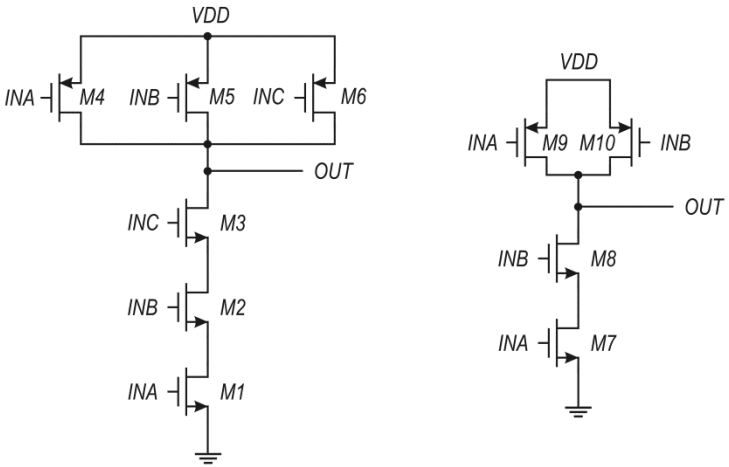


Fig. 2.35. Schematic of three and two inputs static CMOS NAND gates used for designing the static CMOS J/K flip-flop.

Transistor sizing – JK flip-flop		
3 inputs NAND gate		
Description	Type	W/L [µm/µm]
M1, M2, M3	N	3000/20
M4, M5, M6	P	500/20
2 inputs NAND gate		
Description	Type	W/L [µm/µm]
M7, M8	N	2000/20
M9, M10	P	500/20

Table 2.6. Transistor sizing of the static CMOS J/K flip-flop.

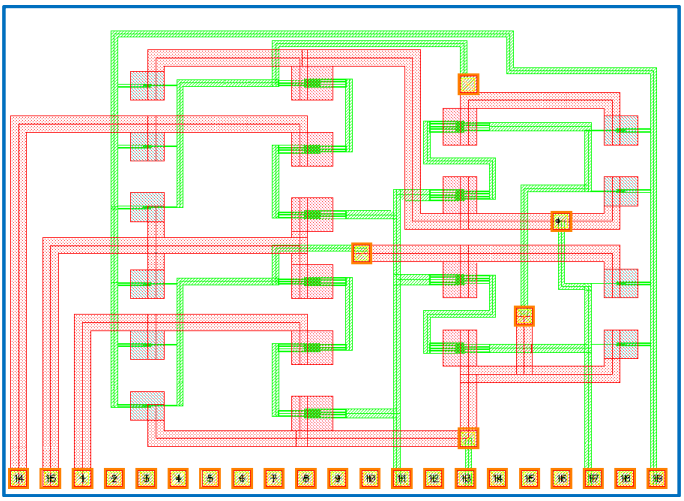


Fig. 2.36. Layout picture of the static CMOS J/K flip-flop.

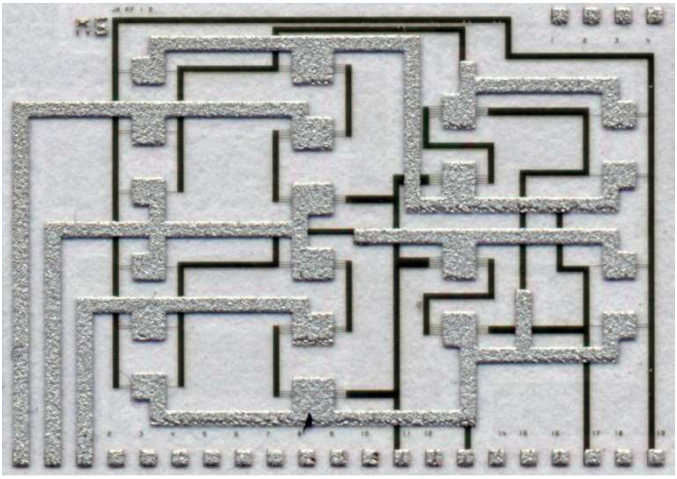


Fig. 2.37. Photograph of the static CMOS J/K flip-flop.

The layout picture and photograph of the J/K flip-flop are shown in Figs. 2.36 and 2.37. Layout was optimized in order to minimize area consumption and using only two metal layers for interconnection.

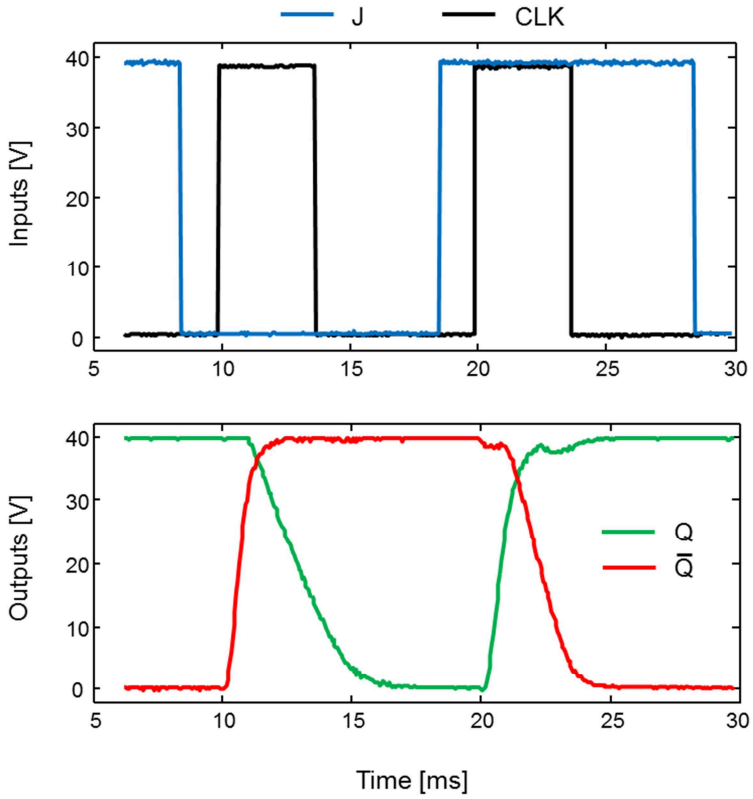


Fig. 2.38. Experimental result of the static CMOS J/K flip-flop.

Static CMOS J/K flip-flop was measured on foil and in air at ambient temperature/pressure condition. In particular, it was tested by setting the supply voltage at 40 V and by using a 100 Hz clock signal. In order to simplify the flip-flop characterization its inputs are set so that it can work as a D flip-flop. It was done by setting the K input signal as a negated of the J input signal. Measurement results shown in Fig. 2.38 are reasonably close to the circuit simulations and agree to the expected behavior described by the flip-flop truth table. Only the pull-down process is slightly slower than what predicted with simulations.

2.3.4 Dynamic CMOS NAND gate and positive edge triggered TSPC D flip-flop

The screen-printing processes used for fabrication of organic thin-film transistors in the adopted complementary technology require a large distance between n-type and p-type OTFTs. The area consumption of circuits is strong affected by the number of transistors. Increasing the complexity of the digital circuits or systems the required area for integration could be so high making the circuit design unfeasible.

A logic function implemented in static CMOS logic requires 2N transistors, where N is the fan-in number. For

example, a master-slave D flip-flop designed using a fully static approach requires at least 36 transistors.

A variety of different approach were developed in order to reduce the number of transistors required for the implementation of a given logic function. One of them is the *dynamic logic* gates. With dynamic logic approach the required number of transistors is substantially lower than in the fully static approach (i.e., N+2 against 2N). Moreover, the switching speed of dynamic logic is faster compared with a static logic. It only consumes dynamic power even though the overall current consumption can be significantly higher compared with a static logic.

The operation of dynamic logic is mainly divided into two main phases: *pre-charge* and *evaluation*.

The basic construction of dynamic logic gate made using pull-down network (PDN) is shown in Fig. 2.39. The logic function is implemented by the pull-down network and its synthesis is made using the same design strategy for a static CMOS logic.

When CLK="0" the dynamic logic is in pre-charge phase and its output node is pre-charged to high level (V_{DD}). In this case the evaluate n-type transistor (M_E) is off, so the PDN is disabled.

When CLK="1" the dynamic logic is in evaluation phase and its output value is a function of the PDN inputs. If the PDN inputs are such that the PDN conducts the output goes to low level (GND) otherwise the output continues to stay to high level (V_{DD}).

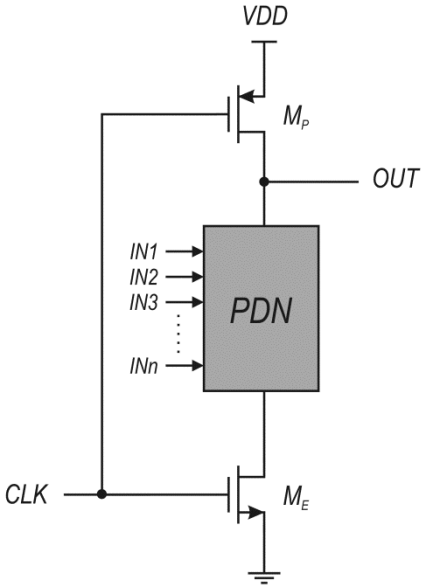


Fig. 2.39. Basic structure of a dynamic logic gate implemented with PDN.

The main advantages of dynamic logic are increased speed and reduced integration area compared to the static logic but it is affected by some signal integrity issues that include charge

leakage, charge sharing, capacitive coupling, and clock feedthrough. More details about them are discussed in [27].

Despite above mentioned advantages, fully static logic gates typically show better performance in terms of noise margin compared to dynamic logic gates.

A dynamic NAND gate and a positive edge triggered TSPC D flip-flop were designed in order to investigate the feasibility of dynamic logic circuits with organic complementary technology. The possibility to integrate dynamic logic gates with organic CMOS technology allows saving integration area thus increasing the complexity of digital circuits and systems allowing to using them in a real application.

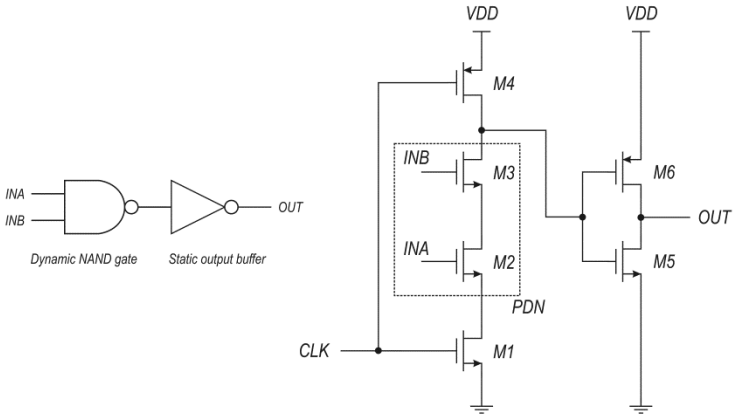


Fig. 2.40. Schematic of the dynamic CMOS NAND gate with an additional static CMOS output buffer.

The schematic of dynamic NAND gate and the transistor sizing are shown in Fig. 2.40 and Table 2.7, respectively. A static CMOS output buffer was added for testing purposes, so the overall logic function is AND.

Transistor sizing – Dynamic NAND gate		
Description	Type	W/L [µm/µm]
M1, M2, M3	N	3000/20
M4	P	500/20
M5	N	2000/20
M6	P	1000/20

Table 2.7. Transistor sizing of the dynamic CMOS NAND gate and static CMOS output buffer

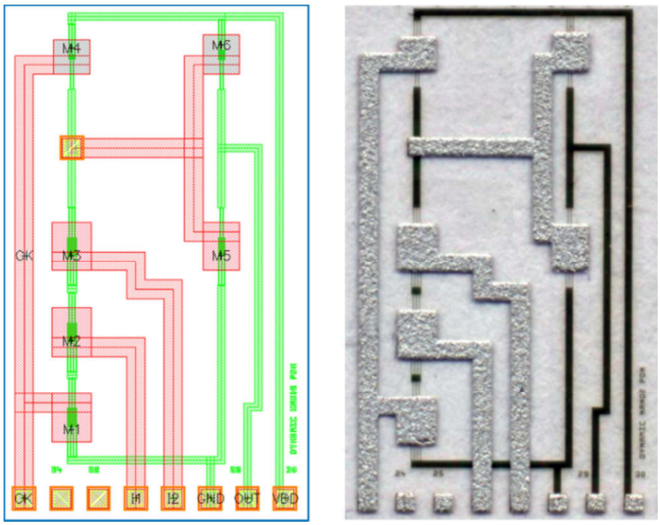


Fig. 2.41. Layout picture and photograph of the dynamic CMOS NAND gate with static CMOS output buffer.

The design of the dynamic NAND gate and the static output buffer was carried out assuming that charge carriers mobility ratio between the p-type and n-type transistors was 2.

The layout picture and the photograph of the dynamic NAND gate are shown in Fig. 2.41.

Layout was arranged in order to minimize the area consumption; p-type and n-type transistors were located at the minimum distance allowed by technology design rules.

Dynamic NAND gate was tested on foil in air at ambient temperature/pressure condition.

During the experimental characterization the supply voltage was set to 40 V and the frequency of the clock signal was set to 150 Hz. Measurement results shown in Fig. 2.42 were achieved by fixing one input of the logic gate to high level (INB="1") and the other input was changed. As can be noticed when the clock signal is low the output of dynamic gate goes high (V_{DD}) driving the output of the static buffer to low level (GND). As expected, when the clock signal goes high the output static buffer gate goes high only when both input signals are high. In other words, the output of dynamic gate goes low only when both input signals are high so it works as a NAND gate and hence, as expected, the overall system works as an AND gate.

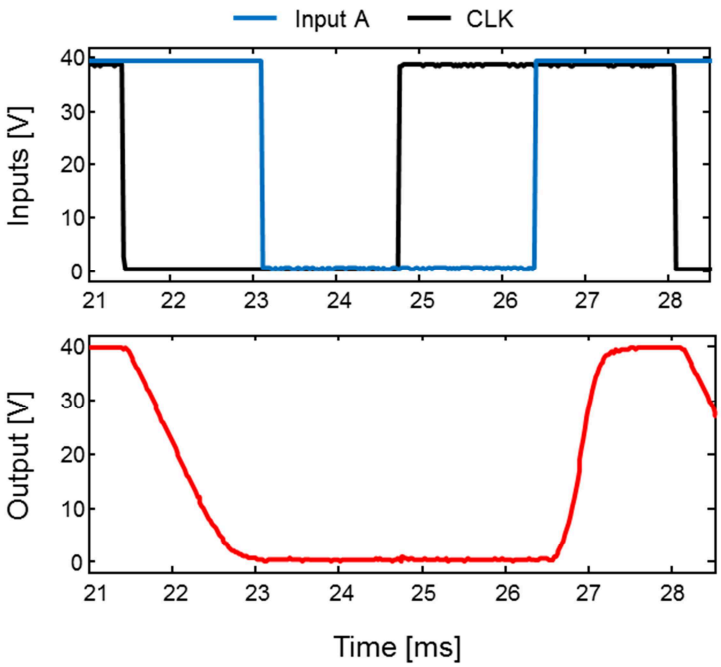


Fig. 2.42. Experimental result of the dynamic NAND gate for two different input states (A="0", B="1" and A="1", B="1").

A positive edge triggered TSPC D flip-flop was also designed, fabricated and tested. As can be seen in Fig. 2.43, it consists of only 11 transistors and thus the area needed for its integration is much smaller compared to that required for the fabrication of fully static D flip-flop.

The flip-flop operation is determined by the clock signal. When the clock signal is low the first inverter stage is transparent and its output (A) is equal to negated of input D,

while the second stage is in pre-charge phase and its output (B) goes to high level (V_{DD}); the third stage is disable and it stays in hold mode.

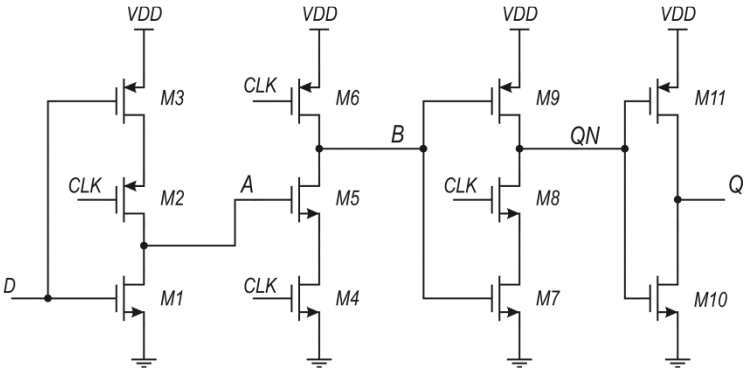


Fig. 2.43. Schematic of the positive edge triggered TSPC D flip-flop.

When the clock signal goes from low to high level (rising edge) the output of the second stage (B) changes and its value depends by the input value (A) (B stays high if A is low and B goes low if A is high); the output of third stage (QN) also changes and the flip-flop output (Q) is equal to its input (D). In other words, the flip-flop output only changes during the transition of the clock signal from low to high state and its value follows the input signal (D).

Transistor sizing is reported in Table 2.8. TSPC D flip-flop was designed assuming that the charge carrier mobility ratio between p-type and n-type transistor was 2.

Transistor sizing – TSPC D flip-flop		
Description	Type	W/L [µm/µm]
M1	N	500/20
M2, M3	P	500/20
M4, M5	N	2500/20
M6	P	500/20
M7, M8	N	2000/20
M9	P	500/20
M10	N	2000/20
M11	P	1000/20

Table 2.8. Transistor sizing of the positive edge triggered TSPC D flip-flop

Layout picture and photograph are shown in Fig. 2.44 and Fig. 2.45; layout was arranged to save integration area and only two metal layers were used for interconnection.

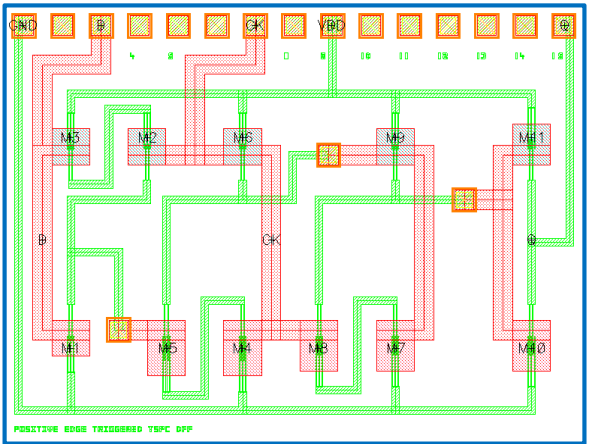


Fig. 2.44. Layout picture of the positive edge triggered TSPC D flip-flop.

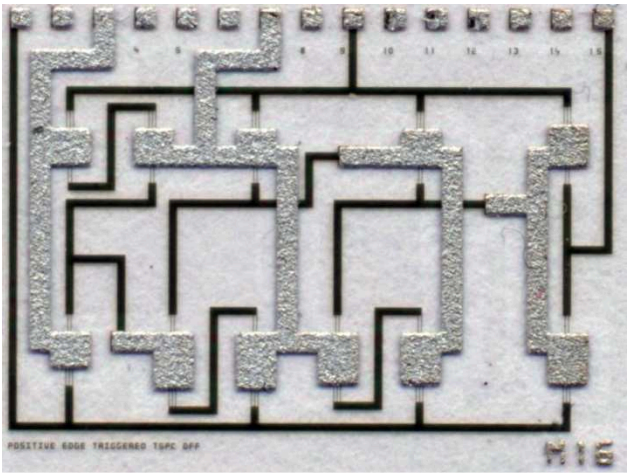


Fig. 2.45. Photograph of the positive edge triggered TSPC D flip-flop.

Flip-flop was tested on foil in air at ambient temperature/pressure condition.

Supply voltage was fixed at 40 V and the frequency of the clock signal was set at 100 Hz. Measurement results are shown in Fig. 2.46. As can be seen, in the first rising edge of the clock signal the flip-flop input (D) is high and as expected the flip-flop output (Q) goes high following the input signal. In the second rising edge of the clock signal the flip-flop input (D) is low and also in this case the flip-flop output (Q) goes low. As expected, with the provided clock and input signals, the flip-flop output (Q) is a delayed replica of its input (D).

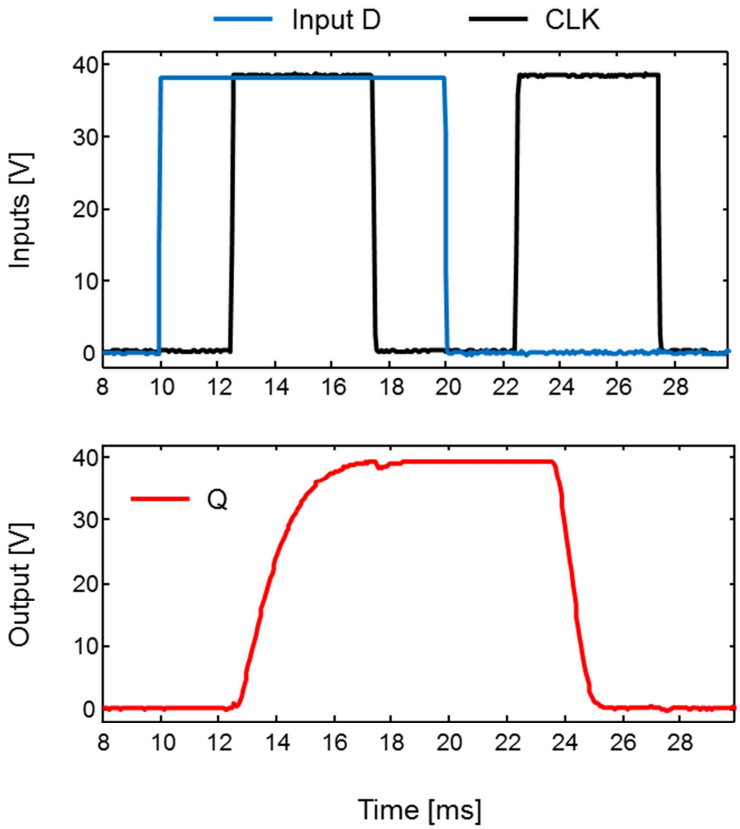


Fig. 2.46. Experimental result of the positive edge triggered TSPC D flip-flop.

This is the first reported [15] positive edge triggered TSPC D flip-flop fabricated using a fully-printed complementary organic technology on flexible substrate.

2.3.5 Single-stage CMOS differential amplifier with active load

The performance of a single stage differential amplifier with current mirror active load was also investigated. Two different amplifier versions with both p-type and n-type input differential pair were designed, circuit schematic are shown in Fig. 2.47.

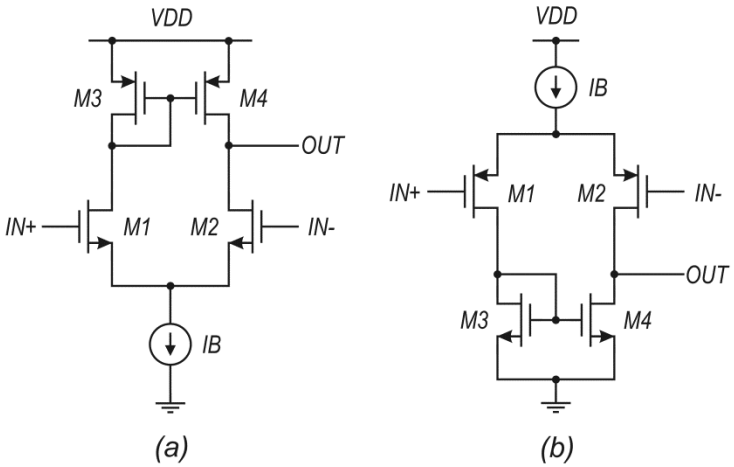


Fig. 2.47. Schematic of the single stage CMOS differential amplifier with complementary active load. (a) n-type input differential pair; (b) p-type input differential pair.

The availability of an organic complementary technology allows designing a differential amplifier with a current mirror active load that performs the differential to single-ended

signal conversion without any loss of voltage gain. Since the current mirror active load increases the differential amplifier transconductance value by a factor 2 and hence the voltage gain is 6 dB higher compared to a differential gain stage that exploits a resistive load.

Differential amplifier is typically the first gain stage of every operational amplifier (OP-AMP); since it has a strong impact on the fundamental OP-AMP characteristics such as input offset voltage, noise and common mode signals rejection (CMRR), the evaluation of its performance is essential for designing more complex analog circuits and systems.

Transistor sizing		
n-type differential gain stage		
Description	Type	W/L [µm/µm]
M1, M2	N	2000/20
M3, M4	P	2000/20
p-type differential gain stage		
Description	Type	W/L [µm/µm]
M1, M2	P	2000/20
M3, M4	N	2000/20

Table 2.9. Transistor sizing of both n-type and p-type single stage differential amplifier with current mirror active load.

Transistor sizing of both differential amplifier versions are reporter in Table 2.9; n-type and p-type organic transistors are the same in both cases, each transistor has a multi-finger structure with four channels and an aspect ratio of 2000 µm / 20 µm.

Layout picture and photograph of differential amplifier are shown in Fig. 2.48. The layout exploits only two metal layers for connections. It was arranged to improve transistor matching for both differential pair and current mirror.

Both differential amplifiers were tested on foil and in air at ambient temperature/pressure condition; dc measurements were carried out using a semiconductor parameter analyzer.

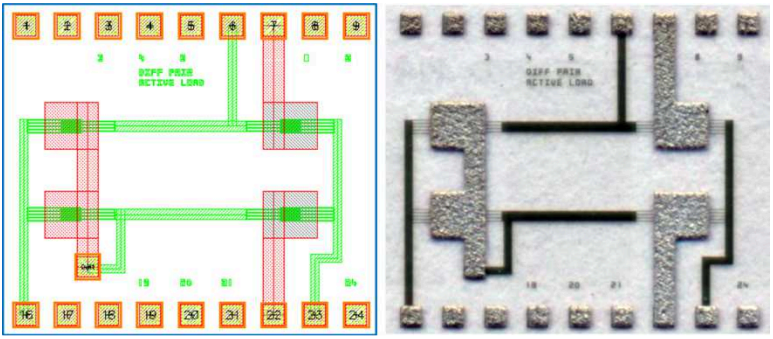


Fig. 2.48. Layout picture and photograph of the p-type differential amplifier with current mirror active load.

For both amplifiers power supply was set to 50 V and the output short circuit current was measured at two different bias currents (i.e. IB = 2 µA and 4 µA) while the differential input signal was swept from -40 V to 40 V, as shown in Fig. 2.49 and Fig. 2.50 for the n-type and p-type differential amplifier, respectively. The transconductance values of differential pair were calculated. For the n-type differential pair its value was 0.1 µA/V and 0.14 µA/V for a bias current of 2 µA and 4 µA, respectively. Instead, for the p-type one its value was 0.13 µA/V and 0.2 µA/V for a bias current of 2 µA and 4 µA, respectively.

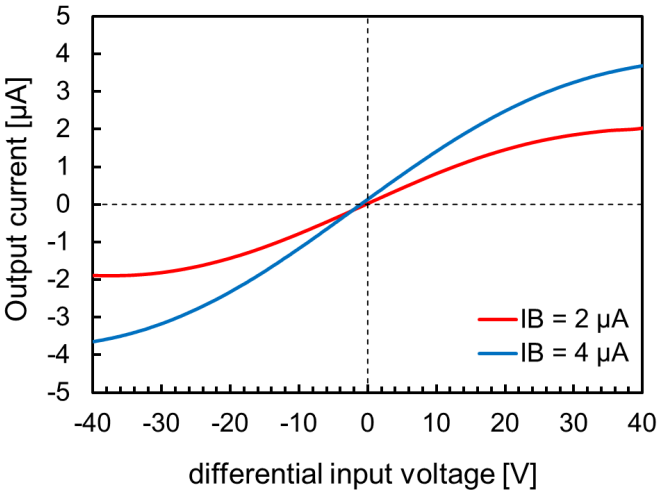


Fig. 2.49. Short-circuit output current of the single stage n-type differential amplifier with current mirror active load.

An input offset voltage of 0.5 V and 4.75 V was measured for the p-type and n-type differential amplifier, respectively. As well-known, the offset voltage in differential amplifier is mainly due to the transistor threshold voltage mismatch. The n-type differential amplifier has shown a lower offset voltage compared to the p-type one since in the adopted technology the threshold voltage variation of p-type OTFT is much higher than n-type one.

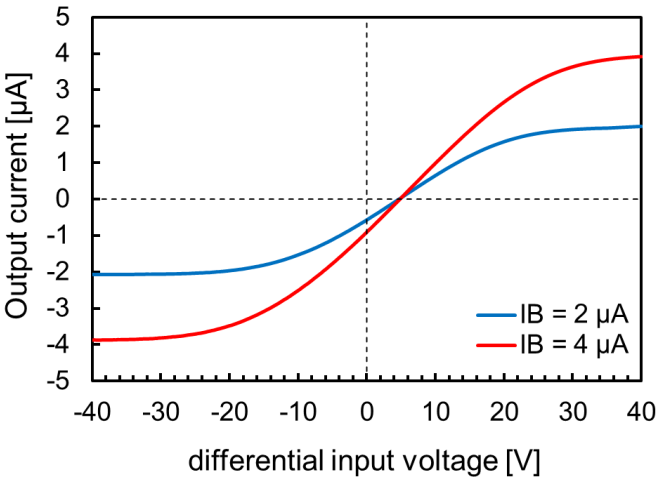


Fig. 2.50. Short-circuit output current of the single p-type differential amplifier with current mirror active load.

The voltage gain of both differential amplifiers was also assessed; it varies in a range between 17 dB - 20 dB and

21 dB – 24 dB for the n-type and p-type differential amplifier, respectively. The measured voltage gain of p-type differential amplifier is higher compared to the n-type one since the p-type OTFTs, with the same channel width, show a higher transconductance value thanks to its better charge carrier mobility.

2.3.6 Rectifier and envelope detector

2.3.6.1 Description

One of the main driver applications in the field of organic electronic is the radio frequency identification (RFID) tag at 13.56-MHz. A key building block of an organic RFID is the rectifier, whose main function is to convert the RF power to a dc in order to supply the whole tag circuits. The rectifier performance is a bottleneck for the overall application due to the high operating frequency and low rectification efficiency. Indeed, working at frequencies above few megahertz is very challenging for organic TFTs (OTFT) since mobility typically does not exceed 0.5-1 cm^2/V s, [28 - 29]. Moreover, the high threshold voltage of OTFTs greatly impacts the rectifier power conversion efficiency (PCE).

The rectifier in its straightforward topology consists of a diode connected in series to a storage capacitor. State-of-the-art organic diodes adopt either vertical Schottky device or

diode-connected OTFT. The former provides the best performance in terms of operating frequency thanks to a very short vertical thickness of the organic semiconductor layer. On the other hand, the latter is preferred when the rectifying diode have to be embedded in a complete RFID system. But the performance of shortened gate-drain OTFT is affected by the larger lateral channel length [30].

In this work, the capability of a simple diode-connected OTFT with an external capacitor was experimentally explored. To take advantage of better mobility, a p-type transistor was preferred. A minimum transistor length of 10 µm was used for a better frequency behavior and the transistor width was set to 36000 µm. A storage capacitor of 100 nF was used. The adopted configuration can be also useful to evaluate the behavior as an envelope detector.

2.3.6.2 Measurement results

The adopted measurement setup for the rectifier characterization is shown in Fig. 2.51. Measurements were carried out on foil by means of a probe station. The rectifier was tested in air at ambient temperature/pressure conditions. The output voltage was measured by means of a semiconductor parameter analyzer.

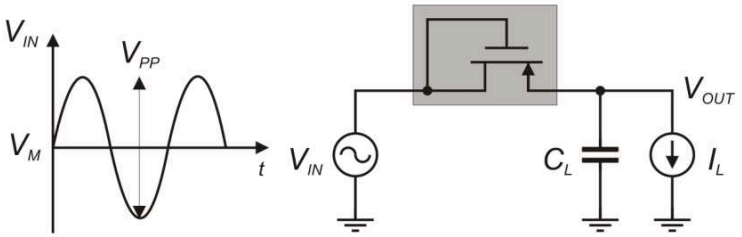


Fig. 2.51. Measurement setup of the rectifier/envelope detector.

The proposed setup was preferred to a traditional resistive load configuration since it allows characterization for different input signal amplitudes at a constant load current (I_L). The rectifier performance was also explored at different input frequencies.

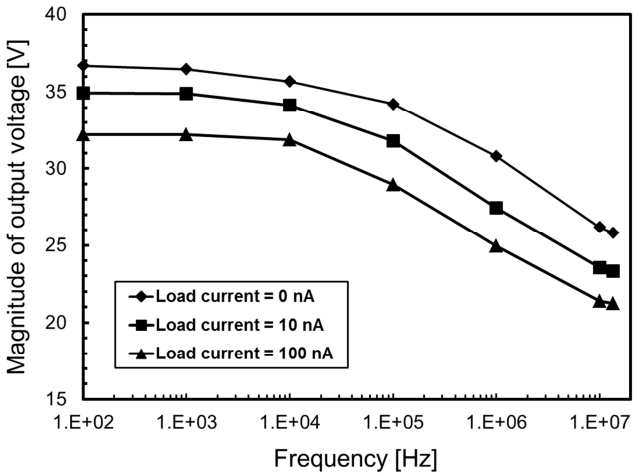


Fig. 2.52. Rectifier output voltage as a function of input frequency at different load currents.

Fig. 2.52 shows the measured output voltage of the rectifier at different frequencies (i.e., 100 Hz, 13.56 MHz) and load currents (i.e., 0 nA to 100 nA). It is apparent how the rectifier performance degrades by increasing frequency, regardless of the load current. A corner frequency of around 10 kHz can be estimated, above which a significant drop of the rectified voltage is experienced.

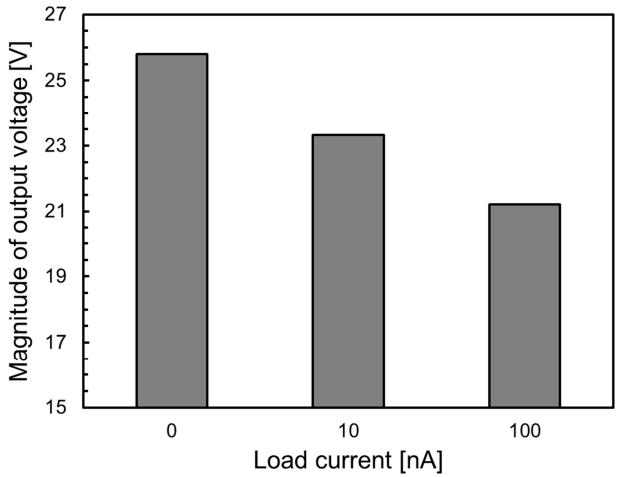


Fig. 2.53. Rectifier output voltage as a function of load currents at 13.56-MHz input frequency.

To better evaluate the rectifier performance at 13.56 MHz, the measured output voltage for three different values of load current (i.e., I_L = 0 A, 10 nA, 100 nA) is depicted in Fig. 2.53. By comparing with the open-circuit condition, rectified

voltage drops as low as 10% and 18% were measured at 10 nA and 100 nA load currents, respectively. For both reported measurements of Figs. 2.52 and 2.53 the input signal adopts V_M and V_{PP} of -25 V and 30 V, respectively.

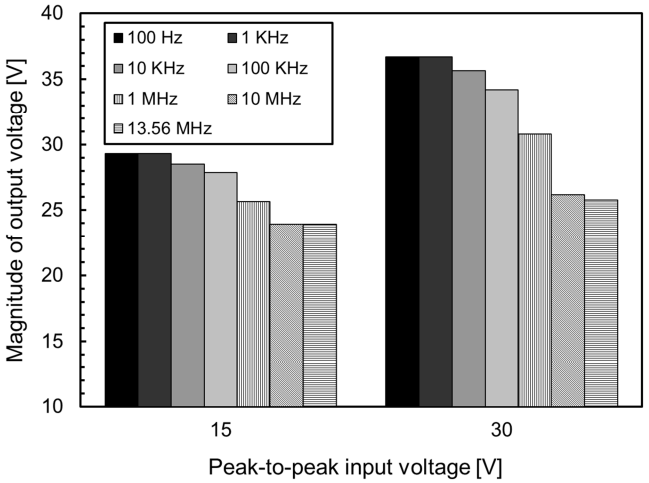


Fig. 2.54. Rectifier output voltage as a function of input signal amplitudes for different input frequencies.

The frequency capability of the rectifier is further explored in Fig. 2.54 that shows the rectifier output voltage at two different V_{PP} (i.e., 15 V and 30 V) at open-circuit condition (i.e., $I_L = 0$ A).

Finally, the robustness and reliability of the adopted organic p-type TFT was evaluated by comparing the dc characteristics before and after the large-signal ac

measurements. Fig. 2.55 shows that no appreciable degradation of the TFT is produced.

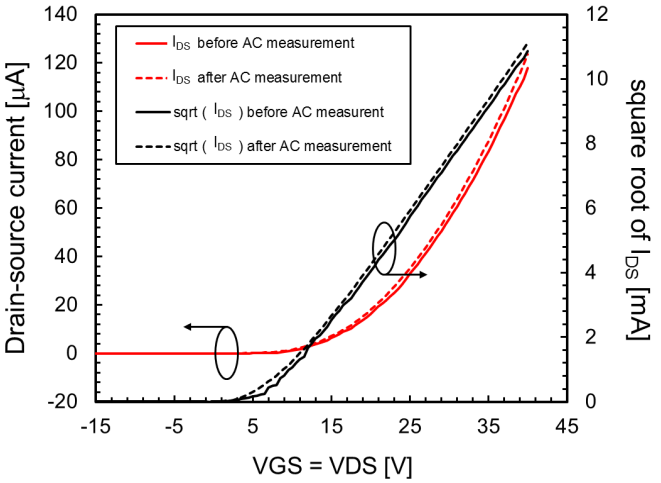


Fig. 2.55. Diode dc characteristics before and after large-signal ac measurements.

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Chapter 3

3.1 Introduction

For enabling the integration of complete systems such as analog filters, analog-to-digital and digital-to-analog converters [1-3], sensor interface [4], temperature and pressure sensors [5-7] and wireless communication interface [8-10] a feasibility study of more complex analog building blocks was done to understand limitations and proper design strategies for the adopted complementary organic technology on flexible substrate.

In particular, this chapter presents the design and the experimental results of a single-stage folded-cascode transconductance amplifier, stacked-mirror and 2-stage high gain OTAs as well as of a switched-capacitor comparator.

3.2 Single-stage folded-cascode amplifier

3.2.1 Description

A single-stage folded-cascode transconductance amplifier was designed and measured, whose circuit schematic is shown in Fig. 3.1.

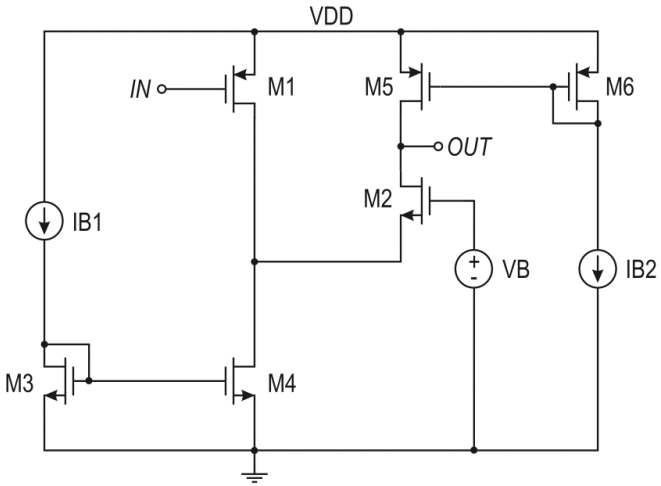

Fig. 3.1. Schematic of the single-stage folded-cascode transconductance amplifier.

The amplifier adopts the single-stage topology employing a simple current mirror load. A p-type input transistor was used to take advantage of its better transconductance value (g_m), due to a higher charge carrier mobility compared to n-type one.

The proposed folded-cascode topology shows an improved voltage gain of about 14 dB compared to the classical common-source configuration since in the adopted complementary organic technology the ratio between the output resistances of the p-type and n-type transistor is approximately 5. The folded arrangement increases voltage

gain while avoiding the excessive output swing reduction of the classical cascode topology.

The cascode topology also greatly reduce the Miller amplification effect of the gate-drain capacitance of transistor M1, which is highly detrimental in this technology since gate-drain and gate-source capacitance are of the same order of magnitude. Miller effect strongly limits the amplifier gain-bandwidth-product (GBW).

To simulate the frequency response and to analyze the stability of the folded-cascode amplifier, additional capacitors were added to the dc transistor model at schematic level to take into account the parasitic effect between gate and source/drain terminals (i.e., C_{gs} and C_{gd}). The capacitor values were estimated by using the overall size of the gate layer and the nominal capacitance density of 20 pF/mm^2, assuming that the overall capacitance (when the OTFT is in "on-state") is equally divided between source and drain terminals.

Transistor sizing and the estimated parasitic capacitances are reported in Table 3.1.

The amplifier was simulated by setting the supply voltage at 50 V and the bias currents, IB1 and IB2, at 4 μA and 2 μA, respectively. The gate voltage, VB, of M2 was set to 35 V that allows obtaining an output voltage swing as high as 15 V,

while preserving the operation of M4 that is far from saturation.

Transistor sizing – Folded-cascode amplifier			
Description	Type	W/L [µm/µm]	C_{GS}=C_{GD} [pF]
M1	P	2000/20	16
M2	N	2000/20	16
M3, M4	N	4000/20	18
M5, M6	P	2000/20	16

Table 3.1. Transistor sizing and parasitic capacitances of the single-stage folded-cascode transconductance amplifier.

Supply voltage (VDD), bias voltage (VB) and bias currents (IB1 and IB2) are externally set for a more exhaustive characterization.

The simulated open-loop dc gain is 44 dB for a supply voltage of 50 V. The nominal current consumption is 10 µA.

In the adopted amplifier topology, dominant pole compensation is exploited. The simulated gain-bandwidth product is slightly above 1 kHz with a phase margin of 56 degree.

The layout picture and photograph of the amplifier are shown in Fig. 3.2 and 3.3, respectively. The amplifier size is 11 x 10.5 mm^2

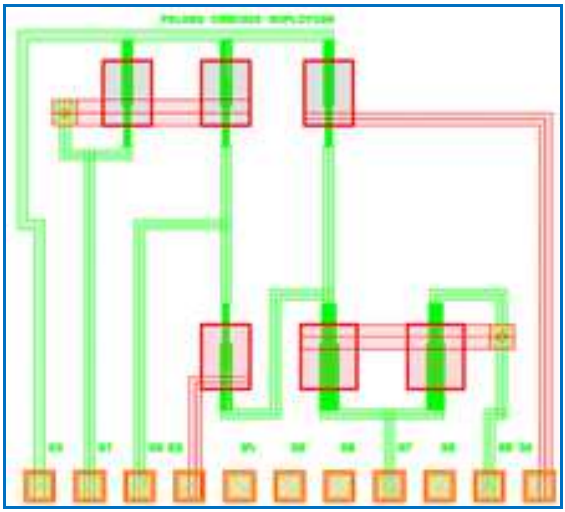

Fig. 3.2. Layout picture of the single-stage folded-cascode transconductance amplifier.

Layout was carried out by exploiting only two metal layers for connections. It was arranged for improving transistor matching in current mirrors while reducing the parasitic capacitances on critical circuit nodes responsible for non-dominant poles.

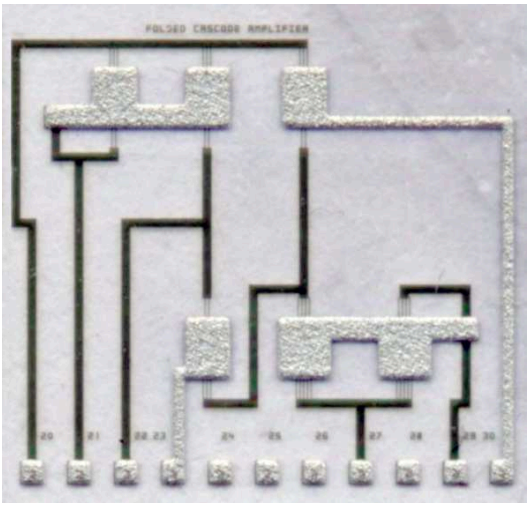

Fig. 3.3. Photograph of the single-stage folded-cascode transconductance amplifier.

3.1.2 Measurement results

The single-stage folded-cascode amplifier was tested on foil by using a dedicated probe card. All measurements were performed in air at ambient temperature/pressure conditions.

The input-output dc characteristic and output short-circuit current are shown in Fig. 3.4. They were measured by using a semiconductor parameter analyzer and setting the supply voltage at 50 V. The measured current consumption was 13 µA.

An open-loop dc gain of about 40 dB was calculated from the input-output dc characteristic. The measured value is very

close to the simulated one (44 dB). The measured output short-circuit current provides an estimation of the transconductance value of transistor M1, which is as high as 0.6 µA/V.

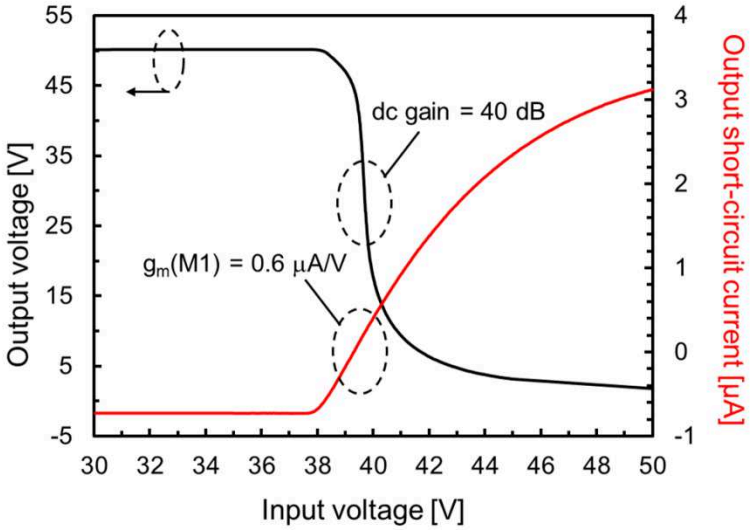

Fig.3.4. Measured input-output dc characteristic and short-circuit output current of the single-stage folded-cascode amplifier.

The folded-cascode amplifier was also fully characterized in the frequency domain using the measurement setup shown in Fig. 3.5.

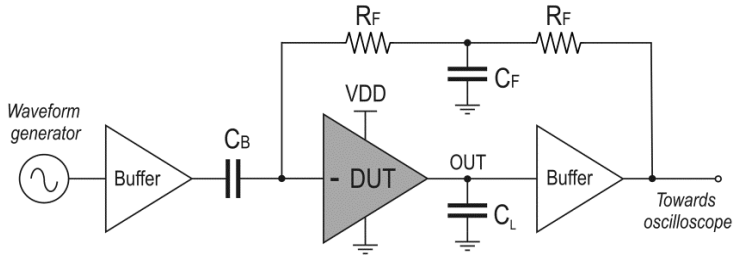

Fig. 3.5.Measurement setup for open-loop gain characterization.

Since the output resistance of the folded-cascode amplifier is of the same order of magnitude of the oscilloscope input resistance, a high voltage output buffer (Texas Instruments OPA445) was used to avoid the loading effects during the experimental characterization. The external R_F-C_F-R_F (i.e., R_F = 1 MΩ, C_F = 11 μF) network was adopted for stabilizing the dc operating point of the amplifier while opening the loop for the ac signal.

As already mentioned, the folded-cascode amplifier exploits the dominant pole compensation at the high impedance output node. The parasitic load capacitance (C_L) due both probe card and output buffer was measured to be around 60 pF and is suitable for the amplifier stability.

The measured open-loop gain and phase are shown in Fig. 3.6. The gain-bandwidth product (GBW) and phase margin (PM) are 1.5 kHz and 58 degree, respectively. The

measured amplifier performance is close to the expected results.

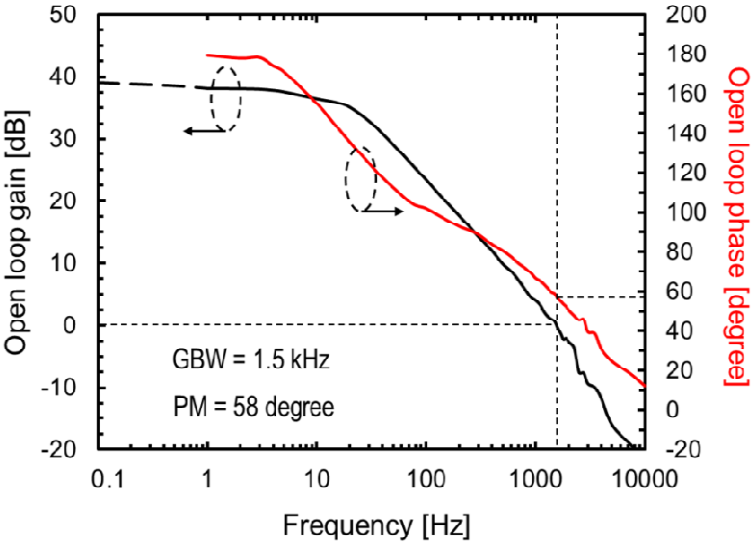

Fig. 3.6. Measured open-loop gain and phase of the single-stage folded-cascode amplifier.

The folded-cascode amplifier was also tested in inverting closed-loop configuration using two external resistors (i.e., R_1 = 12 kΩ and R_2 = 46 kΩ).

Fig. 3.7 shows the measured frequency response in closed-loop condition. As expected, the measured closed-loop gain was 11.6 dB, while the -3 dB bandwidth was about 400 Hz. It

is worth noting that the GBW product value was further confirmed by closed-loop measurements.

These achievements represent the best-in-class results of complementary organic thin-film transistor technologies on flexible substrate.

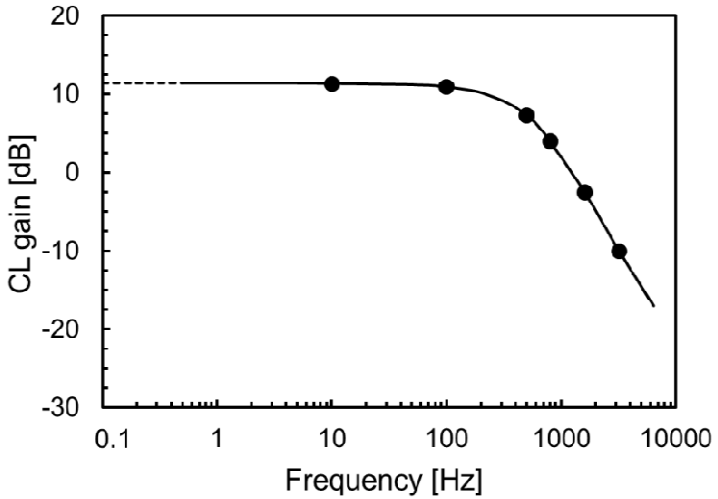

Fig. 3.7 Measured closed-loop gain in inverting configuration of the folded-cascode amplifier

The total harmonic distortion (THD) performance of the amplifier was also evaluated. THD was measured at 20 Hz by connecting the amplifier in inverting closed-loop configuration with a small-signal gain of 11.6 dB and using two external resistors.

The measured THD as a function of the output signal amplitude is shown in Fig. 3.8.

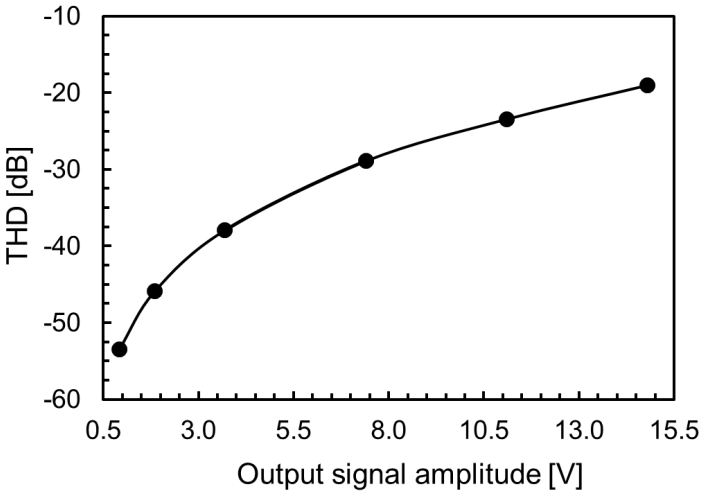

Fig. 3.8. Measured THD of the single-stage folded-cascode amplifier.

3.3 Cascode stacked-mirror and 2-stage high-gain OTAs

3.3.1 Description

Two high-gain OTAs adopting classical topologies, i.e. a cascode stacked-mirror and 2-stage OTA, were also designed. The amplifier schematics are shown in Fig. 3.9 and 3.10, respectively.

Miller compensation is needed for the 2-stage OTA to guarantee closed-loop stability. Instead, stacked-mirror OTA are compensated through a shunt capacitor at the output node (i.e., dominant-pole compensation). However, proper design of the compensation networks requires both a reliable transistor model including parasitic capacitances and repeatable process. To overcome these drawbacks and to increase the degrees of freedom during the characterization phase, both OTAs were compensated using external components.

The amplifiers design was carried out by taking advantage of dedicated transistor models in which additional gate-source and gate-drain parasitic capacitances were added. The parasitic capacitances were estimated as already described in paragraph 3.2.1.

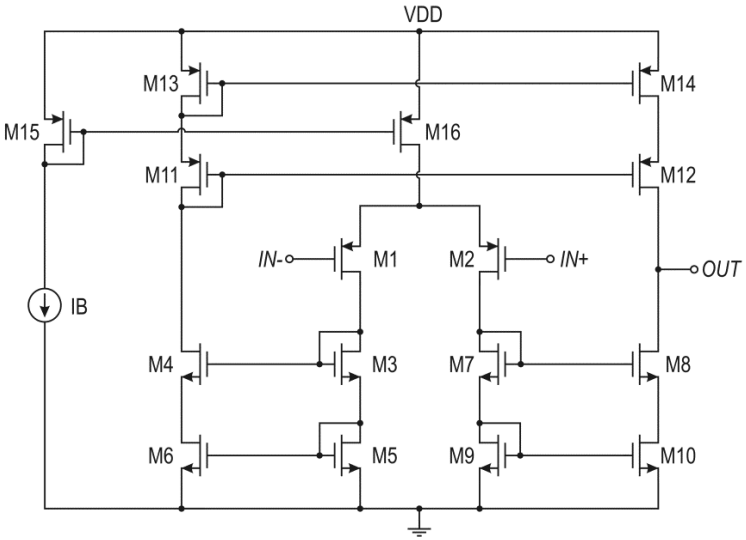

Fig. 3.9. Schematic of the cascode stacked-mirror OTA.

Transistor sizing – Cascode stacked-mirror OTA			
Description	Type	W/L [µm/µm]	C_{GS}=C_{GD} [pF]
M1, M2	P	4000/20	18
M3, M4, M5, M6	N	2000/20	16
M7, M8, M9, M10	N	2000/20	16
M11, M12, M13, M14	P	2000/20	16
M15, M16	P	4000/20	18

Table 3.2. Transistor sizing and parasitic capacitances of the cascode stacked-mirror OTA.

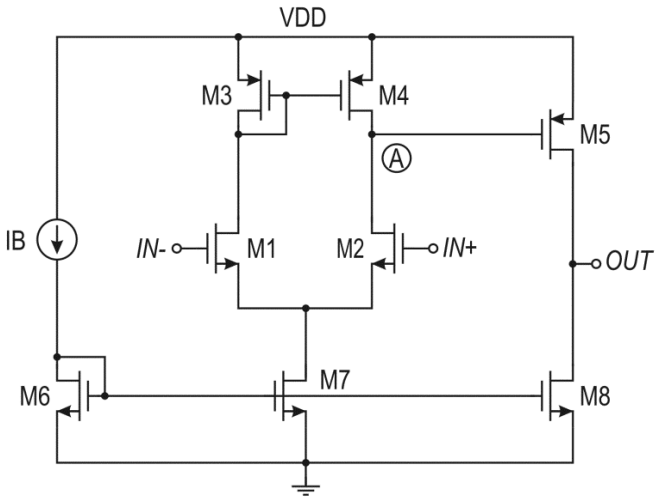

Fig. 3.10. Schematic of the 2-stage OTA.

Transistor sizing – 2-stage OTA			
Description	Type	W/L [µm/µm]	C_{GS}=C_{GD} [pF]
M1, M2	N	2000/20	16
M3, M4	P	1000/20	15
M5	P	4000/20	18
M6	N	4000/20	18
M7	N	2000/20	16
M8	N	1000/20	15

Table 3.3. Transistor sizing and parasitic capacitances of the 2-stage OTA.

Transistor sizing and the estimated parasitic capacitances of both cascode stacked-mirror and 2-stage OTA are reported in Table 3.2 and 3.3, respectively.

Both OTAs exhibit a dc open-loop gain proportional to $(g_m \cdot r_d)^2$ that is as high as 50 dB in the adopted technology. For both OTAs power supply is set to 50 V. The expected current consumptions are 2.5 µA and 7 µA for the stacked-mirror and 2-stage OTA, respectively.

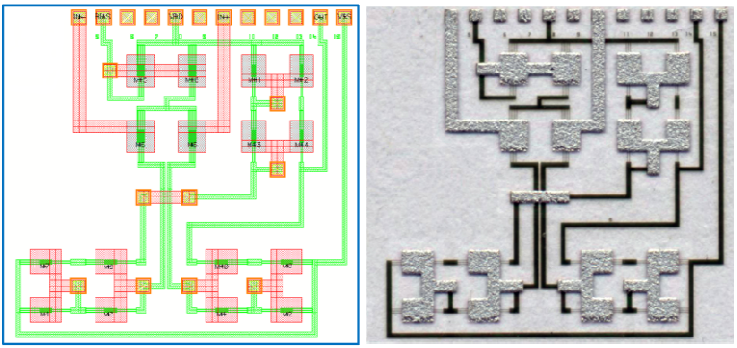

Fig. 3.11. Layout picture and photograph of the cascode stacked-mirror OTA.

Layout pictures and photographs of both OTAs are shown in Figs. 3.11 and 3.12. The amplifier area is 15 x 13.5 mm^2 and 12.5 x 14 mm^2 for the stacked-mirror and 2-stage OTA, respectively. The layouts exploit only two metal layers for interconnections. They were arranged to improve transistor

matching for differential pairs and current mirrors, while reducing the parasitic capacitances on critical circuit nodes responsible for non-dominant poles.

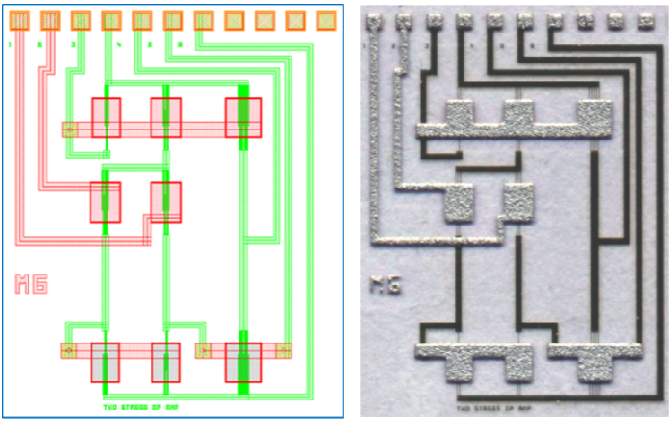

Fig. 3.12. Layout picture and photograph of the 2-stage OTA

3.3.1 Measurement results

Fabricated OTAs were tested on foil by using a dedicated probe-card. All measurements were performed in air at ambient temperature/pressure conditions. The dc characterization was carried out by means of semiconductor parameter analyzer. Supply voltage was set at 50 V for both operational amplifiers and the bias current (IB) was set at 0.5 µA and 1 µA for stacked-mirror and 2-stage OTA,

respectively. The measured current consumption is 1.8 µA and 6.5 µA for stacked-mirror and 2-stage OTA, respectively.

Figs. 3.13 and 3.14 show the dc input-output characteristic and short-circuit output current as a function of input voltage for stacked-mirror and 2-stage OTA, respectively.

For both amplifiers a dc open-loop gain of about 50 dB was calculated from the input-output characteristic.

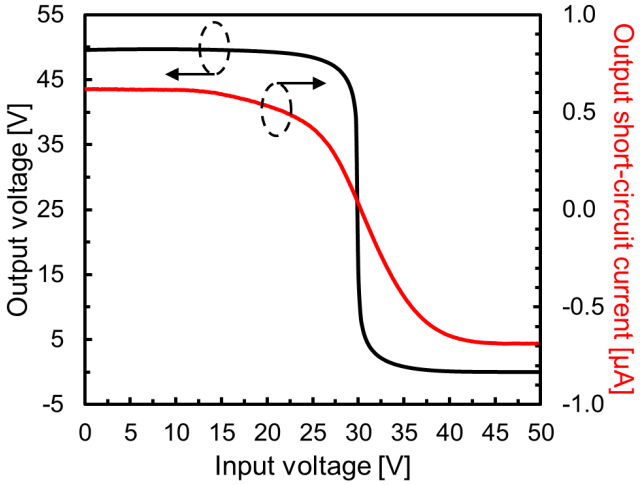

Fig. 3.13. Input-output characteristic and short-circuit output current of the cascode stacked-mirror OTA.

The input offset voltage was measured by connecting OTAs in unit gain configuration and reading the difference between the output voltage and the input common mode

voltage. For the available samples, an input offset voltage of 0.5 V and 4.7 V were measured for stacked-mirror and 2-stage OTA, respectively. Of course, statistical measurements on a large number of samples are needed to accurately evaluate the offset voltage, which is mainly due to transistor threshold voltage mismatches.

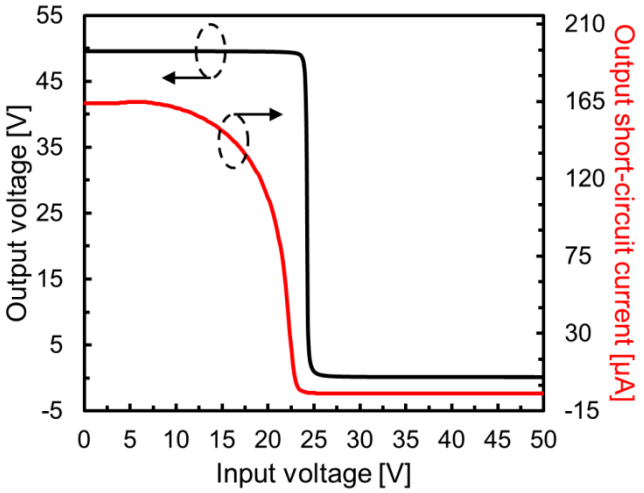

Fig. 3.14. Input-output characteristic and short-circuit output current of the 2-stage OTA.

The short-circuit output currents agree with the expected values. Indeed, the 2-stage OTA can source an output current as high as 165 µA thanks to the current capability of M5, whereas the sinking current is limited by the bias current of

M8 (i.e., around 4.5 µA). Instead, the sink/source current balance of the cascode stacked-mirror OTA (i.e., ±0.65 µA) confirms the good transistor matching in the available sample, which also agrees with the low measured value of the offset voltage. For the stacked-mirror configuration the measured short-circuit output current also provides the transconductance value of differential pair M1-M2, which is about 0.09 µA/V.

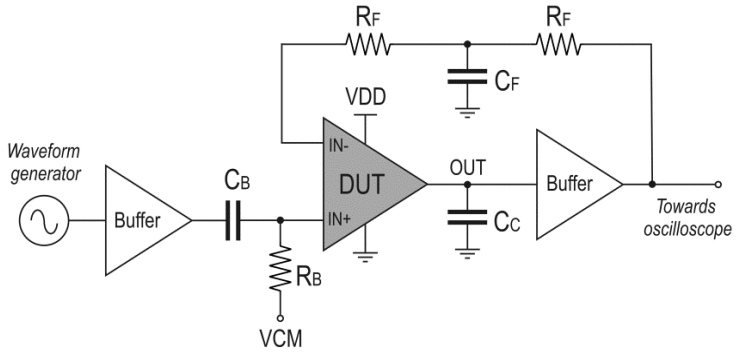

Fig. 3.15. Measurement setup for open-loop gain characterization of the cascode stacked-mirror OTA.

The cascode stacked-mirror OTA was also fully characterized in both frequency and time domain by means of open-loop gain and step-response measurements, using the experimental setups shown in Figs. 3.15 and 3.16, respectively.

In both measurement setups a high voltage output buffer (Texas Instruments OPA445) was used to avoid the loading effects introduced by both the lab equipment and the external components. The parasitic load capacitance at the output of the amplifier due to both probe-card and output buffer was measured to be around 60 pF. This parasitic load was taken into account in the design of the amplifier compensation network.

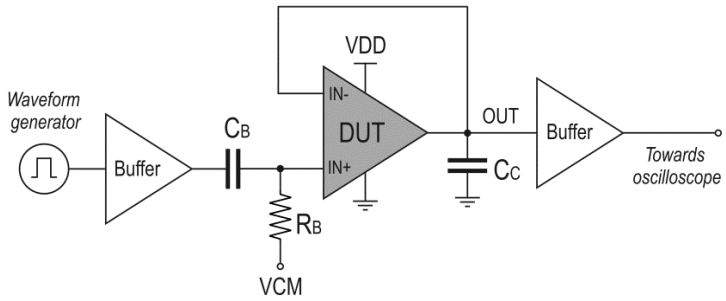

Fig. 3.16. Measurement setup for step-response characterization of the cascode stacked-mirror OTA.

In the open-loop gain measurement setup, an external network R_F-C_F-R_F (i.e., R_F = 1 MΩ and C_F = 11 μF) was used. It allows the dc operating point of the amplifier to be properly set while opening the loop for the ac signal.

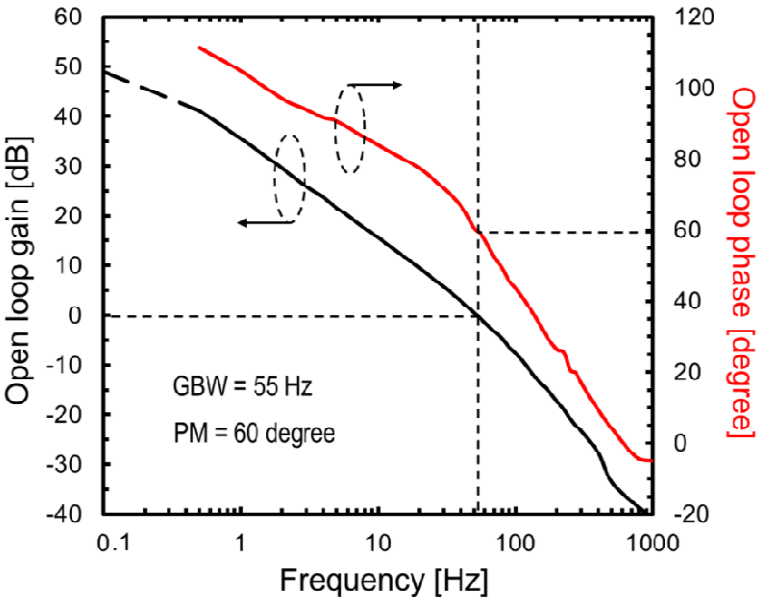

Fig. 3.17. Measured open-loop gain and phase of the cascode stacked-mirror OTA.

The cascode stacked-mirror OTA was externally compensated by putting a capacitance C_C of about 150 pF at the output node in addition to the parasitic load capacitance. As clearly shown by the open-loop characterization reported in Fig. 3.17, GBW and phase margin (PM) of the stacked-mirror OTA are 55 Hz and 60 degree, respectively.

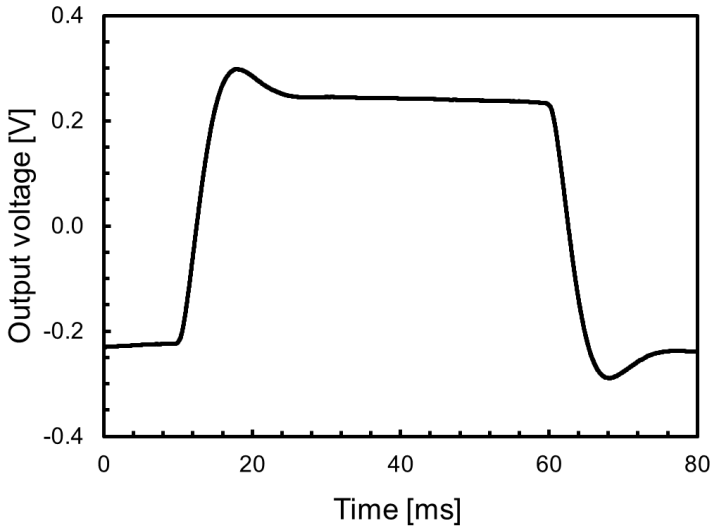

Fig. 3.18. Measured step-response of the cascode stacked-mirror OTA.

The step-response of the compensated stacked-mirror OTA was also measured by using the experimental setup shown in Fig. 3.16. A square-wave input signal with peak-to-peak amplitude of 500 mV and frequency of 10 Hz was used to evaluate the amplifier step-response. The measured step-response is shown in Fig. 3.16. The 1 % setting time is 13.5 ms.

The step-response of the 2-stage OTA was measured using the experimental setup shown in Fig. 3.19. Also in this case a

high voltage output buffer was used to avoid loading effects. The measured load parasitic capacitance (C_L) was 60 pF.

A square-wave input signal with peak-to-peak amplitude of 500 mV and frequency of 10 Hz was used to evaluate the step-response of the 2-stage OTA.

The step-response of the 2-stage OTA is shown in Fig. 3.20, where C_C and R_C of the external Miller compensation network were set to 270 pF and 2 MΩ, respectively.

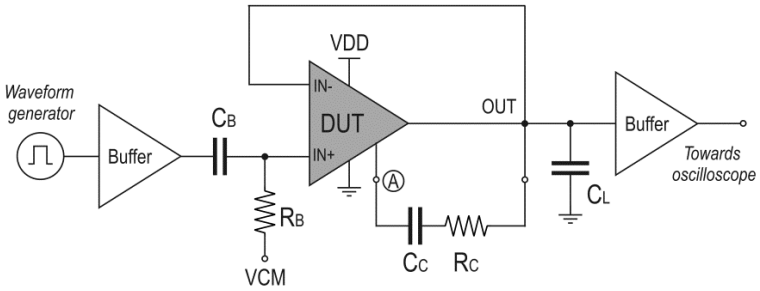

Fig. 3.19. Measurement setup for step-response characterization of the 2-stage OTA.

A GBW of 75 Hz and a phase margin of 70 degree were calculated from the step-response of the 2-stage OTA. Moreover, the measured 1 % settling time of the 2-stage OTA is 12.5 ms.

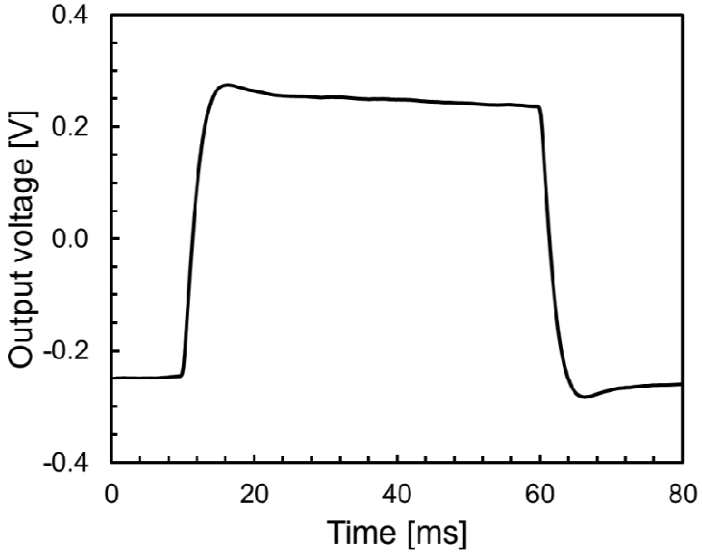

Fig. 3.20. Measured step-response of the 2-stage OTA.

The open-loop gain of the 2-stage OTA was not measured due to stability problems of the characterization setup at low frequencies.

Both OTAs were also tested in inverting closed-loop configuration by using two external resistors (i.e., $R_1 = 12\ k\Omega$ and $R_2 = 46\ k\Omega$). The measured frequency response in closed loop conditions of both OTAs is shown in Fig. 3.21.

As expected, the closed-loop gain was 11.6 dB for both amplifiers, while the -3 dB bandwidth was about 15 Hz and 20 Hz for the stacked-mirror and 2-stage OTA, respectively.

It is worth mentioning that the -3 dB closed-loop bandwidth for both amplifiers closely agrees with the measured gain-bandwidth-product.

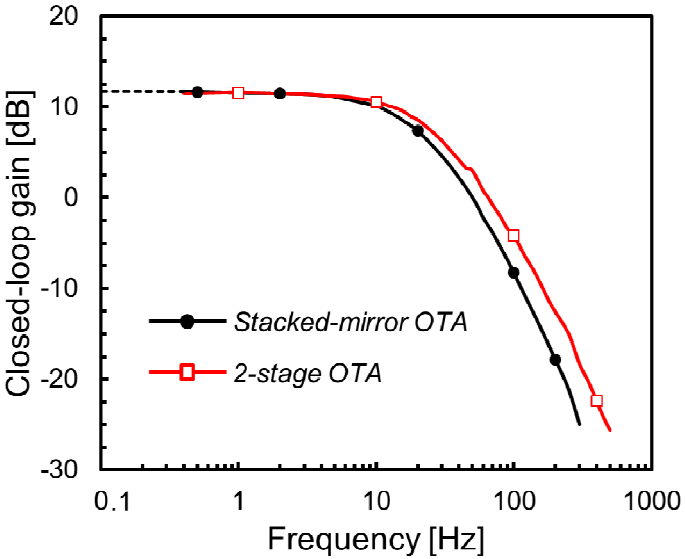

Fig. 3.21. Measured closed-loop gain of both OTAs in inverting closed-loop configuration.

Fig. 3.22 also gives an insight into the THD performance measured at 2 Hz of both OTA topologies.

The amplifiers were tested in inverting closed-loop configuration with a small-signal gain equal to 11.6 dB. The measured THD is lower than -50 dB for output signal amplitude up to 9 V and 3.5 V for the stacked-mirror and 2-

stage OTA, respectively. As expected, the 2-stage OTA shows a better THD behavior than the stacked-mirror OTA in the overall range of the output signal amplitude. Indeed, the THD of the stacked-mirror topology is affected by a lower output swing.

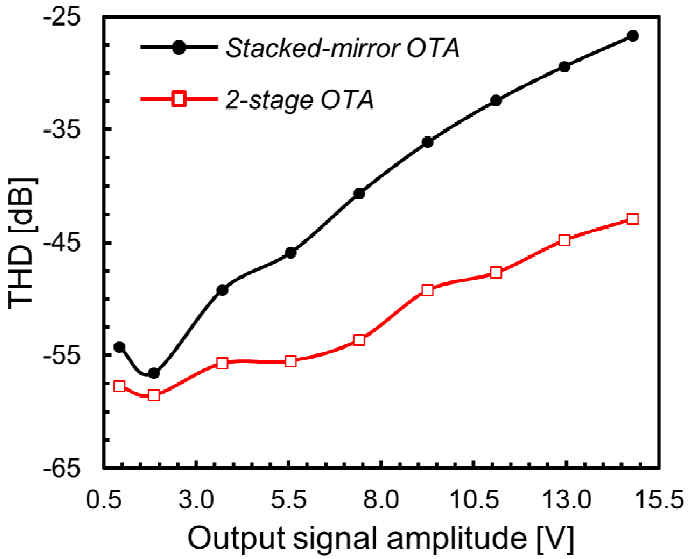

Fig. 3.22. Measured THD at 2 Hz in inverting configuration of both OTAs.

Table 3.4 summarizes and compares the main measured performance of the two amplifier topologies.

		Stacked-mirror OTA	**2-stage OTA**
Supply voltage VDD [V]		50	50
Bias current IB [µA]		0.5	1
Current consumption [µA]		1.8	6.5
Open-loop gain [dB]		49	51
Input offset voltage [V]		0.5	4.7
GBW [Hz]		55	75
PM [degree]		60	70
Settling time 1% [ms] 0.5 V_{PP} input signal		13.5	12.5
THD [dB] @ 2 Hz CL gain=11.6dB	V_{OUT}=1.8V	-57	-59
	V_{OUT}=14.8V	-27	-43
Size [mm x mm]		15 x 13.5	12.5 x 14

Table 3.4. Summary of the measured performance.

3.4 Switched-capacitor comparator

3.4.1 Description

Organic semiconductor technology typically exhibits high process mismatches and low transconductance values. In this contest, the switched-capacitor design technique is suitable since it allows compensation of both offset and operational amplifier finite gain to be easily achieved.

The feasibility of switched-capacitor circuits was also investigated by designing a switched-capacitor comparator.

The folded-cascode amplifier, presented in paragraph 3.22, was exploited in the switched-capacitor (SC) comparator by adding another gain stage in order to increase the voltage gain. Simplified and detailed circuit schematics of the SC comparator are shown in Figs. 3.23 and 3.24, respectively.

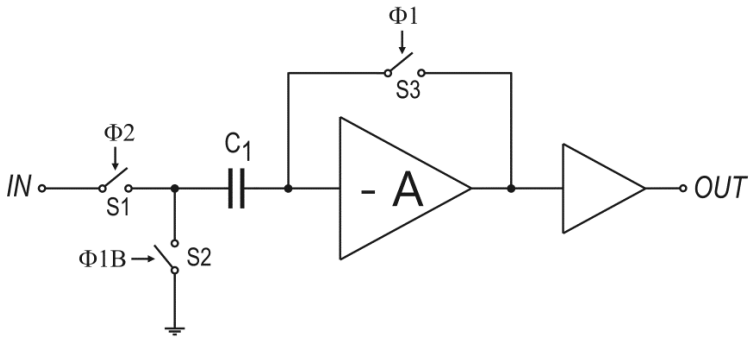

Fig. 3.23. Simplified schematic of the SC comparator.

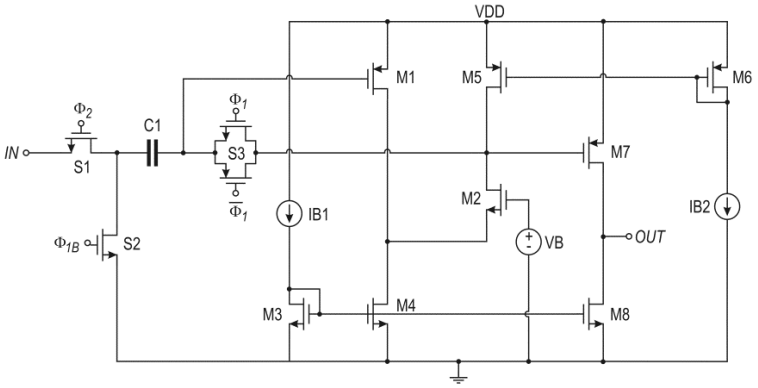

Fig. 3.24. Detailed schematic of the SC comparator.

Transistor sizing along with the estimated parasitic capacitances are reported in Table 3.5.

The circuits adopts an input capacitor, C_1, of 25 pF and three TFT switches, S1, S2, and S3, which are driven by the control signals shown in Fig. 3.25.

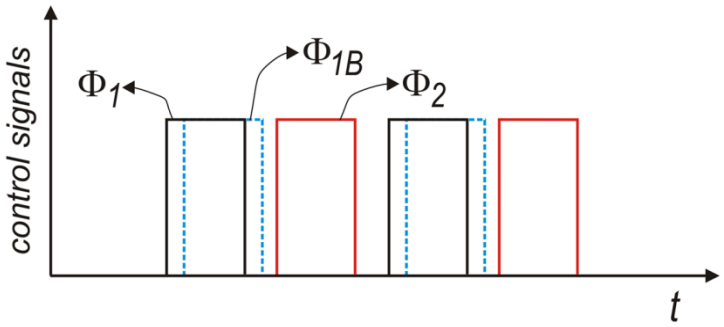

Fig. 3.25. Control signals of the SC comparator.

Transistor sizing – SC comparator			
Description	Type	W/L [µm/µm]	C_{GS}=C_{GD} [pF]
M1	P	2000/20	16
M2	N	2000/20	16
M3, M4	N	4000/20	18
M5, M6	P	2000/20	16
M7	P	2000/20	16
M8	N	4000/20	18
S1, S2	N	500/20	14
S3	N/P	2 x 500/20	2 x 14

Table 3.5. Transistor sizing and parasitic capacitances of the SC comparator.

Control signals Φ_1 and Φ_2 are disoverlapped, while Φ_{1B} is a delayed replica of Φ_1. This delay is required in order to avoid charge injection effects of switch S2 into the gate terminal of M1, which give rise to a detrimental input offset. Thanks to Φ_{1B}, when switch S3 opens, switch S2 is closed thus no charge can be injected into the amplifier's input node.

A similar charge injection effect takes place also for the switch S3, but it is greatly reduced by using a complementary switch topology along with a proper switch sizing. To this aim, the parasitic capacitances of switch S3 are matched by using equal size for both p-type and n-type TFTs. It is worth noting that differently from silicon CMOS technology, the

clock-feedthrough phenomena is here dominant over channel-charge injection due to the large values of gate-source and gate-drain parasitic capacitances (i.e., around 15 pF). For this reason, traditional rule for the W/L ratio between p-type and n-type TFTs in the complementary switch (i.e., equal to g_m ratio) for the compensation of the channel injection cannot be adopted. Indeed, it would produce a large difference in the parasitic capacitances and hence a high charge injection due to the clock-feedthrough effect.

Finally, a current-controlled inverter gain stage, M7-M8, was added at the output of folded-cascode amplifier to increase the voltage gain, as shown in Figs. 3.23 and 3.24.

Layout picture and circuit photograph are shown in Fig. 3.26. The circuit size is 19 x 12.2 mm^2. The layout exploits only two metal layers for connections. It was arranged to improve transistor matching for current mirrors while reducing parasitic capacitances on critical circuit nodes.

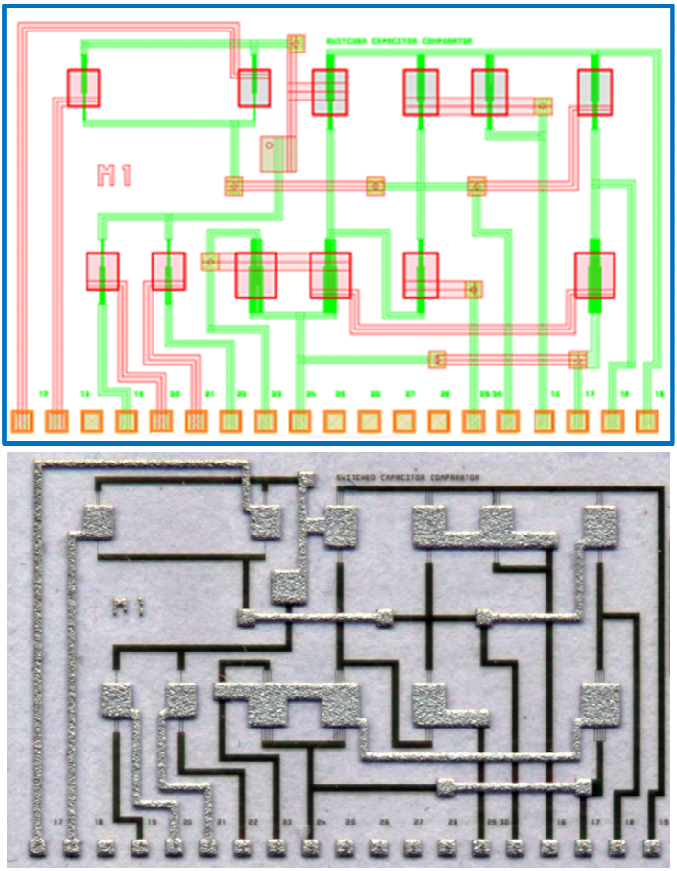

Fig. 3.26. Layout picture and photograph of the SC comparator.

3.4.2 Measurement results

The fabricated SC comparator was tested on foil by using a dedicated probe-card. Measurements were performed in air at ambient temperature/pressure conditions. Supply voltage and control signals were set at 50 V.

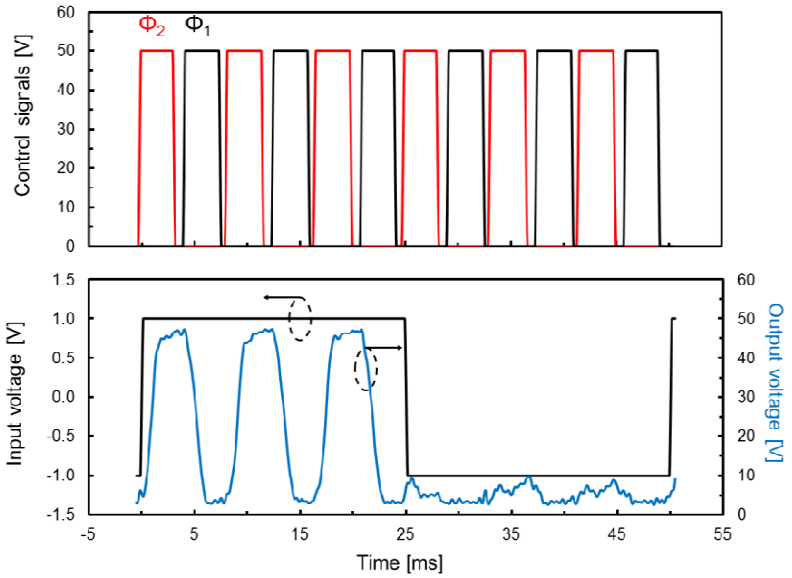

Fig. 3.27. Switched-capacitor comparator measurement for an input signal frequency of 20 Hz and a sampling frequency of 120 Hz.

The SC comparator was tested by using 5-to-50 Hz square wave input signals with a duty cycle of 50 % and sample frequency (f_S) from 100 Hz to 150 Hz with a minimum

oversampling factor of 3. For lower values of the sampling frequency, the comparator functionality was appreciably affected by the off-mode switch leakage.

Fig. 3.27 shows the measured output signal of the SC comparator (blue curve) when a square wave input signal with an amplitude of 1 V and a frequency of 20 Hz was applied. The sampling frequency was set to120 Hz.

For the sake of clarity, control signals Φ_1 (reset phase) and Φ_2 (sampling phase) are also reported for reference in Fig. 3.27.

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Chapter 4

4.1 Organic light sensor

4.1.1 Description

A fully organic light sensor was designed and fabricated using a complementary organic technology on flexible substrate (see par. 2.2) developed by CEA-LITEN [1-4].

The circuit schematic of the light sensor is shown in Fig. 4.1.

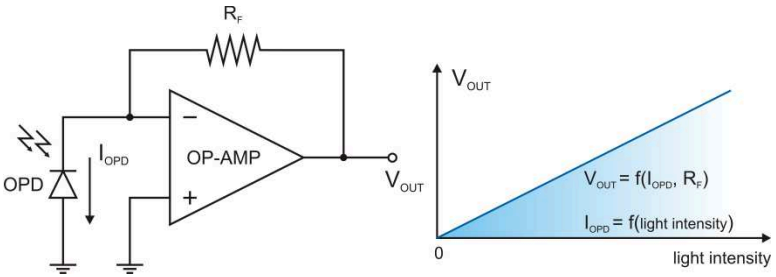

Fig. 4.1. Circuit schematic of the organic light sensor.

It is made up of two basic building blocks, i.e. an organic photodiode (OPD) and an operational amplifier (OP-AMP), which is suitable for signal conditioning. Basically, the

operational amplifier is used in a current to voltage feedback configuration to convert the photodiode current into an output voltage. The circuit allows a linear detection of the incident light intensity. Indeed, the operational amplifier output voltage is proportional to the OPD photocurrent ($V_{OUT} = R_F$ x I_{OPD}).

A classical 2-stage operational transconductance amplifier (OTA) topology was adopted. The amplifier was designed and fabricated by using the latest CEA technology process flow. Its circuit schematic is shown in Fig. 4.2.

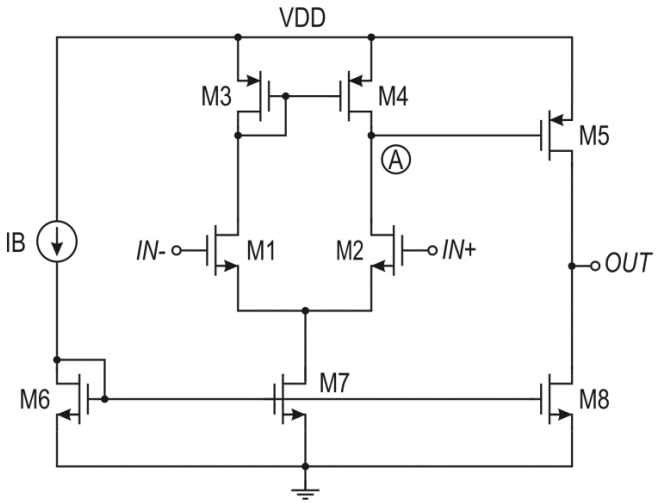

Fig. 4.2. Schematic of the 2-stage OTA.

The n-type input differential pair (M1-M2) guarantees a lower input offset voltage since in the adopted technology the

threshold voltage dispersion of the n-type transistor is lower than the p-type one [1]. Moreover, the p-type common-source output gain stage (M5) is able to provide the required OPD current (I_{OPD}) that flows in the feedback resistor (R_F). The maximum output current provided by the operational amplifier can be set by properly sizing M5. Input offset voltage is an important performance parameter of the operational amplifier, which affects the reverse bias voltage of the OPD. To minimize the systematic input offset, the bias circuit was designed according to the following customary rule:

$$\frac{I_{D4}}{\left(\frac{W}{L}\right)_4} = \frac{I_{D5}}{\left(\frac{W}{L}\right)_5} \tag{4.1}$$

The operational amplifier simulations were carried out by taking advantage of a dedicated dc transistor model [5], which was properly modified to take into account the transistor's parasitic capacitances (i.e., C_{GD} and C_{GS}). The method used for estimating the parasitic capacitances was already described in paragraph 3.2.

The operational amplifier was compensated exploiting Miller compensation technique. An estimation of the output load capacitance of 30 pF was considered, which is mainly

due to the parasitic capacitance introduced by the flexible flat cable and external components (i.e., PCB and output buffer) used for characterization.

Amplifier transistor sizing along with the estimated transistor's parasitic capacitances are reported in Table 4.1.

For a supply voltage of 60 V and for the nominal values of the Miller resistance and capacitance of 2 MΩ and 270 pF, respectively, the simulated dc gain, gain-bandwidth-product and phase margin of the operational amplifier are: 60 dB, 100 Hz and 75 degree. The expected current consumption is 7 µA.

Transistor sizing – OP-AMP			
Description	Type	W/L [µm/µm]	C_{GS}=C_{GD} [pF]
M1, M2	N	2000/20	16
M3, M4	P	1000/20	15
M5	P	4000/20	18
M6	N	4000/20	18
M7	N	2000/20	16
M8	N	1000/20	15

Table 4.1. Transistor sizing and parasitic capacitances of the OP-AMP designed for the integration of organic light sensor.

The performance of the operational amplifier in closed-loop configuration (i.e., light sensor configuration) was also

evaluated by using an equivalent circuit for the organic photodiode (OPD) (i.e., a current generator and the equivalent OPD parasitic capacitance), and a feedback resistor (R_F), as shown in Fig. 4.3.

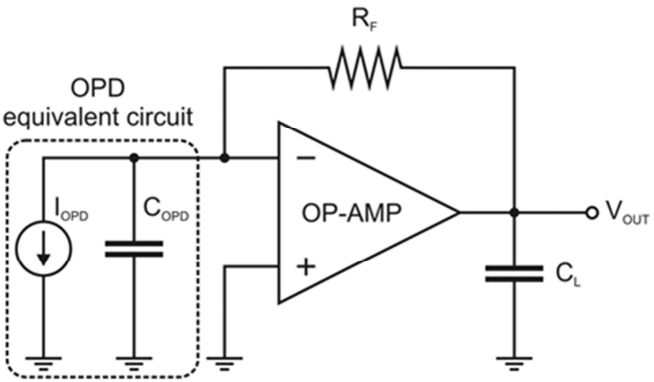

Fig. 4.3. Circuit schematic of the light sensor with the OPD equivalent circuit.

A one-pixel photodiode was used for the organic light sensor. In a maximum illumination condition, it typically draws a current between 1 µA to 3 µA and exhibits a parasitic capacitance between 500 pF to 1.5 nF with a reverse bias voltage between 2 V to 5 V. A feedback resistor (R_F) of 680 kΩ was used to achieve an output voltage variation between 0.7 V to 2 V at the light sensor output for a maximum OPD current (I_{OPD}) variation between 1 µA to 3 µA. Due to the large OPD parasitic capacitance (C_{OPD}) and

feedback resistance (R_F), the operational amplifier needs to be properly compensated to provide the light sensor with a stable behavior. The amplifier compensation network was set with $R_C = 2\ M\Omega$ and $C_C = 400\ pF$. The simulated dc gain, gain-bandwidth-product and phase margin of the whole light sensor are 60 dB, 57 Hz and 60 degree, respectively. Table 4.2 summarizes the performance of the stand-alone operational amplifier and light sensor, respectively.

Description	OP-AMP	Light sensor
Nominal supply voltage [V]	60	60
Bias current [µA]	1	1
Current consumption [µA]	7	7
Input common mode [V]	33	33
Output load capacitance [pF]	30	30
Miller capacitance [pF]	270	400
Miller resistance [MΩ]	2	2
DC gain [dB]	60	60
Gain-bandwidth-product [Hz]	100	57
Phase margin [degree]	75	60

Note:

1. *One-pixel organic photodiode exhibits a parasitic capacitance (C_{OPD}) between 500 pF to 1.5 nF in maximum illumination condition.*
2. *A feedback resistance (R_F) of 680 kΩ was used.*

Table 4.2. Summary of the simulated performance of the OP-AMP and light sensor.

The organic photodiode cross-section and layout bottom view are shown in Fig. 4.4. A first version of the OPD, reported in [6], was built on glass substrate.

Since the operational amplifier was fabricated using a complementary organic technology on flexible substrate (PEN), a technology transfer was put in place to fabricate the OPD on the same substrate thus enabling the integration of a fully organic flexible light sensor.

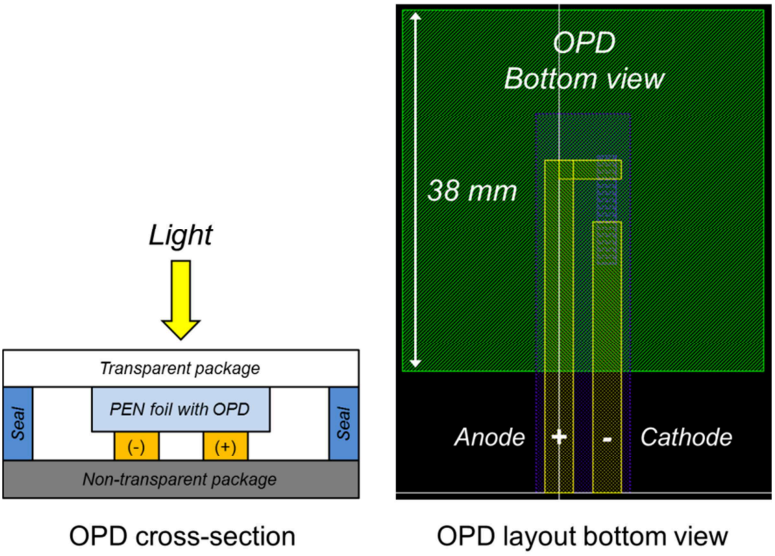

Fig. 4.4. Cross-section and layout bottom view of the encapsulated organic photodiode.

In order to guarantee a correct debugging of each light sensor building block, four test chips with different integration levels were fabricated.

A stand-alone operational amplifier was implemented to evaluate and compare its performance with the simulated ones. The operational amplifier layout, shown in Fig. 4.5, was arranged by exploiting only two metal layers for interconnections and improving the transistor matching for differential pair and current mirrors.

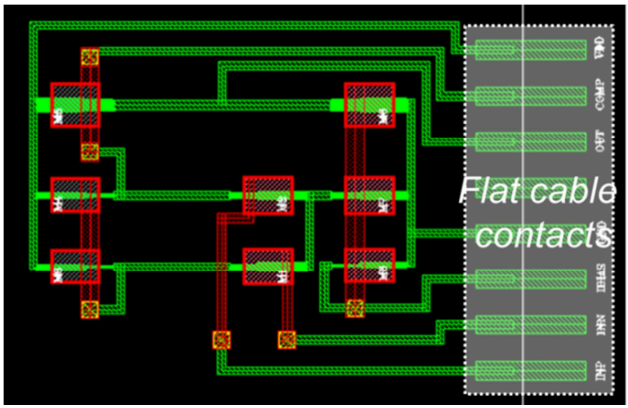

Fig. 4.5. Layout picture of the stand-alone OP-AMP.

To simplify interfacing with the lab instruments during circuit characterization, a flexible flat cable was used for connecting operational amplifier terminals (i.e., bias current

(IB), supply voltage (VDD), ground (GND), non-inverting (IN+) and inverting (IN-) input, output (OUT) and the intermediate node (A) for compensation) to a dedicated PCB in which the external compensation network can be soldered. Anisotropic conductive glue was used for connecting the flexible flat cable to the amplifier. Size of the operational amplifier is 15 mm x 15 mm.

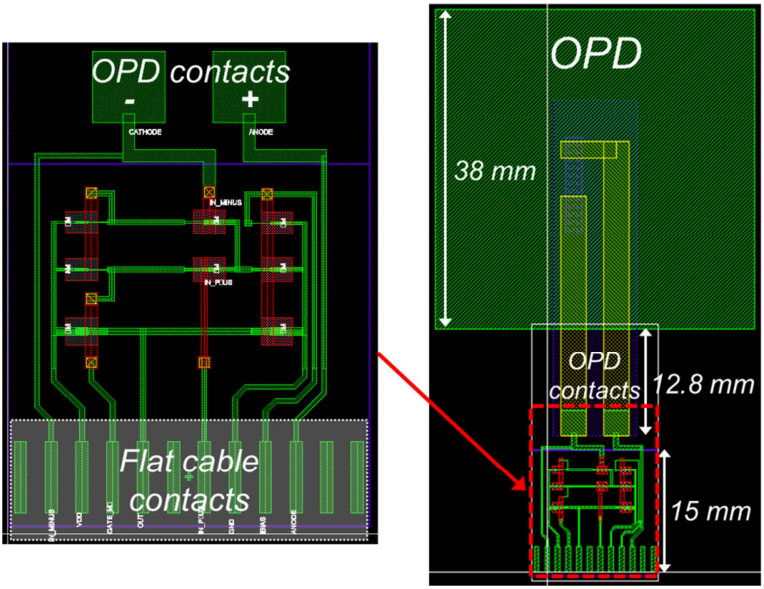

Fig. 4.6. Layout pictures of the foil-to-foil organic light sensor.

A basic version of the organic light sensor was implemented by exploiting the foil-to-foil assembly. In this

version, the operational amplifier and the organic photodiode were fabricated in two different foils and then they were connected together by using anisotropic conductive glue. As shown in Fig. 4.6, the amplifier layout was optimized to guarantee a correct assembly with OPD and the flexible flat cable. Also in this case, passive components (i.e., amplifier compensation network and feedback resistor of the light sensor) are external and soldered on a dedicated PCB. The size of the foil-to-foil light sensor is 15 mm x 30 mm.

Two different versions of fully integrated organic light sensor (i.e., on-foil implementation) were designed. In both light sensor versions operational amplifier, OPD and passive components (i.e., resistors and capacitor) were fabricated on the same foil. The only different between the two versions concerns the implementation of the passive components. Indeed, in the first one passive components with nominal values were integrated, instead in the second one reconfigurable passive components were implemented that can be properly tuned by using the laser cutting of metal layers (only two metal layers were used for interconnections, i.e. source/drain and gate layers). The range of variation of each reconfigurable passive component is reported in Table 4.3. The adopted technology process features MIM capacitor, with a specific capacitance of 20 pF/mm^2, and

carbon-ink resistor with a sheet resistance of 35 kΩ/sq. They were extensively used in light sensor for integrating passive components.

Description	Min	Max	Step
Feedback resistor (R_F)	90 kΩ	990 kΩ	90 kΩ
Miller resistance (R_C)	500 kΩ	5.5 MΩ	500 kΩ
Miller capacitance (C_C)	80 pF	960 pF	80 pF

Table 4.3. Range of variation of each reconfigurable passive component.

The layout pictures of both versions of fully-integrated light sensor are shown in Figs. 4.7 and 4.8. Layouts were arranged exploiting only two metal layers for interconnections, and improving matching of both transistors and passive components.

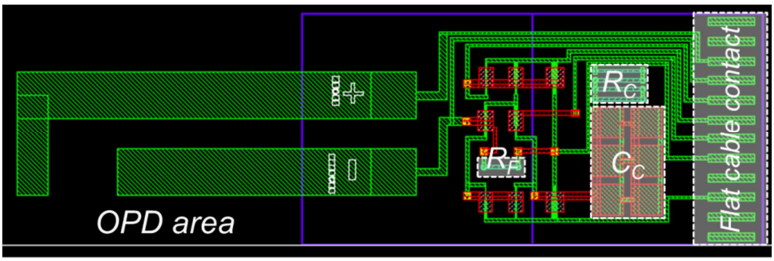

Fig. 4.7. Layout picture of the on-foil light sensor with integrated nominal passive components.

As shown in Figs. 4.7 and 4.8, a suitable integration and contact area for OPD and for flexible flat cable have to be guaranteed. A dedicated PCB connected to light sensor by means of flexible flat cable is used for testing. The light sensor sizes, without the OPD, are (15 mm x 37 mm) and (15 mm x 45 mm) for the first and the second version, respectively.

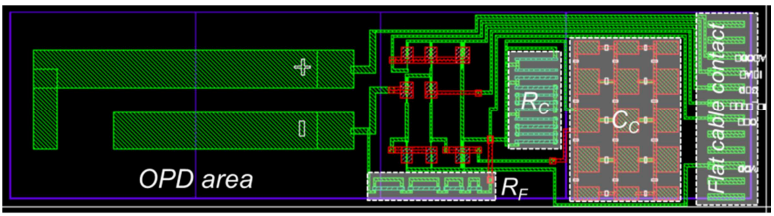

Fig. 4.8. Layout picture of the on-foil light sensor with integrated reconfigurable passive components.

4.1.2 Measurement results

4.1.2.1 Organic photodiode

The photograph of the organic photodiode (OPD) on flexible plastic substrate is shown in Fig. 4.9. It was tested in air at ambient temperature/pressure condition. The current-voltage (I-V) characteristic of the OPD was measured at different light intensity with the sensor inside a black box and using a semiconductor parameter analyzer (Agilent 4156B). Halogen lamp (PHILIPS Brilliant Line 50 W, 12 V, 36°) was used as light source for illuminating the OPD. The distance between light source and OPD was set at 45 cm during characterization. The intensity of incident light was measured using ISO-TECH ILM 1335 lux meter.

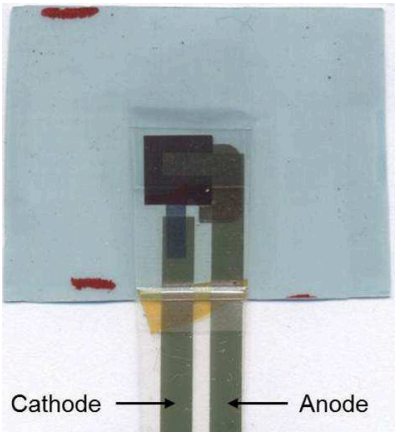

Fig. 4.9. Photograph of the organic photodiode fabricated on flexible plastic substrate.

The measured I-V characteristics of the OPD at different light intensity, i.e. from dark (0 lx) to maximum illumination condition (11400 lx) are shown in Fig. 4.10.

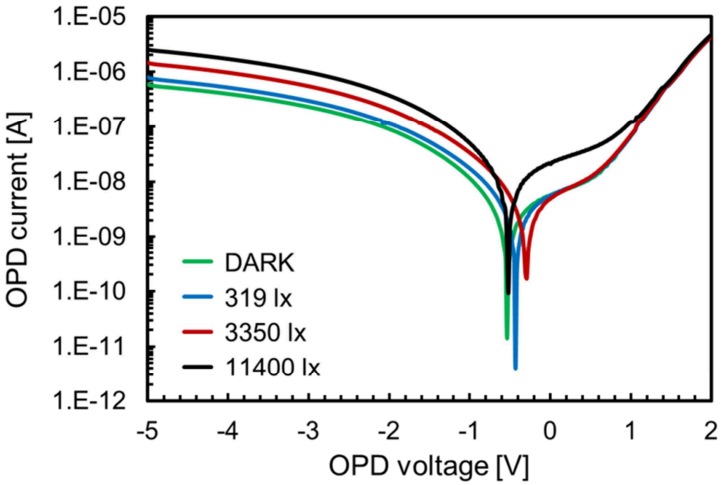

Fig. 4.10. I-V characteristics of the OPD measured at different intensity of incident light.

In order to evaluate the degradation effects of the OPD performance, the I-V characteristics were also measured after 12 hours using the same testing setup and conditions of the first measurement. The measured I-V characteristics of the OPD after 12 hours are shown in Fig. 4.11.

A very slight reduction of the photocurrent was found in the OPD performance. For the sake of clarity, the first and the

second (i.e. after 12 hours) measured I-V characteristics in dark and maximum illumination condition are shown in Fig. 4.12.

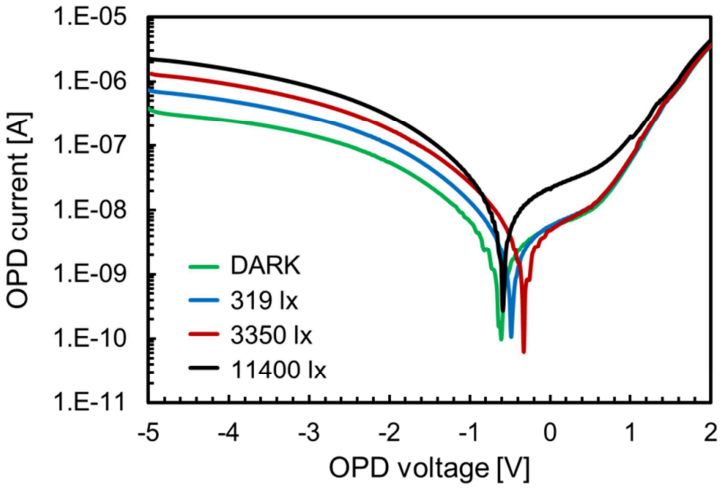

Fig. 4.11. I-V characteristics of the OPD measured at different intensity of incident light after 12 hours from the first measurement.

As can be easily seen from the measured I-V characteristics in Figs. 4.10, 4.11, and 4.12, the organic photodiode have to be reverse-biased to achieve a larger photocurrent variation when moving from dark to maximum illumination condition and hence enabling the detection of a light intensity variations.

The measured OPD current in dark and maximum illumination conditions for two reverse bias voltages (i.e., OPD voltage equal to -2 V and -5 V) are reported in Table 4.4.

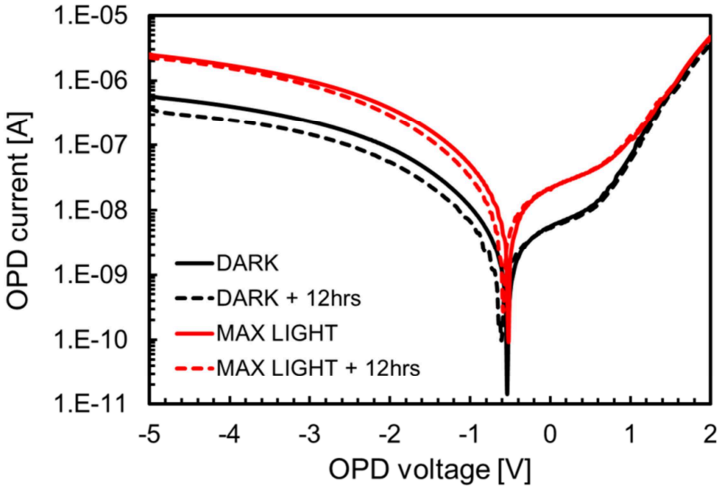

Fig. 4.12. The first and the second (after 12 hours) measured I-V characteristic of the OPD in dark and maximum illumination condition, respectively.

	V_{OPD} = - 2 V		V_{OPD} = - 5 V	
	I_{DARK}	I_{MAX}	I_{DARK}	I_{MAX}
First measure	111 nA	376 nA	800 nA	2.54 µA
Second measure after 12 hours	55 nA	292 nA	383 nA	2.28 µA

Table 4.4. Measured OPD current in dark and maximum illumination condition at two different reverse bias voltages.

The parasitic capacitance of the available OPD sample was measured to be around 1.5 nF in maximum illumination condition.

4.1.2.2 Operational amplifier

The operational amplifier was tested using a dedicated PCB connected to the amplifier by means of a flexible flat cable, as shown in Figs. 4.13 and 4.14.

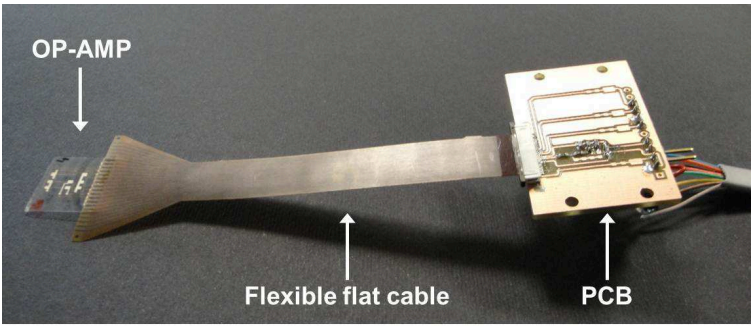

Fig. 4.13. Photograph of the measurement setup adopted for the characterization of the operational amplifier.

The flexible flat cable was glued to the operational amplifier using anisotropic conductive paste. The PCB design was arranged to allow the soldering of the required passive components. The adopted assembly provides an easy interfacing of the operational amplifier with lab instrumentations.

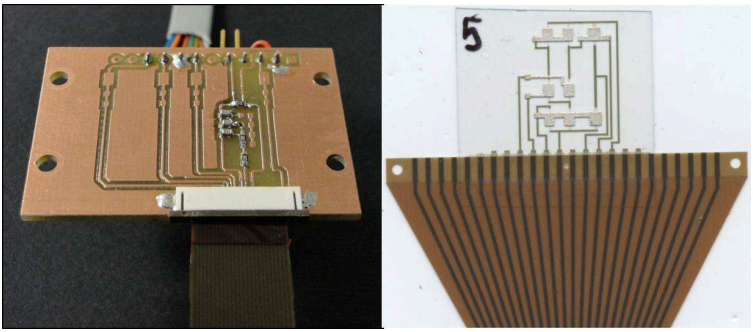

Fig. 4.14. Detailed photograph of the PCB and the operational amplifier glued on flexible flat cable.

All measurements were performed in air at ambient temperature/pressure conditions.

Measurements of the dc input-output characteristic and output short-circuit current of the operational amplifier were carried out in open-loop configuration for three different supply voltages (i.e., 40 V, 50 V and 60 V). The non-inverting input (IN+) was hence set at three common mode bias voltages (i.e., 23 V, 28 V and 33 V) and the inverting input (IN-) was swept from 0 to VDD by using a semiconductor parameter analyzer (Agilent 4156 B). By setting the bias current (IB) was set to 1 µA, the measured current consumption was 6.3 µA.

The measured dc input-output characteristics are shown in Fig. 4.15.

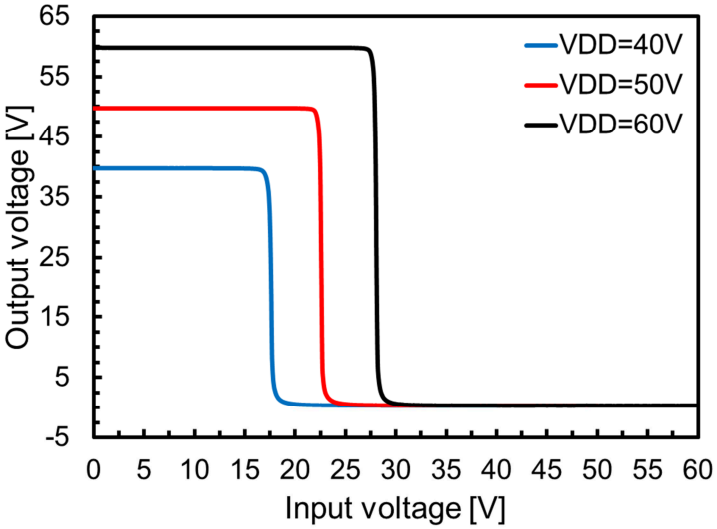

Fig. 4.15. Input-output characteristic of the operational amplifier at three different supply voltages.

The dc open-loop gain at different supply voltages was calculated by differentiating the measured input-output characteristics as shown in Fig. 4.16. It assumes a value of 47 dB, 51 dB and 54 dB at a supply voltage of 40 V, 50 V and 60 V, respectively. Although the measured gain is lower than the simulated one, it is high enough to guarantee accuracy to the light sensor.

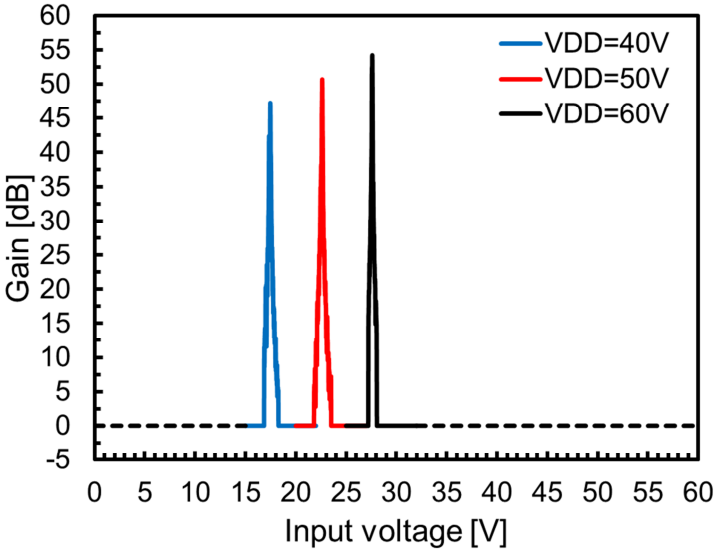

Fig. 4.16. dc open-loop gain of the operational amplifier vs. input voltage for three different supply voltages.

An input offset voltage of 5.6 V was measured by connecting the operational amplifier in unit-gain configuration and by reading the difference between output and input common mode voltage.

The measured output short-circuit currents agree with the expected values. The adopted operational amplifier topology can source a maximum output current that depends on both the aspect ratio (W/L) of the transistor M5 and by the voltage swing at its gate terminal, whereas the sinking current is limited by the bias current of M8.

The measured output short circuit current for three supply voltages (i.e., 40 V, 50 V and 60 V) is shown in Fig. 4.17.

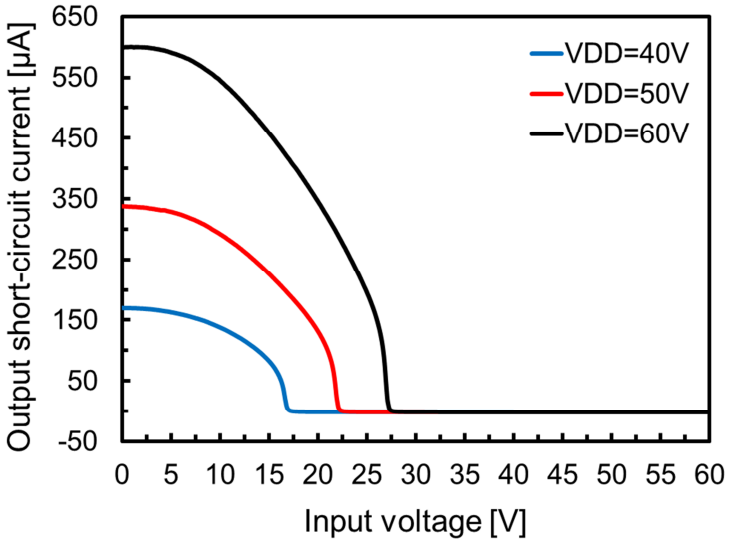

Fig. 4.17. Output short-circuit current vs. input voltage of the operational amplifier at three different supply voltages.

The maximum value of the source current depends on the supply voltage since a higher supply voltage leads to a higher voltage swing at M5 gate terminal (i.e., 170 µA, 337 µA and 600 µA), while the sinking current is limited to 3.5 µA. As expected, amplifier is able to provide the required photocurrent when the light sensor works in maximum illumination conditions.

The operational amplifier was also connected and tested in light sensor configuration (i.e. closed-loop configuration) by including a feedback resistor (R_F) of 680 kΩ and an equivalent OPD parasitic capacitance (C_{OPD}) of 1.5 nF on PCB.

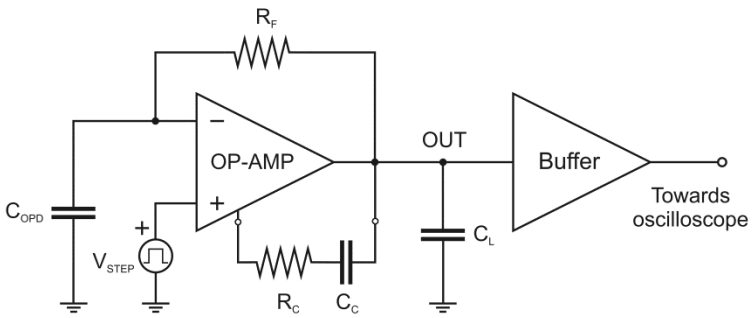

Fig. 4.18. Measurement setup adopted for step-response characterization of the operational amplifier in closed-loop configuration.

To evaluate stability in closed-loop configuration, the operational amplifier was characterized in time domain by means of step-response measurement using the experimental setup shown in Fig. 4.18.

Supply voltage and bias current were set at 60 V and 1 µA, respectively. External Miller compensation network (i.e., R_C = 2 MΩ, C_C = 400 pF) was also included on PCB. The output load parasitic capacitance (C_L) due to the flexible flat

cable, PCB and output buffer was measured to be around 39 pF and it was taken into account in the design of the compensation network. A high voltage output buffer (Texas Instruments OPA 445) was used to avoid the detrimental loading effect of the oscilloscope input impedance. A square-wave signal with peak-to-peak amplitude of 1 V and frequency of 5 Hz was fed to the non-inverting input for evaluating the amplifier step-response.

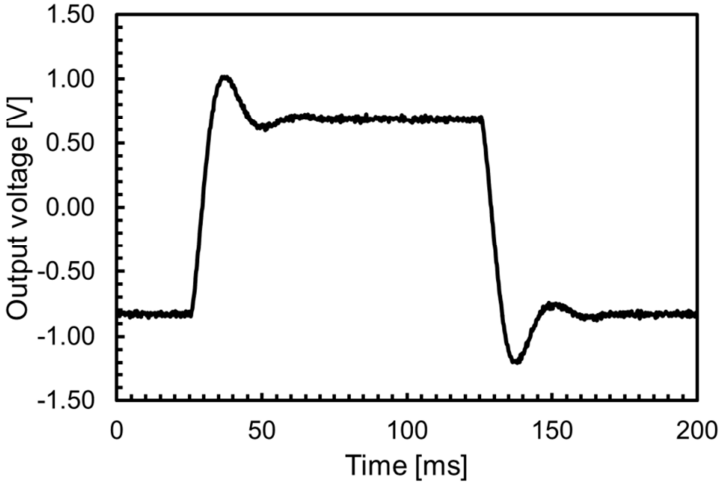

Fig. 4.19. Measured step-response of the operational amplifier in closed-loop configuration (i.e. light sensor configuration).

The measured step-response of the operational amplifier in closed-loop configuration is shown in Fig. 4.19. It demonstrates that stability margin (i.e. phase margin of about

50 degree) was guaranteed thanks to the use of an optimized compensation network. The amplifier gain-bandwidth-product is not a critical requirement since in an ambient light sensor application the incident light intensity is a slowly variable signal.

To further analyze the operational amplifier behavior as light sensor an additional time domain measurement in closed-loop configuration was performed by applying a discrete current ramp made up of ten current steps, i.e. from 0 to 5 µA with a step size of 0.5 µA. The adopted measurement setup is shown in Fig. 4.20.

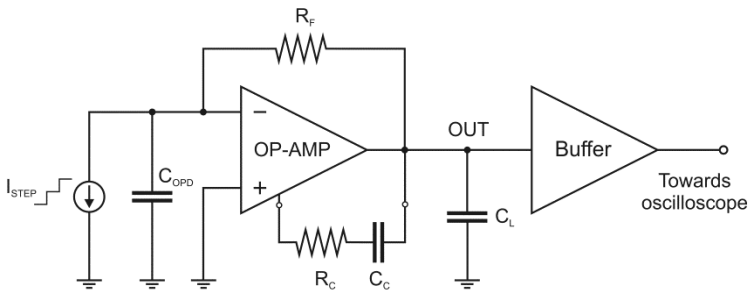

Fig. 4.20. Measurement setup adopted for current step response characterization of the operational amplifier in closed-loop configuration.

The ramp current was accurately generated with a semiconductor parameter analyzer (Agilent 4156B), and the

output voltage was measured using a high voltage output buffer (TI OPA 445) and an oscilloscope.

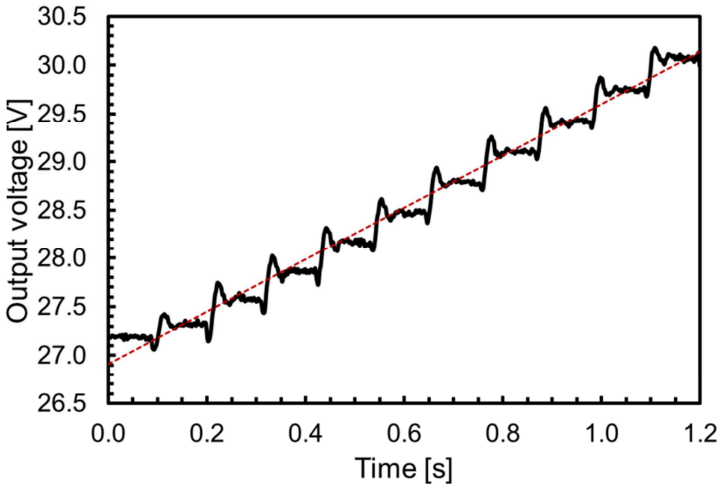

Fig. 4.21. Measured output voltage of the operational amplifier in closed-loop configuration when a discrete current ramp is applied at the input.

The measured output voltage is shown in Fig. 4.21. The output voltage variation confirms the system stability since it can be seen as the system step-response to a consecutive ten input current steps. As expected, the operational amplifier works as a linear current to voltage converter. Indeed, by calculating the extrapolation curve of the measured output voltage (i.e. red curve in Fig. 4.21), the operational amplifier

basically provides an output voltage variation proportional to the input current.

4.1.2.3 Foil-to-foil light sensor

The foil-to-foil light sensor was fully tested. As already described, the organic photodiode in this light sensor version is glued to the operational amplifier using an anisotropic conductive paste and all passive components are externally soldered on PCB. As in the case of the stand-alone operational amplifier, the light sensor is glued to a flexible flat cable and connected to the PCB through it, see Figs. 4.22 and 4.23.

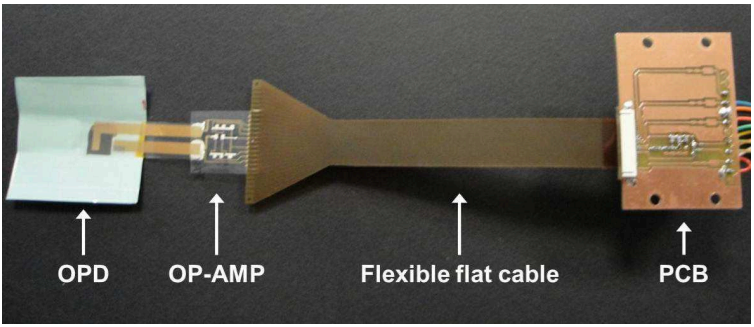

Fig. 4.22. Photograph of the measurement setup adopted for the foil-to-foil light sensor characterization.

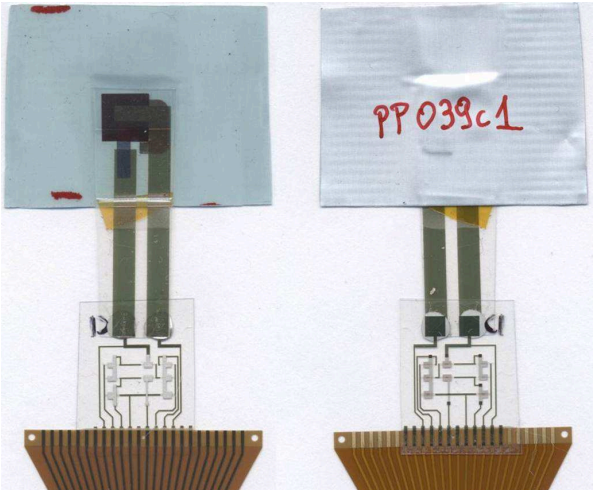

Fig. 4.23. Photograph of the foil-to-foil light sensor.

The light sensor was measured in air at ambient temperature/pressure conditions inside to a black box according to the measurement setup shown in Figs. 4.22 and 4.24.

A semiconductor parameter analyzer (Agilent 4156 B) was employed to measure all voltages and currents required during the light sensor characterization.

The supply voltage and bias current were set to 60 V and 1 µA, respectively. The measured current consumption was about 7.5 µA. Feedback resistor (R_F) of 680 kΩ and Miller compensation resistance (R_C) and capacitance (C_C) of 2 MΩ

and 400 pF, respectively, were soldered on PCB. The load capacitance (C_L) due to both flexible flat cable and PCB was measured to be around 25 pF.

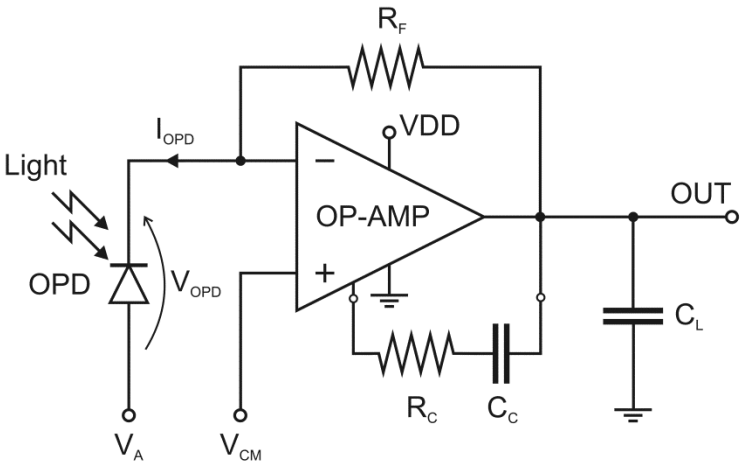

Fig. 4.24. Measurement setup adopted for the light sensor characterization.

Since the organic photodiode has to work in reverse bias conditions, the anode voltage has to be properly set by taking into account the input offset voltage of the operational amplifier. Therefore, the input offset voltage has to be measured before proceeding with the light sensor characterization.

The anode and cathode terminals were shorted and left floating to prevent damages to the photodiode when

measuring the input offset voltage. The measured offset voltage was as high as 13.5 V.

Given the offset voltage and the amplifier common mode input voltage, the anode bias voltage has to be set according to the following equation:

$$(4.2) \qquad V_A = (V_{CM} + V_{OS}) - V_{OPD}$$

Where V_{CM} is the input common mode input voltage, V_{OS} is the input offset voltage (it can take a positive or negative value) and V_{OPD} is the required reverse bias voltage of the organic photodiode.

The input common mode voltage (V_{CM}) and the reverse bias voltage of the OPD (V_{OPD}) were set at 33 V and 5 V, respectively. According to equation (4.2) and taking into account the measured input offset voltage (V_{OS}) of 13.5 V, the anode bias voltage (V_A) was set to 41.5 V.

The light sensor functionality was verified by reading the output voltage variation due to the incident light intensity variation.

The light source (halogen lamp PHILIPS Brilliant Line 50 W, 12 V, 36°) was placed at 45 cm from the light sensor and the incident light intensity to the photodiode was

measured by using a precision lux meter (ISO-TECH ILM 1335).

The light sensor output voltage variation measured at ten different values of the intensity of the incident light (i.e. from 0 lx to 11400 lx) is shown in Fig. 4.25.

As expected, a linear detection of the incident light intensity was achieved. Indeed, an output voltage variation of about 1 V (i.e. from 46.75 V to 47.7 V) was measured with the photocurrent in dark (0 lx) and maximum illumination condition (11400 lx) of 0.37 µA and 1.76 µA, respectively.

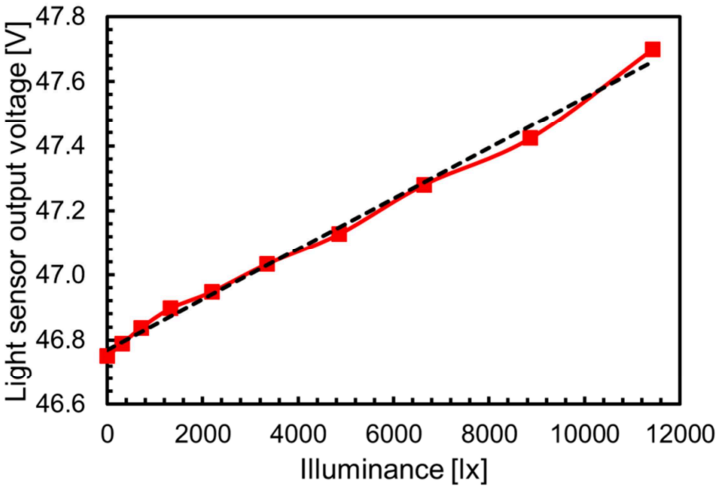

Fig. 4.25. Foil-to-foil light sensor output voltage measured with ten values of the incident light intensity.

For the sake of completeness, the light sensor functionality was also proved at lower supply voltages (i.e. 40 V and 50 V).

The measurement results of the fully integrated light sensor were not reported since during the drawing up of this thesis the finalization of the fabrication process, which enable the integration of OPD, amplifier and passive components on the same flexible substrate, was still on going.

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