UNIVERSITÀ DEGLI STUDI DI CATANIA

SCUOLA DI DOTTORATO

Dottorato di Ricerca Internazionale in Ingegneria dei

Sistemi – XXVIII° ciclo

Ph. D. Thesis

Fully integrated systems with on-chip galvanic isolation in silicon technology

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Anno accademico 2014/2015

Summary

This thesis summarizes main activities that I have been carrying out at the *Radio-Frequency Advanced Design Center* (RFADC), a joint research center between STMicroelectronics and the University of Catania, during my three years of Ph. D. studies.

My principal activity was part of an RFADC research project which exploits an STMicroelectronics technology providing on-chip galvanic isolation. This available platform was previously addressed to the implementation of galvanic-isolated data transfer and it is currently used for mass production. In this context, the principal purpose of my work was the investigation on fully integrated systems providing on-chip galvanic isolation in a silicon technology. This research is mainly motivated by the higher level of integration that is demanded to the next generation of power converters and several other applications requiring galvanic isolation. In this field both data and/or power transfer are commonly required for sensing and control purposes, with typical applications requiring few tens of Mbps and less than 1 W for data and power transfer, respectively. Within this context, fully integrated interfaces can provide several advantages, including higher reliability, lower PCB area, lower system complexity and hence lower costs, especially if only silicon technology is exploited. However, the state of the art of silicon-based integrated solutions mainly concern data-transfer devices, whereas for power transfer even the most advanced solutions rely on post-processed passive devices. These topics are presented in Chap. 1.

Integrated power transfer in current silicon technologies entails several challenges

due to inherent technology limitations, which require peculiar and customized design strategies to properly exploit the integrated approach. Therefore, this thesis focuses on fully-integrated systems, with the aim of filling this last gap by implementing also power transfer with silicon technology. This is a complex task that requires accurate evaluation of on-chip and off-chip parasitics, modeling of integrated passive devices, and customized active and passive circuit co-design. Specifically, my two principal activities are discussed in this thesis, that were the integration of a galvanically isolated, watt-level, step-up, power transfer system for gate driver's power supply applications, and the design of two ASK data receivers for an innovative data/power transfer system. They are the object of Chap. 2 and Chap. 3, respectively, whereas my contributions to two more CMOS-based power transfer systems can be found in App. B. These systems have been integrated in the aforementioned technology and successfully characterized, showing comparable power and data transfer performance with respect to the state of the art. To the best of the author's knowledge, these are also the first reported systems of this kind which do not require post-processing steps, therefore demonstrating the feasibility of power with/without data transfer on silicon technologies and thus promising new and highly-integrated devices to become available.

Besides these main topics, It is worth mentioning a secondary topic, carried out during the first year of my Ph. D. studies. Specifically, I actively contributed to the "COSMIC" Project, a second research project to which the RF-ADC participated in last years, in collaboration with the Technical University of Eindhoven, CEA-Liten, Fraunhofer Institute EMTF, and several other international partners. The COSMIC project was an FP7 research project in the field of organic and printed electronics. Organic electronics is seen as one of the most promising technology, especially if printed manufacturing techniques are used. By providing very low-cost electronics and flexible or wearable devices, its aim is to participate to the ubiquitous computing trend promised and renowned as the "Internet of Things", and extend its

applications. For example, the availability of a printed *radio-frequency identification* (RFID) tag is a key target for printed electronics, which could further shrink the costs of RFID technology, thus enabling a wider range of applications to take advantage of it. However, current organic technologies offer very low performance, thus requiring proper design techniques and architectures to be introduced. As a main outcome of my contribution to this project, the implementation of an integrated 13.56-MHz RFID tag in a printed complementary organic thin-film transistors technology (C-OTFT) on flexible substrate has been successfully demonstrated for the first time. This circuit is the most complex mixed-signal integrated system ever published in a printed C-OTFT technology, with more than 250 organic TFTs on the same foil. Its design and characterization are the object of two publications, [1] and [2].

Contents

List of Tables

List of Figures

Chapter 1

Introduction

This chapter introduces the object of this dissertation, that are fully-integrated systems providing on-chip galvanic isolation. Starting from system-level considerations, low-power applications that can be addressed with current silicon technology are identified and their state of the art is presented. Afterwards, the aim, the adopted technology platform, and the main outcome of this work are briefly presented.

1.1 Low-power isolated interfaces

Galvanic isolation, from now on simply referred to as "isolation"[1], is becoming more and more important due to its mandatory requirement in the wide field of applications involving digital control and measurement, either for proper operation, system reliability, or safety reasons. It is commonly adopted whenever high-power equipments are required to be operated by human beings or to guarantee fault protection in harsh industrial environments. Incidentally, these and many other applications often require isolated power supplies with relatively low output power, as well as

[1]In this context, the terms "insulation, isolation", and "galvanic isolation," have all the same meaning.

data-transfer links to enable communication across the insulation barriers.

We will briefly present the need for these low-power isolated interfaces in power converters and wireline transceiver applications, and more generally the safety reasons which make isolation mandatory by many system-level standards. Then the state of the art of low-power isolated interfaces is briefly discussed, along with their relative component-level regulations. Finally some market data are presented, which are useful to understand the potential revenues for these devices.

1.1.1 Applications

House-keeping circuitry

Every modern power conversion system relies on switched-mode power electronics (SMPE) for high-efficiency power conditioning and control. Typical examples are switched-mode power supplies (SMPS) and motor drivers. These systems target output power from few tens of watt to hundreds of kilowatt and thus require galvanic isolation between the control circuitry and the high-voltage one. Traditional applications involve both household and industrial appliances, while recent developments include converters for distributed power generation and for renewable energy sources such as wind turbines or photovoltaic plants. Besides, a further growth opportunity for SMPE is represented by the mass production of electric vehicles, which is predicted for the next decades [20]. Of course, the block diagram of an SMPE system involves digital control of the power stage for optimal operation, and hence, several low-power galvanic-isolated interfaces are required for the following use cases:

A. Power supply of signal circuitry, e.g. controllers, op-amps, comparators.

B. Power supply of drivers, e.g. gate driver's power supplies.

C. Bi-directional signal transfer, e.g. control signals, sensor interfaces.

For example, Fig. 1.1 shows four typical architectures for a motor drive, and each one includes all of these applications.

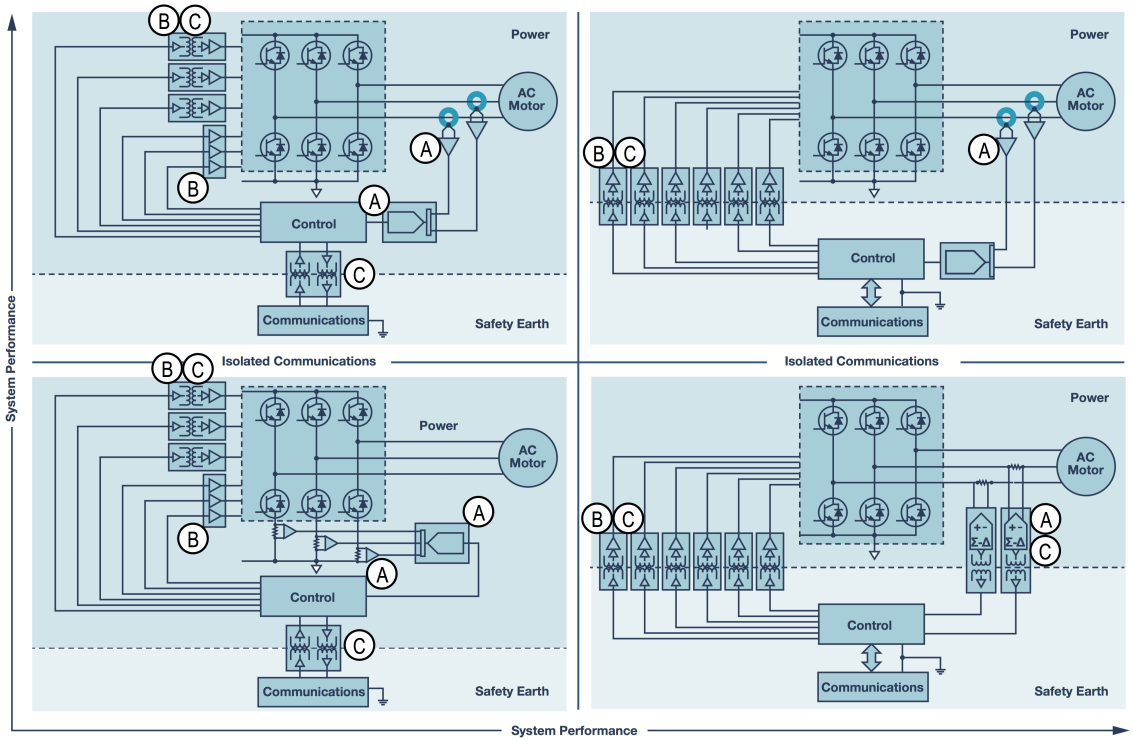


Figure 1.1. Typical architectures for a motor drive [6].

Application A is more common in legacy systems where isolated amplifiers were widespread, or when the controller must be located at the secondary side. It requires relatively low-voltage power supplies, with output power of several tens of milliwatt.

Application B entails much higher output power, since high supply voltages are typically required to reduce the conduction losses of the power switch. The easiest way to drive power switches are gate driver integrated circuits (ICs) based on high-voltage level shifters, which do not provide isolation and can drive a limited range of power devices, while still requiring an auxiliary power supply [21]. The traditional solution for high-side power supplies relies on the bootstrap capacitor technique, which poses limitations on the start-up, the duty cycle, and the maximum off time

for the high-side switches of the converter, while still requiring an auxiliary isolated power supply [22]. Besides that, both solutions do not completely eliminate the risk for latch-up even in the low-side gate-driver IC. This risk arises when the output node of the power switch goes below ground during inductive spikes or free-wheeling diode conduction, and can be eliminated by using galvanic isolation to connect each gate driver's ground to the source terminal of the relative power switch. The minimum power supply required by a gate driver can be expressed as

$$P_{GD} = P_{DR} + P_{GG}, \tag{1.1}$$

where P_{DR} is the power consumption of the driver and P_{GG} is the power required to periodically turn on and off the power switch. For power MOSFETs or IGBTs the input impedance is capacitive and hence P_{GG} can be estimated as the power required to charge its gate capacitance, that is

$$P_{GG} \;=\; f_S \;\cdot\; Q_G \cdot\; \Delta V_G. \tag{1.2}$$

Here f_S is the maximum switching frequency of the converter, while Q_G and ΔV_G are the gate charge required to turn on the power device, and the voltage swing at the gate, respectively. State-of-the-art gate-driver ICs operate with peak switching currents between 4 and 6 A and $f_S < 1\,\text{MHz}$, that are well suited for mass market applications such as 600/1200 V inverters, UPS equipment, industrial drives, and motor drivers in hybrid and electric vehicles [21, 23]. These specifications match the requirements of commonly used power switches, e.g. $2 - 4\,\text{nF}$ and ΔV_G of $15 - 20\,\text{V}$ for IGBTs[2] [25, 26]. Taking into account typical IC power consumption for P_{DR}, a maximum power supply of around 1 W at 20-V output voltage is required to enable a wide range of real-world applications. These power levels are typically managed by

[2]Typical IBGTs require $V_{GE} = 15\,\text{V}$ in the on-state and often $V_{GE} = -5\,\text{V}$ in the off-state [24]. It is worth mentioning that the trend for next generation power switches such as GaN, GaAs, and SiC, is to reduce both the gate charge and the gate voltage swing.

fully integrated power amplifiers for RF communication, therefore a fully integrated implementation in silicon technology is potentially feasible. It is worth noting that for both A and B power supplies, their power consumption is often a small fraction of the overall power losses involved in the application, e.g. of the main converter, therefore their power efficiency is not a main concern from the application point of view.

Application C typically involves low-frequency signals for feedback or control purposes. On the other hand, large data-rate can be required by high-precision sensors, commonly used for voltage/current sensors in offline converters, inverters, and power meters or even stand-alone sensor interfaces [27]. Typical applications call for data-transfer rates from tens to few hundreds of Mbps. Besides the data transfer, it is worth noting that the data interface also requires an additional low-voltage power supply. Low output voltage ($< 2.5\,\mathrm{V}$) is convenient to take advantage of scaled technologies for the sensor interface implementation, which guarantee the best performance in terms of speed. Again, the peak power efficiency required for these applications is not a main concern, whereas low-load efficiency and quiescent power dissipation are much more important [28].

Wireline networks

Although RF communication is very popular for consumer applications, when it comes to safety-critical applications wireline networks are the solution of choice. Wireline networks based on TIA-485 physical layer are the most used in industrial applications due to differential signaling, communication distances up to 1.2 km and data-rates up to 10 Mbps [29, 30]. However, the most widespread application of wireline networks is probably found in the automotive industry: modern high-end vehicles can house up to 120 electronic controller units indeed, which need to share sensor data or drive actuators. The complexity of in-vehicle communication networks led car manufacturers to define several communication standards, e.g. Local

Interconnect Networks, Controller Area Networks (CAN) and Flexray, with the CAN bus as the most successful one, actually gaining popularity even in automation and remote control applications [31, 32].

Either in a large industrial plant or in the small environment of a car, wireline networks are often subject to very high disturbances like electro-magnetic interferences (EMI), voltage surges and ground shifts. A common issue of these networks is avoiding ground loops, as described in Fig. 1.2. Wireline communication requires

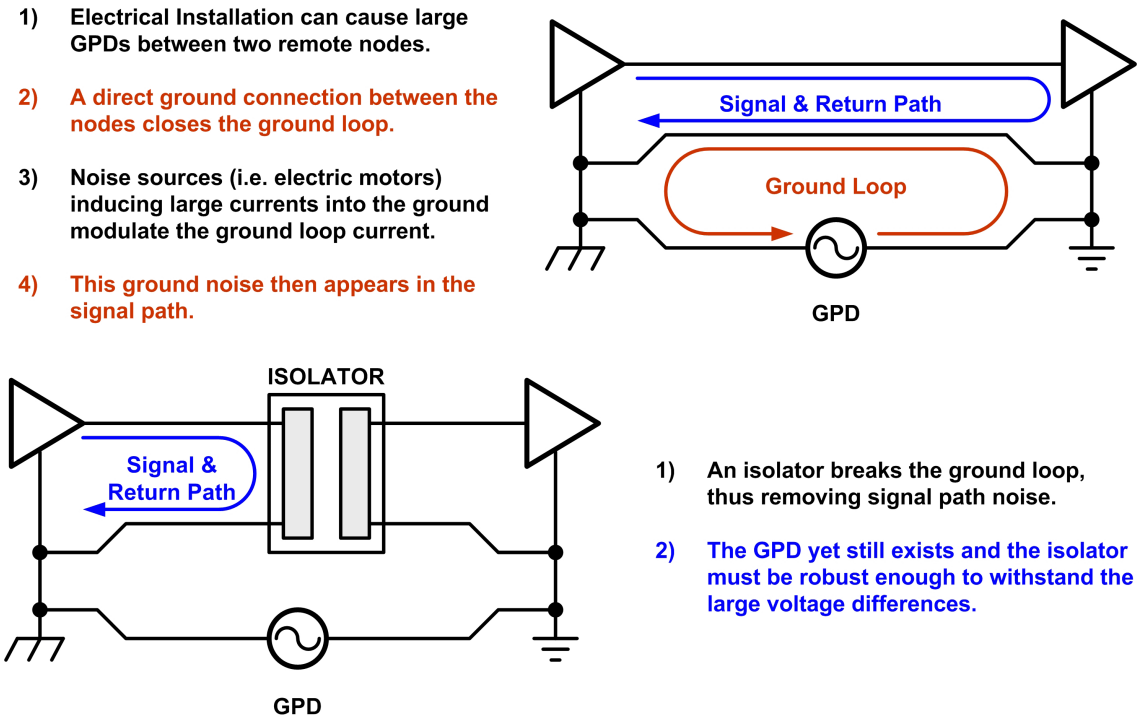


Figure 1.2. Ground loops problem in wireline communication systems [7].

a low-impedance ground connection between network nodes, which forms a ground loop with the local ground reference of each transceiver. It is unlikely for systems with very far ground references to maintain the same potential, and therefore ground potential differences (GDPs) are commonly found in wireline installations. Due to

the low-impedance path offered by the ground conductor, even small GPDs can produce high current flowing in the ground loops, which corrupts the signal integrity and can be harmful for both sensitive circuitry and human operators. By providing isolation at the transceiver interface all the systems connected to the bus can be referenced to a single ground, therefore preventing any ground loops. Moreover, any electro-magnetic (EM) noise coupled to the cable can cause both GPDs and instantaneous voltage surges in the range of hundreds or even thousands of volts. Typical surges are due to high-current switching loads (e.g. electric motors), or unpredictable events such as electrostatic (ESD) discharges and lightning strikes. These surges can irreparably damage grounded transceiver interfaces, whereas isolation allows the transceiver ground to follow the surge and hence improves the robustness of the network [33].

Low power wireline transceivers for CAN bus and TIA-485 networks operate at 5 V with current consumption around 70 mA in normal operating conditions [34, 35]. Therefore, an isolated power supply providing around 350 mW output power at 5 V is highly desirable to simplify wireline network's design.

Safety reasons and systems regulations

Previous examples mainly require low-power isolation either to enable correct operation of the system or to improve its performance. This requirement is called *"functional isolation"* because it does not guarantee protection from electric shocks. Of course, safety reasons are the most important motivation for galvanic isolation, being the flow of current through human body the main cause of electric shocks. As shown in Table 1.1, electrocution due to ventricular fibrillation can be triggered even by relatively low current values. Other mishaps that can represent serious life threats and are directly related to electrical shocks are burns, either directly from sparks or indirectly from increased fire risks, and the involuntary muscle reaction as a consequence of the electric shock.

Table 1.1. Thresholds and limits for continuous 60 Hz current and their effects [3].

Physiological effect	Reaction	Threshold for continuous 15- to 100-Hz current (mA)
Involuntary muscular reaction	Perception level, tingling sensation	0.5
Inability to let go (tetanized muscle)	Painful shock, freezing current, "can't let go"	10
Ventricular fibrillation	Heart rhythm affected, death may occur	35

Consequently, several safety standard regarding commercial products have been developed to guarantee suitable end-user protection through isolation. They limit voltage and currents which may be in contact with human operators, either in static or transient conditions, and define system specifications, patterns of test-cases, and physical restrictions to be passed by end-products, depending on the application and for realistic operating conditions. Some examples of commonly used regional and international standards are reported in Table 1.2. Regional regulations are

Table 1.2. System-level standards involving isolation by market and region [4].

	Household	Industrial	Information Technology	Measurement and Control	Medical	Telecom
International	IEC 60065	IEC 60204	IEC 60950	IEC 61010-1	IEC 60601	IEC 60950
Germany	VDE 860		EN 60950	VDE 410/0411	VDE 0750	VDE 0804
USA	UL 60065	UL 508, UL 60947	UL 60950	UL 61010	UL 60601	UL 60950
Canada		CSA. 14-10	CSA 60950	CSA 61010	CSA 601	CSA 60950

defined by national bodies, such as Verband Deutscher Elektringenieure (VDE), Underwriters Laboratories (UL), and Canadian Standards Association (CSA), for Germany, United States, and Canada, respectively. These agencies also provide system-level testing and certification of products. Their regulations often follow the guidelines of international agencies such as the International Electrotechnical Commission (IEC) and the European Norms (EN), although there can be substantial differences between each regional version [4].

The main concept behind these regulations is that three levels of protection are commonly defined, that are *basic*, *double*, and *reinforced* insulation [15]. Basic

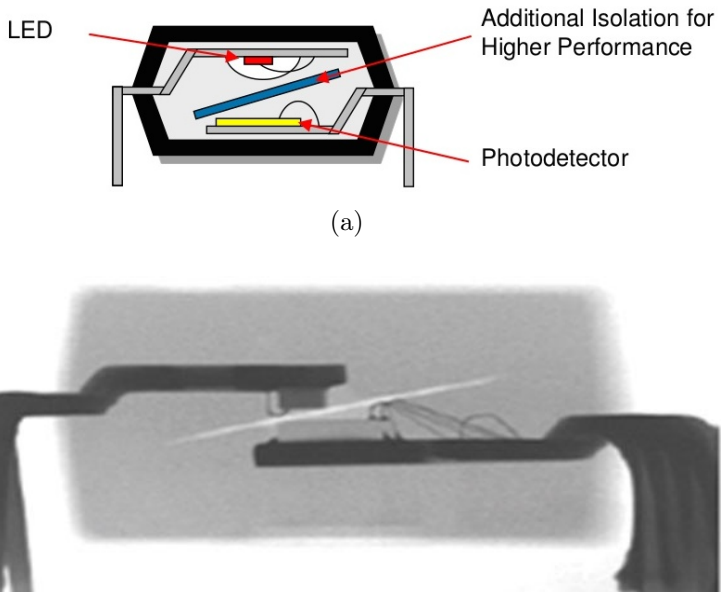
insulation is ascribed to a system which provides isolation while protecting the end user from potentially lethal shocks, as long as the isolation barrier is intact. Double insulation is often mandatory for end-user products. It requires a second insulation system to guarantee basic protection even if the first insulation system fails, therefore providing redundant protection. The straightforward way to achieve double insulation is by cascading two basic-insulation systems, thus increasing costs and complexity and limiting the performance of the system. As a result, reinforced insulation has been introduced, and it is the most used isolation level, being defined as a single insulation system which guarantees electrical-shock protection equivalent to double insulation. For a given application, system designers must choose the insulation characteristics of each component to meet system-level standards.

1.1.2 State-of-the-art

The traditional components used to guarantee isolation for data transfer and their relative low-power supplies are optocouplers and discrete transformers, respectively. In last years, several different solutions for galvanic-isolated silicon-integrated data transmission have been proposed using RF links [36], capacitive coupling, or integrated coreless transformers. These devices are commonly referred to as "digital isolators" or simply "isolators". As far as power transfer is concerned, discrete transformers are still the solution of choice even for the aforementioned low-power ($<<$ 1 W) applications. Few attempts to achieve higher integration levels through traditional topologies indeed end up with cm-sized solution for the sole transformer. An example is the work reported in [37], which also require unconventiional processes and technologies and hence is not cost-effective.

Optocouplers

Optocouplers exploit light to transfer electrical signals, usually in the near-infrared region. The typical internal structure of an optocoupler is described in Fig. 1.3(a), while an X-ray scan of a device is shown in Fig. 1.3(b)[38]. Two separate metal



(a)

(b)

Figure 1.3. (a) Typical optocoupler structure. (b) X-ray cross section of a device.

frames house a light source and a photodetector, respectively. A GaAs light emitting diode (LED) and a phototransistor are commonly used to generate and detect the light. The dice are coated with the molding compound which provides isolation from external light, galvanic isolation, and the mechanical substrate for the metal frames. The spacing between the two dice depends on the isolation rating of the device, being typically greater than 400 μm for high-end products. The highest performance in terms of isolation and speed is obtained including more than one dielectric material within the package, for example silicon lens can be used to increase isolation and sensitivity of the photodetector [39], but they also increase costs and complexity of the package.

Optocouplers have been historically used to implement both analog and digital data-transfer links since they exhibit several cost and size advantages over the only alternative available in the past, i.e. bulky discrete pulse-transformer. However, their use is quite complex due to the intrinsic variability of their performance. Fig. 1.4 shows the common equivalent circuit of an optocoupler. It is character-

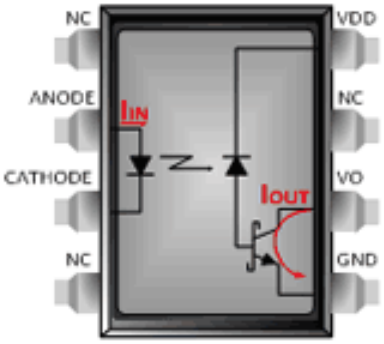


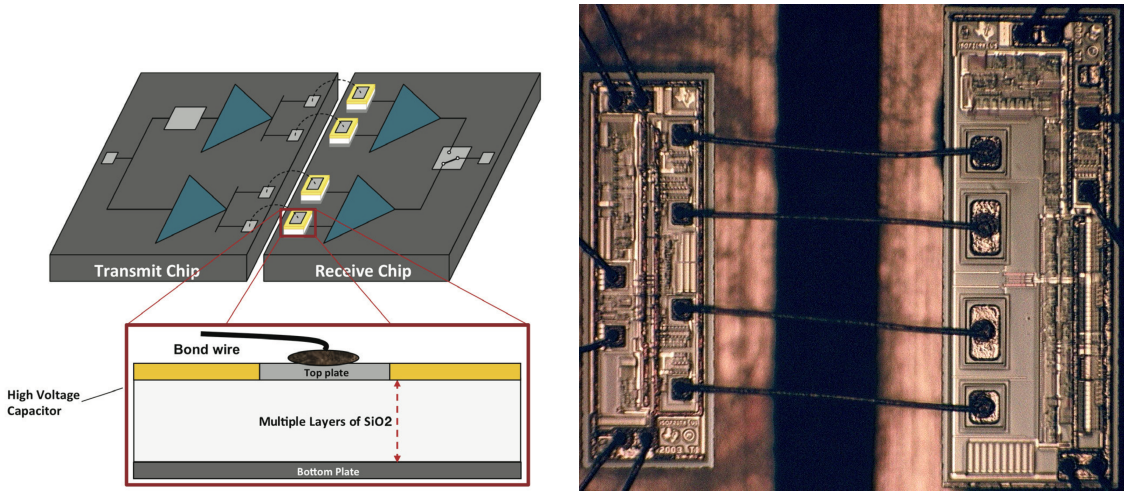
Figure 1.4. Optocoupler equivalent circuit [8].

ized by the current transfer ratio (CTR), that is the ratio of the output current of the phototransistor I_{OUT} versus the input current of the LED I_{IN}. Biasing currents define the bandwidth of the link and hence are proportional to the data rate. State-of-the-art high-speed optocouplers draw more than 30 mA for a 40 Mbps link. Being related to the phototransistor current gain β, the CTR depends on both biasing currents and temperature and changes widely between each sample. These dependencies are accentuated by the great temperature sensitivity of GaAs and the impact of aging on the LED brightness. This last aspect is particularly important since the LED aging is accelerated with higher current levels, therefore a trade-off exists between performance and lifetime of the device [8].

Capacitive isolators

Capacitive isolators rely on high-voltage capacitors to sustain the required voltage rating and provide isolation. Although advanced or exotic technologies have been

proposed [40, 41], the most diffused and integrated approach adopt the inter-metal dielectric (IMD) commonly used in silicon manufacturing technology, that is silicon di-oxide (SiO_2), to achieve isolation. Figure 1.5(a) shows the typical arrangement of a state-of-the-art capacitive isolator, along with the cross section of the high-voltage capacitor. The latter is a parallel plate capacitor which uses standard metal layers for the top and bottom plate and several layers of thin-film SiO_2 to achieve isolation [9]. Two dice attached on separate metal frames house transmitters and receivers, respectively. The receive chip in the figure houses the isolation capacitor, whose top plate is connected to the transmitter output by bonding wires. Figure 1.5(b) shows a micrograph of the isolator before packaging [10]. The transmitter



(a) (b)

Figure 1.5. (a) Typical capacitive isolator system [9]. (b) Photo of the system before packaging [10].

adopts radio-frequency (RF) amplitude modulation to transfer the data across the insulation barrier, usually on-off keying (OOK) to maximize the noise margin. The receiver performs filtering of the input signal to reject interferers and common-mode disturbances, and amplitude demodulation to recover base-band data. By working at very high frequency (VHF), this approach enables low values for the isolation capacitors and simplifies the filtering. Besides that, SiO_2-based capacitive isolators

offer several advantages when compared to optocouplers:

- their level of integration is the highest possible for conductive-substrate based system
- they are CMOS compatible and take advantage of scaling and VLSI advancement
- the high impedance of capacitors entails very low current consumption
- low silicon area is required thanks to RF modulation

Clearly, the fully-integrated insulation approach is the key factor in providing these advantages: silicon di-oxide is known as one of the best dielectric insulator with reported dc dielectric strength around 850 V/μm for pure samples, which is much higher than organic-based compounds [41]. Being widely used for decades, thin-film SiO_2 layers of very high quality and very low defects per area can be achieved within the semiconductor's manufacturing process. The high dielectric strength can guarantee a good isolation rating even with a relatively thin insulation layer when compared to organic-based insulators, therefore only two silicon dice are required to implement the isolator. This enables easy and low-cost mass production.

A common concern about capacitive isolators is their sensitivity to common-mode transients and electric fields, which can be effectively taken care of by using differential signal transmission techniques. Such transient events cause common-mode currents to flow through isolation capacitors and may corrupt data transfer. Isolator's robustness to common-mode transients is one of the key parameters of the isolator, and is frequently indicated by the common-mode rejection (CMR) or the common-mode transient immunity (CMTI). It is measured by applying sharp voltage pulses between the two isolated ground references of the device, and defined as the highest potential variation that the isolator can withstand without affecting its data transfer performance. Typical values for CMTI are lower than 25 V/ns for

optocouplers, whereas capacitive isolators can achieve up to 100 V/ns CMTI thanks to differential signaling. However, integrated capacitive isolator techniques do not lend themselves easily to implement power transfer, as shown in Fig. 1.6. Here an

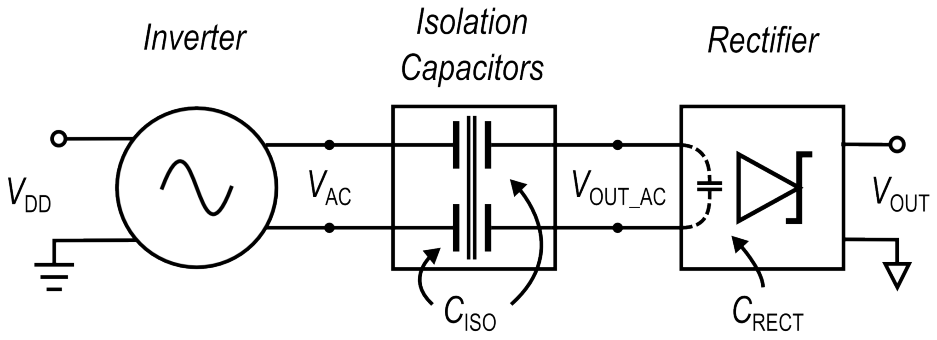


Figure 1.6. Capacitive voltage partition at the rectifier's input port.

inverter produces the ac voltage V_{AC} which drives the isolation capacitors, C_{ISO}. The ac/dc power conversion of the isolated ac voltage, V_{OUT_AC}, is performed by a rectifier that shows finite input parasitic capacitance, C_{RECT}. Clearly, a voltage partition occurs at the rectifier's input, and C_{ISO} should be made much higher than C_{RECT}, being

$$V_{OUT\_AC} = \frac{C_{ISO}/2}{C_{ISO}/2 + C_{RECT}} \times V_{AC} \tag{1.3}$$

This is in contrast with both costs and isolation performance of an integrated isolator, being C_{RECT} in the order of the picofarads and the specific capacitance of a 10 μm-thick SiO_2 layer around 3.45 pF/mm^2. Indeed, high isolation ratings entail high oxide thickness, which reduce the specific capacitance of C_{ISO}, thus increasing the silicon area for a given rectifier capacitance. Furthermore, the latter is typically proportional to the rectifier efficiency.

Magnetic isolators

Magnetic isolators, and particularly the inductive ones[3], currently represent the most diffused integrated approach for isolators between semiconductor manufacturers. Similarly to capacitive isolators, two chip house a transmitter and a receiver, whereas a planar transformer is used to achieve isolation, as shown in Fig. 1.7. The

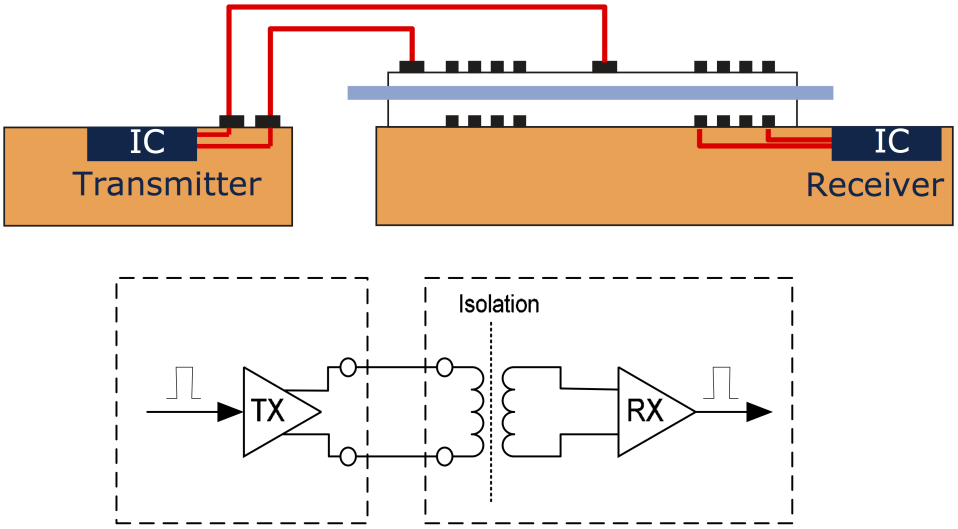
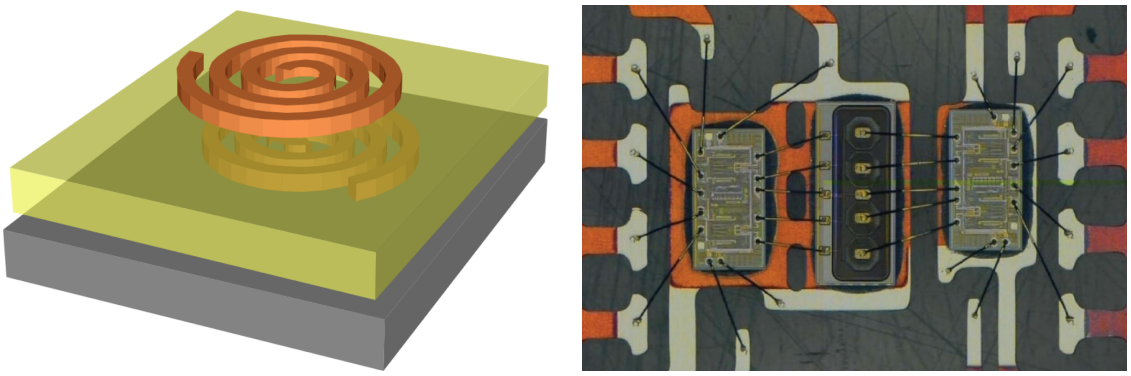


Figure 1.7. Integrated inductive isolator architecture [11].

first successful magnetic isolator was introduced by Analog Devices in 2001 with the iCoupler technology [12]. The transformer is fabricated with two stacked spiral inductors that are isolated by a thin-film dielectric, as shown in Fig. 1.7. The iCoupler technology adopts a 20-25 μm-thick polyimide (PI) layer to provide insulation, depending on the isolation rating. A 6 μm-thick electroplated Au layer is used for the top transformer spiral, whereas the IC top metal layer is used for the bottom one. A photo of a four-channel isolator before packaging is shown in Fig. 1.8(b).

[3]Other magnetic isolation techniques include Hall-effect and giant magneto resistance links, which can be only used for data transfer applications. Besides, isolation in these technique is often achieved at the package level, similarly to optocouplers.



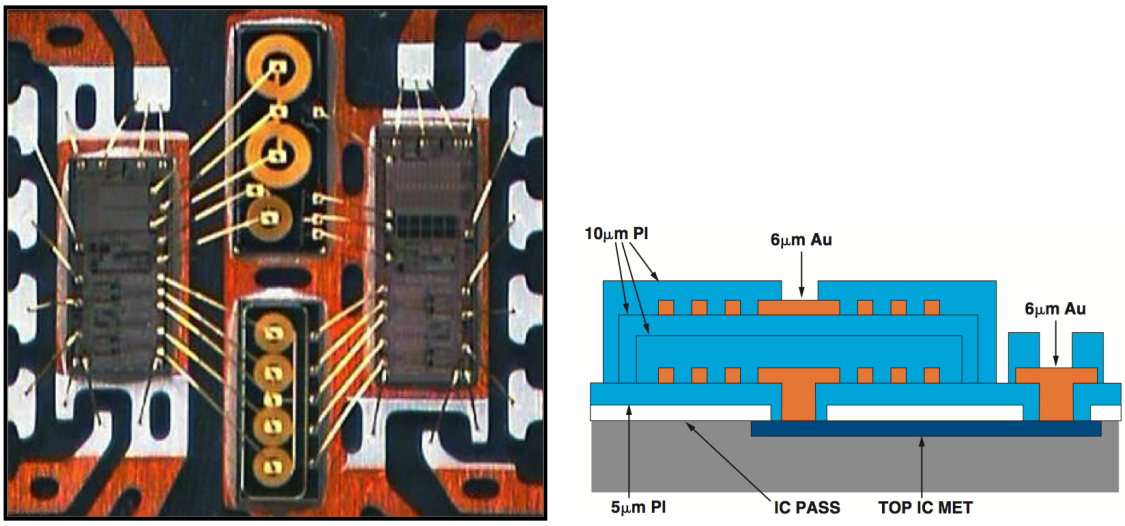
(a) (b)

Figure 1.8. (a) Planar isolation transformer. (b) Photo of an inductive isolated system before packaging [12].

Differently from capacitor-based isolators, transformer-based isolators are well suited for power transfer applications, since the series inductance of the transformer can compensate the input capacitance of the rectifier. Moreover, they are much less susceptible to common-mode transients. Indeed, the capacitive coupling between transformer's windings is a parasitic effect, which is further reduced when high dielectric thickness is used, thus increasing both CMTI and isolation rating.

Several power transfer system in packages (SiPs) are currently available using the aforementioned iCoupler technology, with output power levels from tens to few hundreds of milliwatt and data transfer channels in a multi-die SiP, depending on the output power and complexity of the device [13]. The micrograph of one of these systems is shown in Fig. 1.9(a). It is worth nothing that for power transfer applications both power transformer's coils require thick Au metals to achieve good efficiencies, thus increasing manufacturing costs.

Recently, many products using on-chip silicon galvanic isolation have become available for the applications described in Sec. 1.1.1, e.g. general purpose isolators [42, 43, 44], isolated gate-drivers [23, 25, 45, 46, 47] and so on. These products benefits from all of the advantages previously discussed for SiO_2-based isolators, but they are currently limited to data transfer applications. The main challenge



(a) (b)

Figure 1.9. (a) Cross-section of isoPower transformer. (b) Photo of an inductive power/data transfer SiP [13].

in implementing power transfer is achieving a good trade-off between efficiency and power density to enable cost-effective integration. This is due to the high sheet resistance of IC metal layers, which entails low quality factor for the coils and hence low efficiency and high area for the transformer itself, as discussed in detail in the following chapters.

Component regulations

Component regulations are the counterpart of system regulations, and define specifications to be met by components to guarantee a certain level of protection within a system. Commonly adopted component-level standards are the following:

- UL 1577
- IEC 61010-1[4]

[4] *"Safety standard for measurement, control and lab equipment"*, also defines component requirements.

- IEC/DIN/EN 60747-5
- VDE 0884-10

Two main class of component standards can be recognized: UL 1577 and IEC 61010-1 focus on voltage breakdown, whereas regulations such as VDE 0884-10 and IEC 60747-5 are based on partial discharge tests [48].

The former class consists in breakdown-voltage tests to characterize the robustness of the device to over-voltage conditions. Breakdown is achieved when a substantial static leakage current can be detected across the isolation barrier. For example, UL 1577 defines the isolation withstand voltage V_{ISO} that is the RMS value that can be sustained for one minute. Lot-samples are tested to establish the voltage rating of the component, with common required values of $1\,\mathrm{kV_{RMS}}$, $2.5\,\mathrm{kV_{RMS}}$, $3.5\,\mathrm{kV_{RMS}}$, and $5\,\mathrm{kV_{RMS}}$. This test is destructive: the device must survive for only one-minute, but may fail for longer duration and this over-voltage condition should not be applied anymore. Each device must also pass a one-second non-destructive test at $1.2 \times V_{ISO}$ during production.

These tests do not characterize the ability of the device to withstand periodic or continuous voltage stress. On the other hand, standards like VDE 0884-10 and IEC 60747-5 look for partial discharge across the isolator, which may degrade the lifetime or the insulation rating of the barrier if a second test is performed [14]. For example, both IEC 60747-5 and VDE 0884-10 require the devices to be tested with the waveforms defined in Fig. 1.10. Here V_{IOTM} is the peak transient voltage that the device can sustain, and it is equivalent to UL 1577 isolation withstand voltage V_{ISO} for sinusoidal voltage stress. After the transient voltage the device is tested for partial discharge for a certain voltage that is proportional to the maximum peak repetitive voltage V_{IORM}, or the working voltage V_{IOWM} for RMS or dc rating. Method A and method B1 differ for voltage values and measuring times and are used for lot-samples and production tests, respectively.

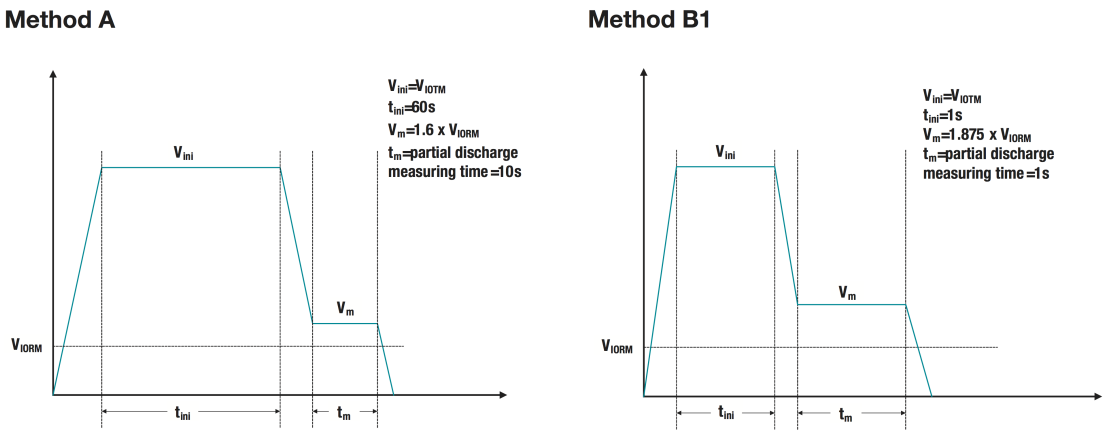


Figure 1.10. Simplified IEC 60747-5 and VDE 0884-10 test profiles [14].

Most regulations were developed when only optical isolators were available and are tailored to their physical structure, where the insulator thickness (a.k.a. *distance through insulator* or DTI) is very high. This is the case for UL 1577 and IEC 60747-5, which only apply to optical isolators. VDE 0884-10 has been recently developed instead, to expressly take into account the availability of highly integrated semiconductor isolators with micro-scale isolation barriers, either using magnetic or capacitive transfer techniques. It certifies reinforced insulation as well as IEC 60747-5-5, but it also includes a 10 kV surge test, which is performed with the waveform in Fig. 1.11, where V_{SURGE} (a.k.a. V_{IOSM}) is the maximum surge isolation voltage [15]. Many other bodies are planning new standard releases, either at component or system level, to take into account these new thin-film semiconductor devices [14, 4].

It is also worth nothing that many component standards and system-level regulations as well, often pose specific requirements on the clearance (i.e. distance through air) and creepage (i.e. distance along the surface) of the isolator's package, as defined in Fig. 1.12, and its fabrication materials.

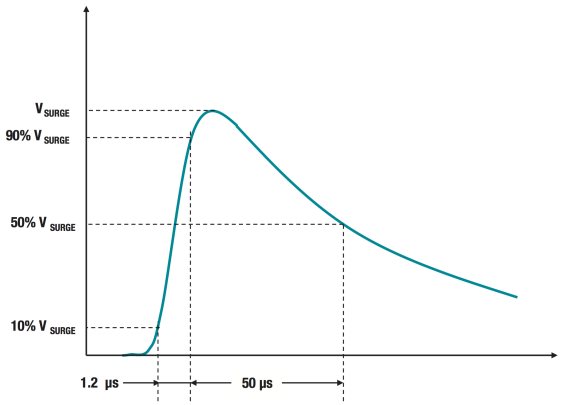


Figure 1.11. Simplified VDE 0884-10 surge test profile [14].

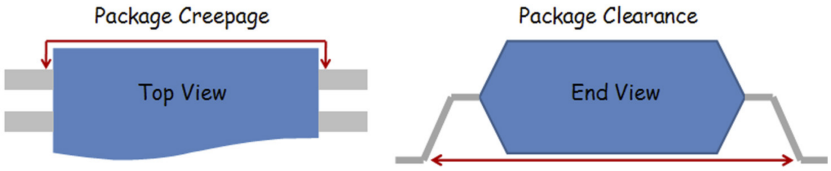


Figure 1.12. Definition of clearance and creepage [15].

1.1.3 Isolator's market

A quantitative estimate of market revenues is a quite complex task, usually provided by highly-specialized consultancy companies. Consultants perform market research, interviews with both customers and manufacturers, and elaborate detailed reports about specific business markets, macroeconomic areas, global trends and so on. Key customers for these expensive and detailed reports are investors, market analysts, financial advisors, and both original equipment manufacturers and semiconductor companies, but also governments. Besides these reports, the few isolator's market data available for free on the internet can also prove useful to understand the amount of isolator's business and hence the importance of innovation in this field.

IHS is one of these consulting companies. In [49], released on 2013, December, a

compound annual growth rate[5] (CAGR) up to 10-20 % from 2013 to 2018 is expected for optocouplers, which are the mainstream isolator technology. Particularly, the gate driver market is expected to experience high-growth, according to this report. Optocouplers market is estimated around $1.3 billion, with $543 million from high performance optocouplers, in spite of their drawbacks when compared with the already discussed integrated isolators.

Another report from IHS, released on 2014, May, contains the graph in Fig. 1.13 that is referred to the worldwide isolation market. It is available at [16], where a growth of 8 % between 2012 and 2013 is reported, thus confirming $1.33 billion of market revenues in 2013. One of the key point for this growth is the automotive

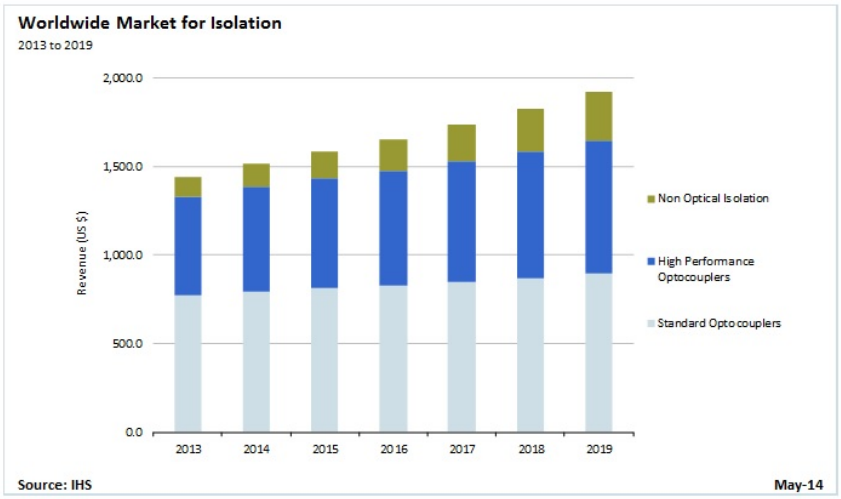


Figure 1.13. Forecasts for worldwide isolation market [16].

market: while being only 10 % of total optical isolation market in 2013, a Hybrid & Electric Vehicles (HEV) market growth of 7 % was observed in 2012/2013 and it is expected to rise up to 18 % in 2014. According to the report, a CAGR of 12 % is expected between 2013 and 2019 for optocouplers and solid-state relays in this

[5]It is defined as the growth rate of a geometric progression which fits initial and final market size values (see [50]).

market. For a comparison, industrial market is expected to grow by 12 % between 2014 and 2019 instead, that is a CAGR around 4.7 %. Fig. 1.13 and [16] also put a glance on non-optical isolators. IHS states that many manufacturers such as Analog Devices Inc., Texas Instruments and Silicon Laboratories have released products or hold patents in this area. Non-optical isolators show increasing success in new and high growth markets such as PV inverters, smart meters and especially HEV due to higher performance and reliability. It is worth nothing again that this is a market where high-performance devices are required, with relatively higher value with respect to industrial applications. Optocouplers companies like Avago, Toshiba and Renesas are trying to compete by introducing new high performance optocouplers but most of their sales occur in the traditional and more stable industrial markets and hence their growth may be lower compared to non-optical isolator companies.

Similar data are found in [51]. Transparency Market Research reports a market value of $1.87 billion in 2014. They also state that the market could reach $3.22 billion in 2021, that is a 8.2 % CAGR.

Finally, it is worth nothing the growing interest and high value of the Galvanic Isolated ADC market. According to IHS, it is worth $163 million or 12 % of the total isolation market in 2013, and it is expected to grow faster than the isolation market [52]. Actually, in spite of accounting for less than 2 % of isolator unit shipments, their price is much higher than the average, i.e. around $1.03 per unit in 2013. Avago was the no. 1 supplier of ADC isolation in 2013, with sales mostly based on standard optocouplers, and other suppliers include Fairchild, Renesas, Sharp and Toshiba but also ADI, whit the already discussed iCoupler technology, was mentioned. It is worth noting that ADI reports that more than 1 billion digital isolated channels were sold between iCoupler introduction in 2001 and 2013 [53].

Although the reliability of these almost exponentially-growing extrapolated data as well as the quality of market analysis and financial advisors are quite subjective, it is clear that an actual growth of isolator's sales took place between 2012 and 2014.

More solid reasons for this growth are the increasing policy support of governs and their commitment towards the reduction of global pollution and CO_2, as already pointed out in [20]. The path to achieve these targets mandates extensive use of switched mode power electronics, where isolated interfaces play a key role. In the end, innovation can be the key reason for increased market value, as it has always been in the past.

1.2 Aim of this thesis

As discussed in the previous section, a wide range of applications can benefit from fully-integrated devices providing on-chip galvanic isolation. These applications can be described by the general block diagram in Fig. 1.14. Here two domains are gal-

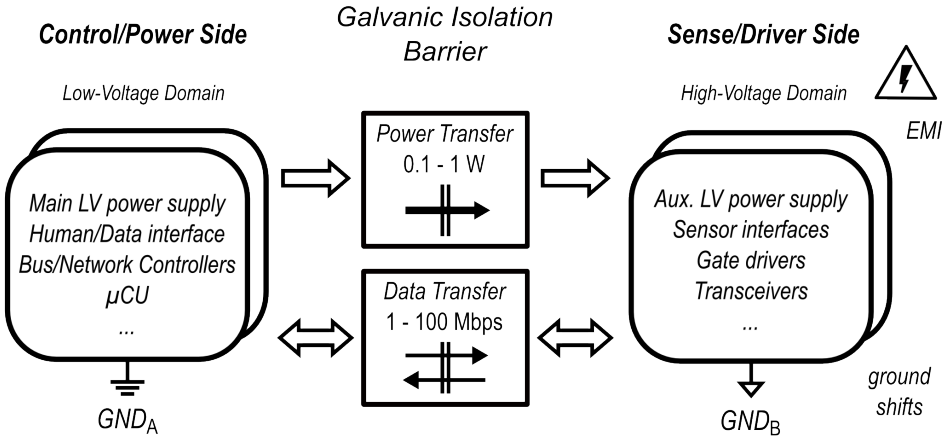


Figure 1.14. Typical low-power applications requiring isolated power transfer.

vanically isolated since one of them is subject to hazardous voltages and/or requires a different ground reference. Data signals are transferred across the galvanic isolation barrier to enable communication between the two domains, while isolated power supply for the second domain should be derived from the first one.

Thanks to continuous advances in semiconductor technologies, today some of

these applications can be addressed with a fully-integrated approach, which means that isolation is provided on-chip without any discrete or post-processed components. The market for these applications presents solid growth opportunities for the next decades, however most players currently focus on data transfer, whereas it is apparent that each isolator requires a relatively low-power isolated voltage supply. Specifically, the state of the art demonstrates that several data transfer applications have already been successfully faced in silicon technology, whereas, further to the power transfer, the most advanced implementations still involve post-processing steps including deposition of both thin-film dielectric and thick metal layers. Therefore, the implementation of fully integrated systems providing on-chip galvanic isolation which include power transfer and are 100 % made in silicon technologies is an ambitious target that can be also a key competitive advantage to gain market share in the expected growth scenario.

In this work we focus on circuit and system design techniques to achieve fully integrated power transfer with currently available silicon technologies, with or without data transfer. Technology aspects regarding the implementation of on-chip galvanic isolation are not covered, since the whole technology platform was supplied by STMicroelectronics. Due to the huge, inherent complexity of developing an isolator, we only focus on the key electrical aspects of the circuit design that are the amount of output power and the search for the maximum efficiency for a given technology. In this section the basic architecture of the developed systems is presented as well as the adopted technology platform and the main results achieved.

1.2.1 Basic architecture

As discussed in Sec. 1.1, inductive isolators are the most promising approach for area and power efficient, integrated dc/dc conversion. An integrated isolation transformer is the key component of these systems, which highly affects the choice of the system

architecture. Specifically, two planar stacked spiral inductors at least are used to implement the transformer windings while providing isolation. Since only thin metal layers are available in standard silicon technologies, these windings show very high series resistance and poor quality factor (Q-factor), which entails very high operation (VHF) frequencies as well as resonance operation to improve their performance [54]. However, the need for a transformer prohibits the use of very simple topologies such as buck or boost, which are proven to offer the best efficiency for fully integrated converters [55].

These considerations point toward a well-established architecture for the proposed systems, that is is shown in Fig. 1.15. Here the converter is basically a

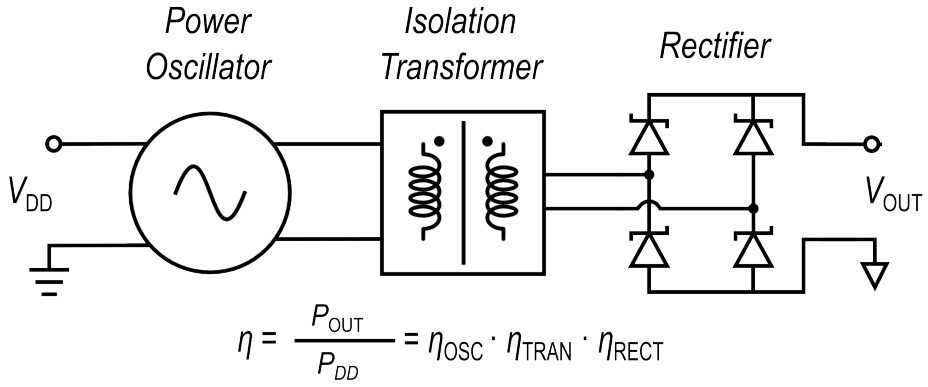


Figure 1.15. Basic architecture for isolated power transfer.

transformer-loaded power oscillator, whose resonant network includes the transformer, and the ac/dc converter input impedance. It converts the input power P_{DD} and the input voltage V_{DD} into ac power which feeds the isolation transformer input and hence the rectifier input. A full bridge rectifier was chosen as the simplest balanced topology to perform the ac/dc conversion, thus converting the ac power at the transformer output into dc output power P_{OUT} for the load, with output voltage V_{OUT}. Each block of this system suffers from power losses that can be expressed by

a power efficiency, i.e. η_{OSC}, η_{TRAN}, and η_{RECT} for the oscillator core, the isolation transformer and the power rectifier, respectively. Their product can be used to express the overall power efficiency of the converter, η_{DC-DC} or simply η.

Main advantages of this architecture include intrinsic soft-switching for the active devices of the oscillator, which is essential to reduce their switching losses, and the resonance operation that maximizes the transformer efficiency. Simplicity here is mandatory to reduce the load capacitance of the transformer, thus achieving high operating frequencies which maximize his intrinsic transfer efficiency, as discussed in the following chapters. Moreover, the oscillator architecture avoids the need for active device's drivers for the inverter, whose power consumption can be prohibitive for VHF operation.

On the other hand, this architecture is inherently characterized by highly nonlinear interactions between each block, which complicates the design. For example, transformer efficiency is highly dependent on the interaction with the driving stage, providing the ac input power, and the cascaded stage, which performs the ac/dc conversion. Moreover, the oscillator is inherently subject to parasitics and input supply variations and does not provide voltage regulation. These problems can be partially circumvented with accurate modeling [55] and feedforward techniques, [56, 57], while modulation of the output power, i.e. control of the output voltage, can be achieved by feedback control loops employing PWM or PFM techniques [55, 56, 58, 59, 60, 61].

1.2.2 Technology platform

The key technology used in this work is a 0.35-μm SOI-BCD technology that features both 3.3 V and 5 V CMOS transistors, a 5 V VHF npn BJT, lateral pnp BJTs and several MOS devices providing high-voltage capabilities through drain-extension techniques [62]. Three Al metal layers with 0.45/0.55/0.9 μm thickness, respectively,

and a 3.7 μm-thick top Cu layer are available for routing. The process was enriched for this work by a thick-oxide module [63] that was previously developed and characterized for galvanic-isolated data transfer, similar to other state-of-the-art integrated isolators [9, 64, 65]. This module has been recently used for mass-production of several devices providing on-chip galvanic isolation [25, 42]. The thick oxide layer is located between the two top metal layers, as shown in the simplified back end of line (BEOL) cross-section in Fig. 1.16, and can have different thickness depending on the isolation rating. The technology choice was driven by its compatibility with the

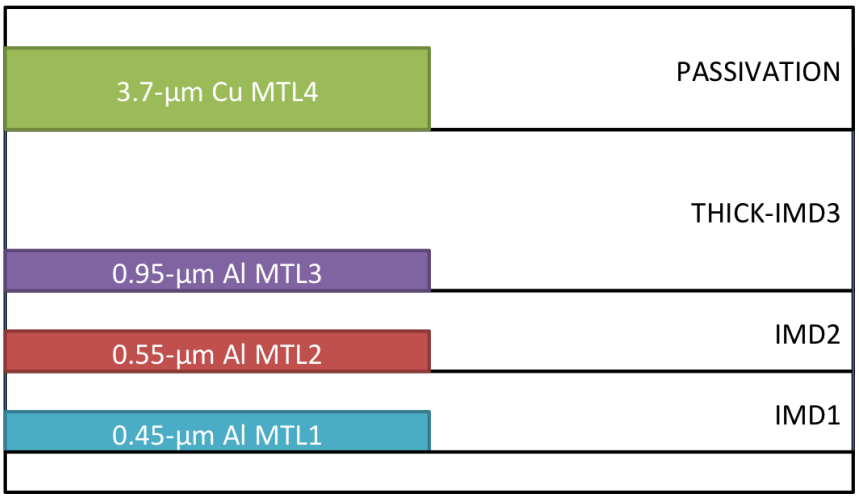


Figure 1.16. Simplified cross-section of the available back end of line with thick oxide module for galvanic isolation.

thick-oxide module fabrication process and by the high resistivity of the available SOI substrate, that is mandatory to achieve high efficiency for power transformers[6].

The second technology adopted in this work is a 0.13 μm standard CMOS process. Specifically, this technology was used to take advantage of the available high-voltage Schottky diode with sub-GHz operation capability, that has been a crucial

[6]It is worth noting that the SOI substrate is actually not required by the systems designed in this work. In principle, as far as the substrate resistivity remains the same, same or better results can be achieved in a process with junction isolation, which also benefits from reduced thermal resistance.

element to implement an efficient power rectifier. All technologies were provided by STMicroelectronics.

1.2.3 Main results

Based on the discussion carried out in the previous section, three real-life applications which require isolated power supplies and could immediately benefit from fully integrated power transfer systems were selected to be addressed during this work as a part of a research project at the RF-ADC, a joint research center between the University of Catania and STMicroelectronics. Accordingly, during my permanence at RF-ADC four fully-integrated systems were designed and characterized in the available technology by different design teams, showing measured performance that are competitive with the state of the art. They are:

- a watt-level, step-up, dc/dc converter for gate driver's power supplies [66],
- two medium-power CMOS converters, with output power of 200 mW and 300 mW, respectively, for power supplies of general purpose circuitry [5, 19],
- a highly integrated data/power transfer system, with relatively low output power, for sensor interfaces applications [17].

Gate drivers pose the highest challenges for silicon technology, since relatively high output power with output voltage around 20 V is required. Such high-power levels entails large area to comply with technology limits and hence its design was addressed to the optimization of power efficiency for a given area constraint, exploiting high-voltage devices such as LDMOS transistors for this task, eventually.

General purpose circuitry, such as the aforementioned wireline transceivers and signal processing blocks, require lower output power and output voltages compared to gate drivers. For generic applications the reduction of technology costs is mandatory to increase the appeal of these innovative integrated systems and hence new

topologies requiring only low-cost, widespread CMOS devices were introduced in [67] and demonstrated in [5, 19].

Finally, sensor interfaces require quite lower output power, e.g. around 10-20 mW, but the need for a data link typically leads to multiple isolation transformer, thus highly affecting the cost of these systems. A new architecture was proposed in [68], which enables both data and power transfer to be implemented with a single integrated isolation transformer, thus showing a great competitive advantage with respect to the state of the art.

Details of the implementations and measured results for some of these integrated systems are the object of this thesis. Specifically, I was in charge for the design and characterization of the watt-level converter presented in [66] and of the data receiver of the data/power transfer system demonstrated in [17], which will be thoroughly discussed in Chap. 2 and Chap. 3, respectively. For each system the design was focused on the maximization of power transfer performance, which is the key parameter to understand the viability of the approach and, eventually, to determine if and which technology improvements are mandatory. Due to the lack of similar examples in literature, this activity has been a quite time-consuming task, which prevented other themes such as CMTI, thermal issues, and closed-loop control to be addressed. Further to the data receiver, the design was addressed to the maximization of robustness though novel topologies which guarantee wide operating range in terms of input signals.

Apart from these main activities, I also contributed to the implementation of the two CMOS converters with an innovative scalable lumped model [5] and by introducing the hybrid coupling for the topology adopted in [19]. These points are briefly discussed in App. B.

Chapter 2

A watt-level, step-up, power transfer system

This chapter deals with the design and the experimental characterization of a watt-level step-up dc-dc converter for gate driver's power supplies. The converter was designed to produce a 20-V output voltage, V_{OUT}, from a 5-V power supply, V_{DD}. To enable a wide range of applications, a relatively high output power of 1 W was addressed. Consequently, the maximization of power density is of utmost importance to achieve a practical, cost-effective solution. An upper bound of 10 mm^2 was chosen as a reasonable specification for the whole system area, which had a significant impact on the converter topology and design. Furthermore, the design was tailored to the maximization of power efficiency, which is another key aspect for practical implementation due to detrimental thermal effects and limited power dissipation of plastic packages.

2.1 System description

A simplified schematic of the galvanically isolated step-up converter is depicted in Fig. 2.1. The integrated transformer, T_{ISO}, is the core of the system since it performs

on-chip galvanic isolation and power transfer. In the proposed implementation it is integrated into the power oscillator chip, whereas a second die houses a full-bridge rectifier for ac-dc conversion, and the turn's ratio of the transformer is exploited to achieve the required step-up voltage conversion ratio. The oscillator chip was fabricated in a 0.35-μm BCD technology providing on-chip galvanic isolation, while the rectifier was fabricated in a 0.13-μm standard CMOS technology, both described in Sec. 1.2.

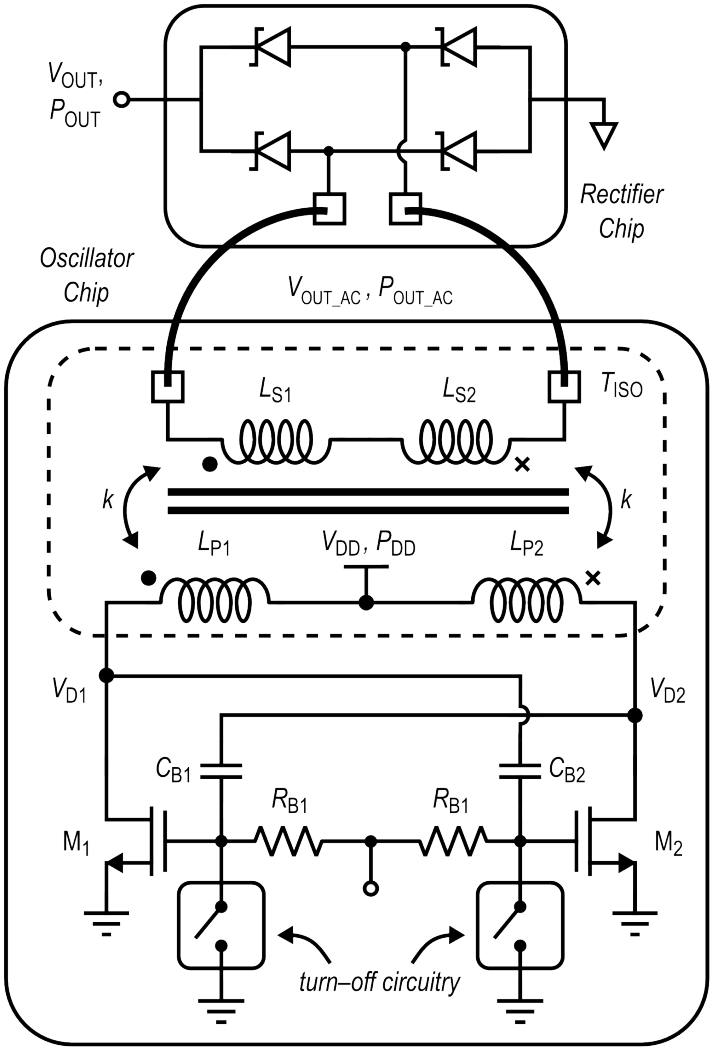


Figure 2.1. Simplified schematic of the watt-level step-up dc-dc converter.

The power oscillator adopts the transformer-loaded cross-coupled topology shown in Fig. 2.1, which is operated in class D to improve power efficiency. The need for highest power density dictates the choice of this topology that is the simplest differential transformer-loaded oscillator: only a differential transformer and two power transistors are required to implement the dc-ac conversion. Differential operation was preferred because it minimizes the impact of bonding wires and other common-mode parasitics on the system, relaxes power constraints on the transformer coils, since each coil has to deal with half the dc current, and does not require complex feedback networks to implement the oscillator, which would be the case for a single-ended topology. Simplicity maximizes the converter's power density by reducing the number of transistors and passive components, although it entails several compromises between each building blocks, which make the design optimization a quite complex problem. For example, the isolation transformer has to implement isolated power transfer while working as a resonating tank for the active oscillator core, i.e. $M_{1,2}$ and the relative bias network. Similar issues arise with the oscillator active core, which must provide the non-linear reactance required to sustain the oscillation and enough power at the transformer primary coils, but it is affected by parasitic capacitances which reduce transformer efficiency. Moreover, the converter operation is similar to the push-pull or flyback converter, which is indicated in [55] as one of the most promising topology for fully integration of galvanic isolated converters.

This topology clearly requires active devices able to sustain at least two times the supply voltage and at the same time operate at very high frequency (VHF). LDMOS transistors similar to [62], available in the adopted BCD process, were used for $M_{1,2}$. Being asymmetric devices, their maximum allowed gate-source voltage, $V_{GS,MAX}$, is smaller than the maximum drain-gate voltage $V_{DG,MAX}$, and hence capacitive coupling is exploited to avoid gate-oxide breakdown. Indeed, coupling capacitors $C_{B1/2}$ perform a voltage partition with the gate capacitance of $M_{1/2}$, thus reducing the ac voltage that is fed back from the transistor's drain nodes $V_{D1/2}$.

They were implemented with 12-V poly-poly capacitors. The transformer is modeled with coupled inductors, $L_{P1,2}$ and $L_{S1,2}$, that represent the primary and secondary coils, respectively. It is worth noting that $L_{P1,2}$ resonates with the large parasitic capacitance at the oscillator drains, $V_{D1,2}$, to maximize the oscillation frequency f_{OSC} and hence the efficiency of the transformer. Finally, a turn-off circuitry is added to switch off the cross-coupled pair. It consists of a network of NMOS switches connected between the gate of the $M_{1,2}$ and ground. A tree of buffers ensures that all the power cells are switched off reliably and almost simultaneously. The turn-off control circuitry is used to control the output power of the converter by periodically switching-off the oscillator. The VHF operating frequency actually simplifies the control of the output power without affecting power efficiency (e.g., PWM or PFM modulations) [55, 56, 58, 59, 60, 61]. Indeed, when the power oscillator is on, it operates at the maximum output power and hence with maximum efficiency, and when is off only leakage current is drawn.

A stacked configuration is used for the transformer, exploiting standard metal 3 and metal 4 for primary and secondary windings, respectively, while the lowest two metals are shunted and used for underpasses, as shown in Fig. 2.2, to minimize their series resistance. The differential topology adopted for the oscillator would suggest the use of a fully symmetric, differential, spiral configuration for the transformer. Such configuration maximizes the quality factor and reduces the area occupation of the coils but requires two underpasses at least for each inductor turn. Therefore, it is not a viable solution for power transfer applications in the adopted technology, because of the higher parasitic capacitance and series resistance of this topology. Instead, two stacked transformers were preferred, which require only two underpasses, thus simplifying the layout. A distance higher than $70\,\mu$m was found to guarantee negligible coupling effects between right and left sides of the transformer, as reported in literature [69]. Of course, high coupling factor between primary and secondary coils is mandatory for an optimized design since a low k-factor combined with the

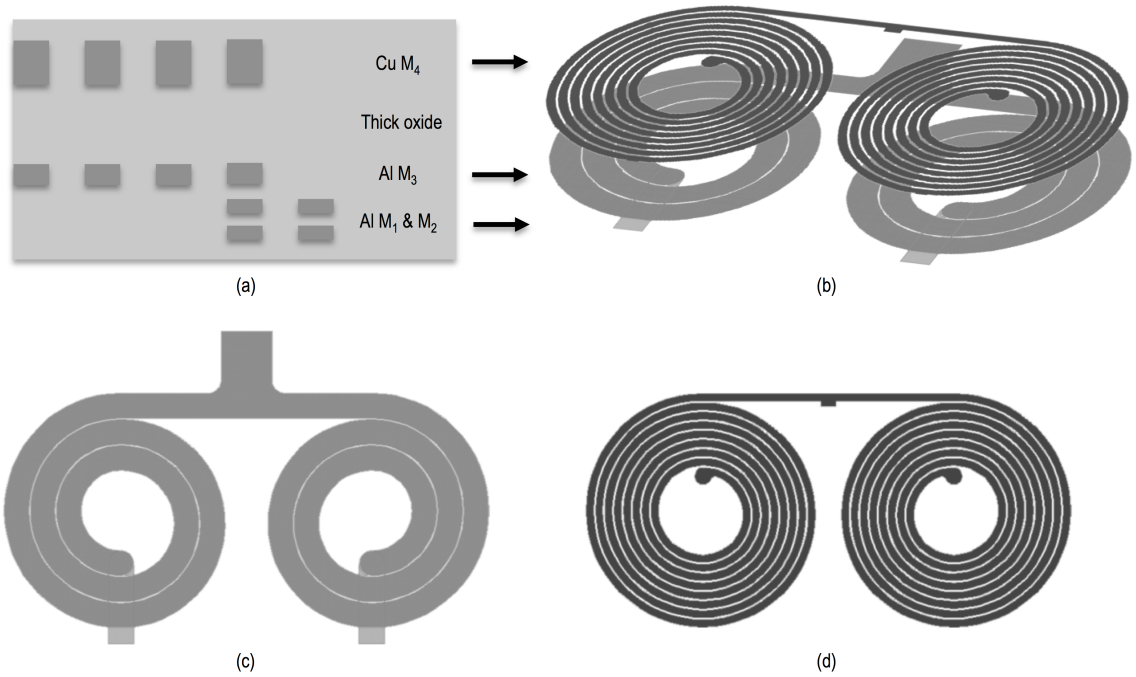


Figure 2.2. Simplified layout of the isolation transformer: (a) BEOL cross-section, (b) 3-D view of the transformer, (c) planar view of the primary coils, and (d) planar view of the secondary coils.

poor Q-factor of integrated transformers would highly affect the power transfer efficiency. Consequently, the maximization of the overlap area between primary and secondary windings is crucial to avoid magnetic coupling factor degradation [70]. Since a high transformer turn's ratio must be used to step-up the output voltage, a proper relationship between primary and secondary geometrical parameters is required to maximize winding overlap, and it was taken into account at the design time. At the secondary side, two bonding wires are used for the connection towards the rectifier chip. The impact of these bonding wires on the system performance is negligible since they are connected in series with the high inductance of $L_{S1,2}$.

2.2 Efficiency analysis and design issues

The design of this dc-dc converter poses several challenges since it is characterized by non-linear interactions between each building stage, which involve system optimization if the maximum efficiency must be addressed. Although radio-frequency (RF) class-D oscillators have recently gained attention for their excellent efficiency in highly scaled technologies, most recent literature focuses on phase noise and power consumption optimization [71, 72], whereas the design for power transfer applications is a quite different problem.

In this section we analyze how each block efficiency depends on the design parameters of the converter as well as on the loading effect of the other blocks, to better understand main issues and trade-offs between each building block design. The overall system efficiency, η, is the product of the efficiency of each building block when operated into the whole system. Specifically, the power flow from the power supply, P_{DD}, to the dc power delivered to the load, P_{OUT}, involves losses in the active devices, in the integrated transformer, and in the rectifier, as detailed in the flow diagram of Fig. 2.3. Here P_{TX} is the total power at the transformer input coils,

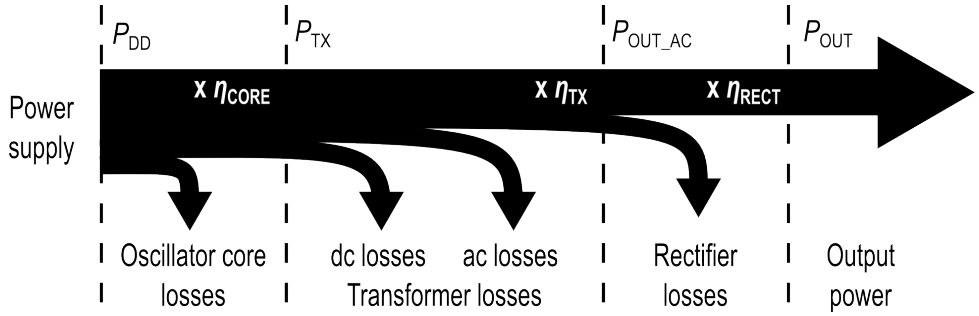


Figure 2.3. Power transfer flow diagram.

and P_{OUT_AC} is the ac power at the transformer output. The rectifier efficiency, η_{RECT}, is defined as P_{OUT}/P_{OUT_AC}, while the overall efficiency of the transformer, η_{TX}, is defined as P_{OUT_AC}/P_{TX}. We also define the active core efficiency, η_{CORE},

as P_{TX}/P_{DD}:

$$\eta_{RECT} = \frac{P_{OUT}}{P_{OUT\_AC}} \tag{2.1}$$

$$\eta_{TX} = \frac{P_{OUT\_AC}}{P_{TX}} \tag{2.2}$$

$$\eta_{CORE} = \frac{P_{TX}}{P_{DD}} \tag{2.3}$$

Starting from the rectifier, the power efficiency of each block is analyzed in the following as a function of main characteristics of the other blocks.

2.2.1 Rectifier

The rectifier performs the ac-dc conversion. It receives the ac power P_{OUT_AC} and produces the output dc power P_{OUT}. Each diode in the bridge is implemented by using several elementary diode cells connected in parallel. The adopted high-voltage Schottky diode has an elementary active area of $100\,\mu\text{m}^2$. This block can be characterized by the conversion efficiency η_{RECT} and its input impedance, Z_{RECT}, which can be conveniently described as a parallel RC circuit, $R_{RECT}//C_{RECT}$. At a given power and voltage level, both are highly affected by the number of elementary diode cells, M.

Of course rectifier efficiency depends on the output power, P_{OUT}, as shown in Fig. 2.4(a), where η_{RECT} vs. P_{OUT} is reported for M between 10 and 50 with a 250-MHz input signal and 20-V V_{OUT}. For increasing power levels a higher number of diode cells is required to do not compromise the efficiency performance. The input resistance shown in Fig. 2.4(b) is inversely proportional to P_{OUT} and increases with M, whereas the input capacitance shown in Fig. 2.4(c) is almost constant with M and does not depend on P_{OUT}. P_{OUT} is fixed for this system by the peak output power required, i.e. 1 W.

For the sake of clarity, Table. 2.1 summarizes simulated η_{RECT} and Z_{RECT} for different values of M at the target P_{OUT} of 1 W. It is apparent that a small efficiency

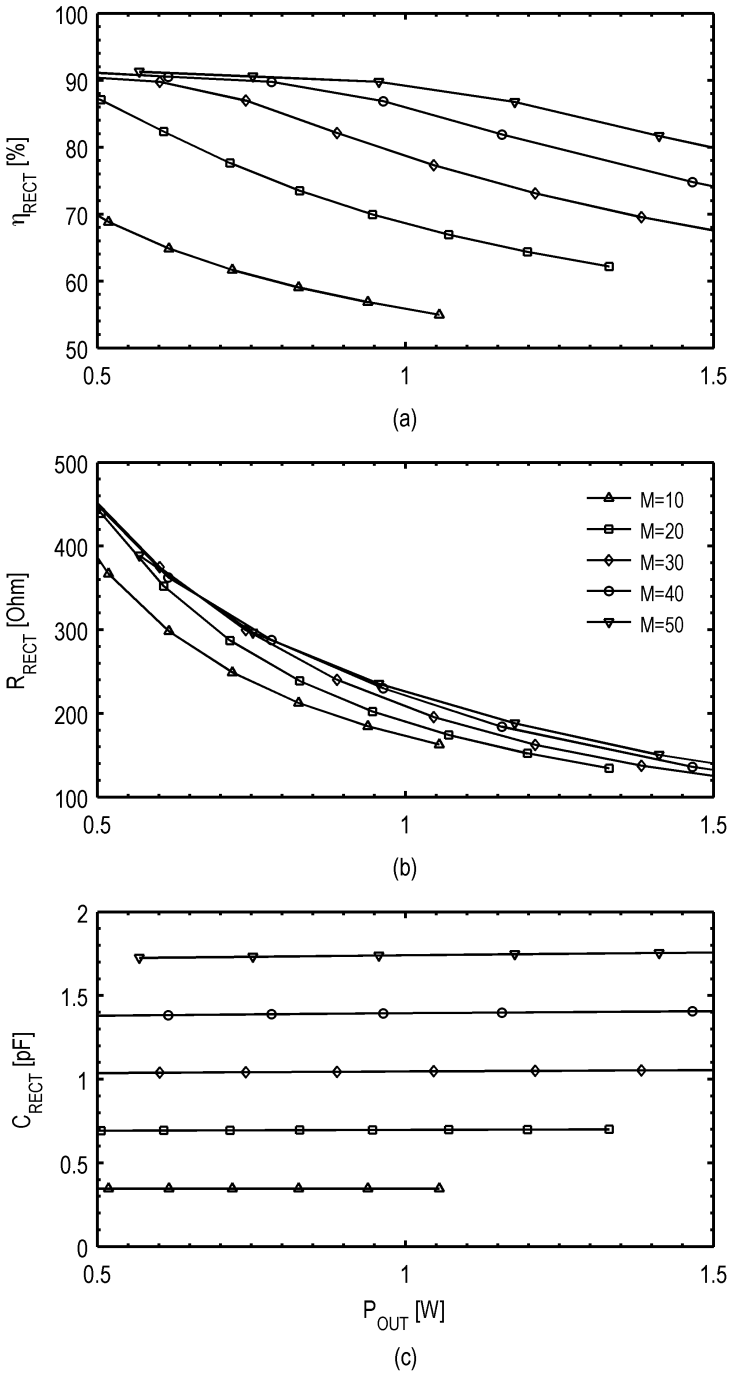


Figure 2.4. Rectifier efficiency as a function of the output power for different diode multiplicity, M.

Table 2.1. Simulated rectifier performance, $V_{OUT} = 20\,\mathrm{V}, P_{OUT} = 1\,\mathrm{W}$

	M	$\eta_{RECT}[\%]$	$R_{RECT}[\Omega]$	$C_{RECT}[pF]$
Schematic	10	56	173	0.35
	20	69	192	0.69
	30	80	211	1.04
	40	87	222	1.37
	50	90	226	1.73
Post-layout	40	82	219	3.58

improvement can be obtained for $M > 40$ at the cost of increased rectifier area and, most importantly, routing complexity.

M was set to 40 to tradeoff η_{RECT} with C_{RECT}. This choice takes into account the fact that this block can easily provide high efficiency when compared to other blocks in the chain. Another important design issue is represented by the rectifier layout: parasitics due to metal connections highly affect efficiency performance and the input capacitance, especially when a high number of elementary cells must be connected. Main degradation of efficiency comes from the resistive parasitics, which were minimized by exploiting all the available metal layers (i.e., metal 1 to metal 4 plus alucap) and optimizing the number of vias.

Finally, a 180-pF output filter metal-oxide-metal capacitor was also integrated in the rectifier chip. Simulations show that for operating frequencies smaller than 400 MHz the rectifier characteristics are quite constant, and therefore it was modeled by an input impedance Z_{RECT} of $220\,\Omega//3.6\,\mathrm{pF}$ for $P_{OUT\_AC} = 1.25\,\mathrm{W}$.

2.2.2 Isolation transformer

The efficiency of the integrated isolation transformer, η_{TX}, is intrinsically difficult to analyze when operated in this topology because it also depends on the dc current flowing into the coils, apart from the load impedance Z_{RECT} and the geometrical design parameters of the coils, thus complicating both analysis and design of the

system.

Transfer efficiency

It is convenient to split the power at the transformer input into a dc and an ac component:

$$P_{TX} = P_{TX\_DC} + P_{TX\_AC} \tag{2.4}$$

For the sake of simplicity, we will neglect for the moment dc losses on the transformer, represented by P_{TX_DC}, and we will thus focus on its transfer efficiency, η_{TX_AC}, that can be defined as:

$$\eta_{TX\_AC} = \frac{P_{OUT\_AC}}{P_{TX\_AC}} \tag{2.5}$$

It only depends on the transformer characteristics and on the rectifier impedance and hence it characterizes the intrinsic maximum power transfer efficiency of the loaded transformer. Incidentally, it corresponds to the S_{21} parameter if measured with matched load and source impedances at the transformer ports. The effect of dc losses will be discussed later.

The relationship between geometrical and electrical parameters is another quite complex task itself, that will be discussed afterwards in the design section, Sec. 2.3, therefore we will only discuss the effect of electrical parameters and load impedance on the transfer efficiency. For a qualitative understanding on how they affect the power transfer efficiency, the simple linear lumped transformer model in Fig. 2.5 can be used as a starting point. The transformer is here modeled by coupled inductors, L_P and L_S, with finite coupling factor k and finite series resistances, R_P and R_S. It is loaded by the single-ended rectifier input impedance at the secondary coils. This model is commonly used in literature to evaluate efficiency and input impedance of an RC loaded transformer, however direct calculations are quite cumbersome, whereas simple expressions found in literature are often inadequate since they are calculated in special matching conditions, for relatively high Q-factors, and/or in the

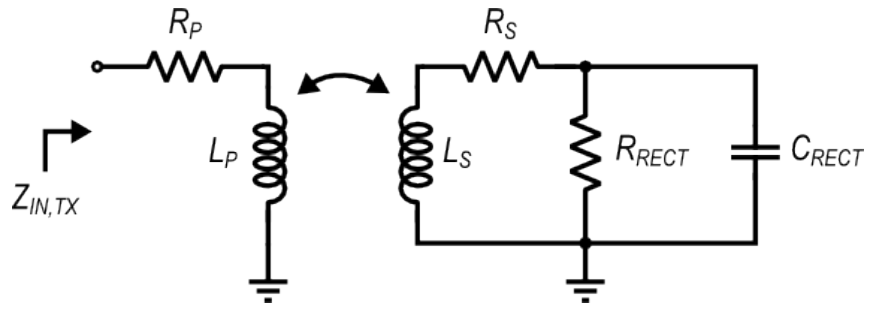


Figure 2.5. Linear lumped transformer model.

nearing of resonance [73, 74]. They are widely used in discrete transformer-loaded circuits, but they are not suited for this context, where matching is not possible and a wide-band evaluation is desirable. Therefore, the following simplified expressions can be used, whose derivation is shown in Appendix A:

$$\eta_{TX\_AC} \approx \frac{\omega Q_{EQ} L_{EQ} \times \frac{R_{RECT}}{R_{RECT}+R_S} \times \frac{1}{(1+\omega^2 C_{EQ}^2 R_S R_{RECT})}}{\omega Q_{EQ} L_{EQ} \left(1+\frac{R_P}{R_{EQ}}\right) + R_{EQ}\left(\omega^2 L_{EQ} C_{EQ} - 1\right)^2}, \tag{2.6}$$

$$Z_{IN,TX} \approx R_P + j\omega(1-k^2)L_P + \left(j\omega k^2 L_P\right) // \left(\frac{R_{EQ}}{1+j\omega C_{EQ} R_{EQ}}\right), \tag{2.7}$$

where

$$\begin{aligned} n &= \frac{1}{k}\sqrt{\frac{L_S}{L_P}}, \\ R_{EQ} &= \frac{R_{RECT}+R_S}{n^2}, \\ C_{EQ} &= C_{RECT} \times \frac{R_{RECT}}{R_{RECT}+R_S} \times n^2, \\ L_{EQ} &= L_P \times k^2, \\ Q_{EQ} &= \frac{\omega L_{EQ}}{R_P}, \end{aligned} \tag{2.8}$$

and $Z_{IN,TX}$ is the input impedance of the loaded transformer. Equations 2.6 and 2.7 are quite intuitive since the effect of both electrical parameters and load impedance is taken into account. As expected, maximization of transfer efficiency entails high coupling factor and minimum series resistances or maximization of the ωQL product

of the transformer coils, especially the primary one. A peak due to the parallel output resonance can be recognized, for frequencies approaching the resonant frequency of the secondary coil, $f_{RF2} \approx 1/2\pi\sqrt{L_{EQ}C_{EQ}} = 1/2\pi\sqrt{L_S C_{RECT}}$. At the increasing of R_{RECT} efficiency reduces, whereas it increases with C_{RECT} for a given frequency, since higher C_{RECT} moves to lower frequency the peaking due to f_{RF2}. The input impedance Eq. 2.7 suggests that a simple RLC model with series resistance can be also used for further simplified calculations. Of course, neglecting the series resistance by using a simplified series-to-parallel transformation is not possible due to the relatively poor quality factor of the primary coils inductance: apart from affecting the oscillator core operation, the series resistance highly affects the transfer efficiency and a narrow-band parallel representation is not adequate to model the transformer impedance and efficiency. A second series resonant frequency is also recognized, due to the series connection of $(1 - k^2)L_P$ and C_{EQ}, that is pushed to very high frequencies for high coupling factors.

Typical curves of η_{TX_AC} for an actual integrated transformer are shown in Fig. 2.6 to follow this qualitative description. Transformer matrix parameters here are extracted from electro-magnetic simulations[1], and efficiency is plotted as a function of frequency, for three increasing R_{RECT} of 150 Ω, 200 Ω, and 250 Ω and three increasing C_{RECT}, i.e. 0.1 pF, 3.6 pF, and 10 pF. It is worth noting that for a given R_{RECT} the peak efficiency changes less than five percentage points with C_{RECT}, which means that high C_{RECT} is not itself a problem for efficiency, whereas its main detrimental effect is the increase of the sensitivity of η_{TX_AC} with respect to the operating frequencies, due to the increased quality factor of the secondary coil's tank.

Although accurate with respect to the model in Fig. 2.5, Equations 2.6 and 2.7 fail to approximate actual transformer characteristics in Fig. 2.6: as well-known,

[1]Geometrical parameters of this transformer are reported in Table. 2.3.

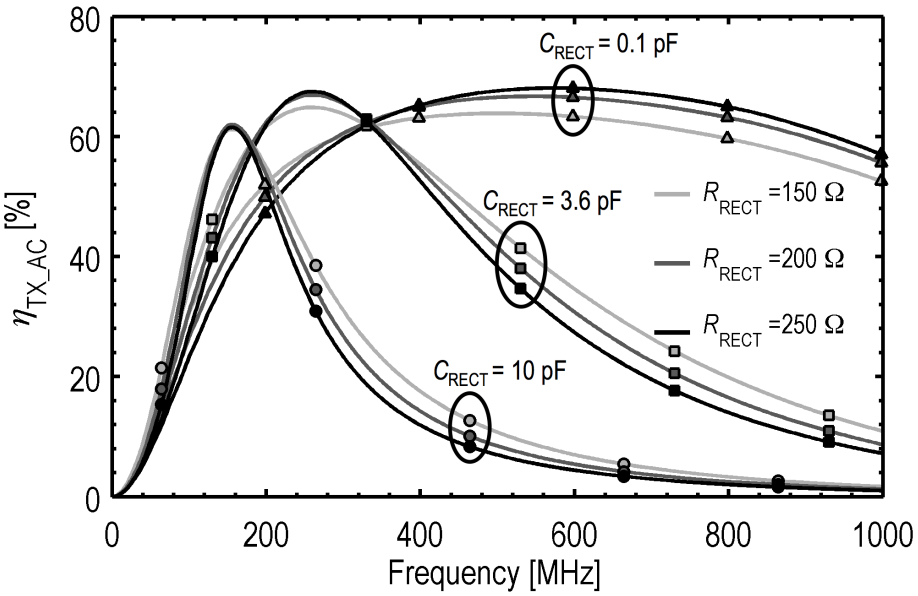


Figure 2.6. Typical power transfer efficiency, η_{TX_AC}, for an integrated transformer.

in the context of RF/IC design these formulae prove of little help, due to the high discrepancy of linear lumped models with respect to actual measured data or electromagnetic (EM) simulations of integrated passive devices. Moreover, it is well-known that integrated transformers exhibit best performance when operated in resonance, i.e. relatively close to their self-resonant frequency, where the simple linear lumped model in Fig. 2.5 is furthermore inadequate [54], and modeling through frequency-dependent matrix parameters is mandatory to achieve sufficient accuracy for power efficiency evaluation [75].

The key points of this chart and more generally of this analysis of transfer efficiency can be summarized as follows. Integrated transformers can provide sufficient transfer efficiency only in the nearing of the resonance frequency f_{RF2}. Apart from coupling and quality factors, maximum efficiency shows a certain dependence on the rectifier load, but the key variable which defines its final value is without any

doubt the operating frequency. With these considerations in mind, it is worth noting that, in a real system, a parallel parasitic capacitance, say C_P, is always present at the primary coils input port, for example due to the oscillator active core parasitics. Although the frequency behavior of η_{TX_AC} does not depend on C_P, its actual value in our system is defined by the operating frequency of the oscillator, f_{OSC}[2]: this frequency is always much lower then f_{RF2}, due to the unavoidable C_P that contributes to the actual f_{OSC} by resonating with the equivalent inductance at primary coils (e.g. around L_{EQ}). Indeed, to sustain the oscillation the input impedance must show inductive behavior, that is true only for $f << f_{RF2}$ according to Eq. 2.7. Therefore, C_P plays a key role in defining the transfer efficiency, and it is mandatory to avoid any excess capacitance at the primary side of the transformer, which further reduces f_{OSC} and hence η_{TX_AC}.

Overall transformer efficiency

Finally, the role of dc losses must be mentioned for the evaluation of the overall transformer efficiency η_{TX}. Although ac losses due to R_P are already taken into account into the evaluation of transfer efficiency η_{TX_AC}, this is not the same for the dc losses, which depend on the dc current drawn from the oscillator, I_{DD}, and that can be calculated as:

$$P_{TX\_DC} = \frac{R_P}{2} \times I_{DD}^2. \tag{2.9}$$

Taking these losses into account, the overall transformer efficiency becomes:

$$\eta_{TX} = \frac{P_{OUT\_AC}}{P_{TX\_AC} + P_{TX\_DC}} = \frac{\eta_{TX\_AC}}{1 + \frac{P_{TX\_DC}}{P_{TX\_AC}}} \tag{2.10}$$

DC losses hence further reduce transformer efficiency and the amount of reduction depends on how much dc current is required by the oscillator core to produce the ac

[2]Of course most of the output power towards the rectifier is transferred to the load through the first harmonic, f_{OSC}.

input power P_{TX_AC}. This aspect will be discussed in the following together with the active core efficiency.

2.2.3 Oscillator core

The efficiency of the oscillator core, η_{CORE}, is the third and last parameter which must be analyzed to understand how this system works and what mainly limits the power efficiency performance for a given technology.

Oscillator modeling

It is worth nothing that a realistic description of the loading tank is a key issue for this topology. Indeed, when working in class D, as well as in any other switched-mode operating class, this pseudo-differential oscillator operates in voltage-controlled mode, due to the absence of a tail current generator: the large-signal and non-linear operation of the switching transistors produces an extra current with respect to the dc current defined by the biasing voltage V_B, which therefore cannot control the current consumption[3] of the oscillator, I_{DD}. Current consumption and operating conditions are completely defined by transistor's characteristics and, especially, by the load impedance. The higher the load impedance the lower the current consumption of the oscillator and hence the power delivered to the tank, which corresponds to P_{TX} as defined in Eq. 2.4.

Accordingly, a simplified but yet realistic schematic of the transformer-loaded oscillator is shown in Fig. 2.7 for a qualitative analysis. Here the transformer and the cascaded rectifier are modeled with their equivalent input impedance as seen by the oscillator, that is a parallel RLC circuit connected in series with R_P[4], i.e.

[3] As it happens, more generally, for every non-linear dynamic circuit in open-loop operation, as discussed in [18] for example.

[4] The small series inductance required by Eq. 2.7 is neglected in this model for the sake of simplicity.

the series resistance of the primary coil, as described by Eq. 2.7. This equivalent circuit actually forms the resonating tank of the oscillator. The RLC circuit is

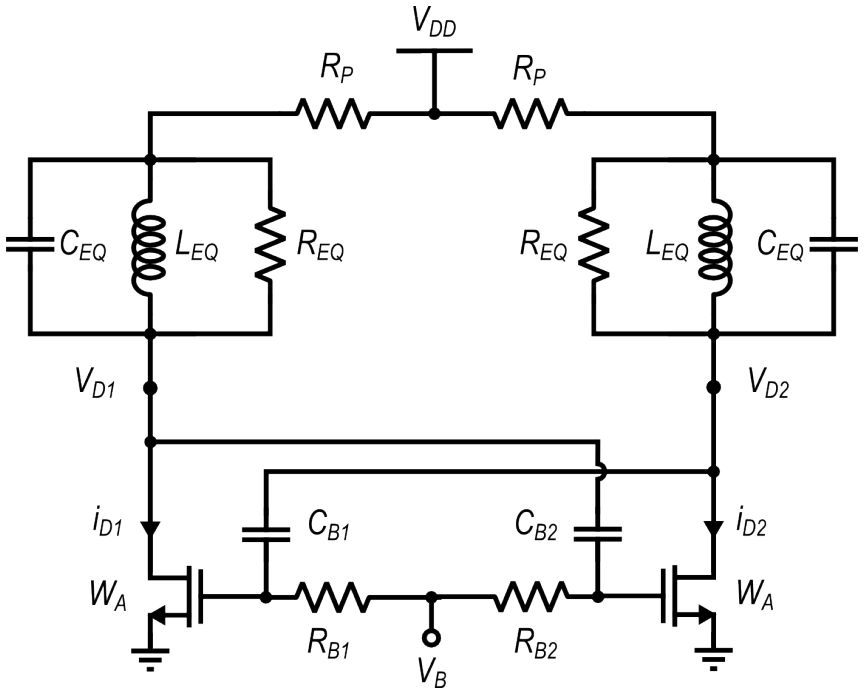


Figure 2.7. Simplified equivalent circuit of the dc-ac converter.

defined by R_{EQ}, L_{EQ}, and C_{EQ} as defined in Eq. 2.8, and models both primary inductance and the reflected impedance from the secondary side. As well-known, R_{EQ} defines the load impedance of the RLC circuit at its resonant frequency, f_0, that is $1/2\pi\sqrt{L_{EQ}C_{EQ}}$. The 3-dB impedance-bandwidth around f_0 is defined by the quality factor of the tank *at the resonance frequency* f_0, Q_{EQ}, which can be expressed as $R_{EQ}/\sqrt{L_{EQ}/C_{EQ}}$. In the following we describe how the oscillator performance changes as a function of the resonating tank characteristics for the available LDMOS devices. For a general analysis, all passive component values have been normalized with respect to transistor's width W_A, i.e. per millimeter. An arbitrary resonant frequency f_0 of 250 MHz was chosen for these simulations, which does not limit the qualitative results of the analysis. Firstly we set $R_P = 0\,\Omega/\text{mm}$ to study how the

parallel RLC tank affects the oscillator operation, then we add the effect of finite R_P.

Oscillator performance - $R_P = 0\,\Omega/\mathrm{mm}$

A useful approximate expression for η_{CORE} is the following

$$\eta_{CORE} \approx 1 - 2\frac{P_{M1,2}}{P_{DD}} \tag{2.11}$$

where $P_{M1,2}$ is the power loss in each power transistor $M_{1,2}$, i.e. the average value of $v_{D1/2} \times i_{D1/2}$, calculated over the oscillating period $T_{OSC} = 1/f_{OSC}$. According to this definition, for high efficiency the transistors should work as ideal switches, which means that drain current $i_{D1/2}$ should be zero with high $v_{D1/2}$, whereas we want low $v_{D1/2}$ when $M_{1/2}$ is on and carries high current, to minimize $P_{M1,2}$. In these preferred operating conditions, when the transistor is off the dynamic of the tank is governed by the RLC equations, while the voltage across the coil is almost constant when each transistor is on. This means that current from the capacitor C_{EQ} is relatively low in this phase, and the transistor's drain current $i_{D1/2}$ is mostly due to L_{EQ} and R_{EQ}. Therefore, to reduce transistor's losses the additional current from the inductor must be low, so we expect higher efficiency with higher L_{EQ}/C_{EQ} ratio, for a fixed tank resonant frequency f_0. Moreover, in these conditions, during current conduction a resistive division takes place between the on-resistance of the transistors, $R_{1,2}$, and the loss resistance of the tank R_{EQ}, therefore we expect for the peak efficiency to increase with R_{EQ} for a given W_A.

Fig. 2.8 shows the efficiency of the oscillator core, η_{CORE}, as a function of the ratio L_{EQ}/C_{EQ} for different R_{EQ}. First we set $L_{EQ} = 10\,\mathrm{nH/mm}$ and adjust the capacitance C_{EQ} to obtain f_0. These values are taken as reference value, i.e. they correspond to $L_{EQ}/C_{EQ} = 1\,\Omega^2/\mathrm{mm}^2$ in the chart. Then L_{EQ} is increased (reduced) while C_{EQ} is reduced (increased) to maintain the same product while increasing (reducing) L_{EQ}/C_{EQ} up to $30\,\Omega^2/\mathrm{mm}^2$ (down to $0.1\,\Omega^2/\mathrm{mm}^2$). We see that, for

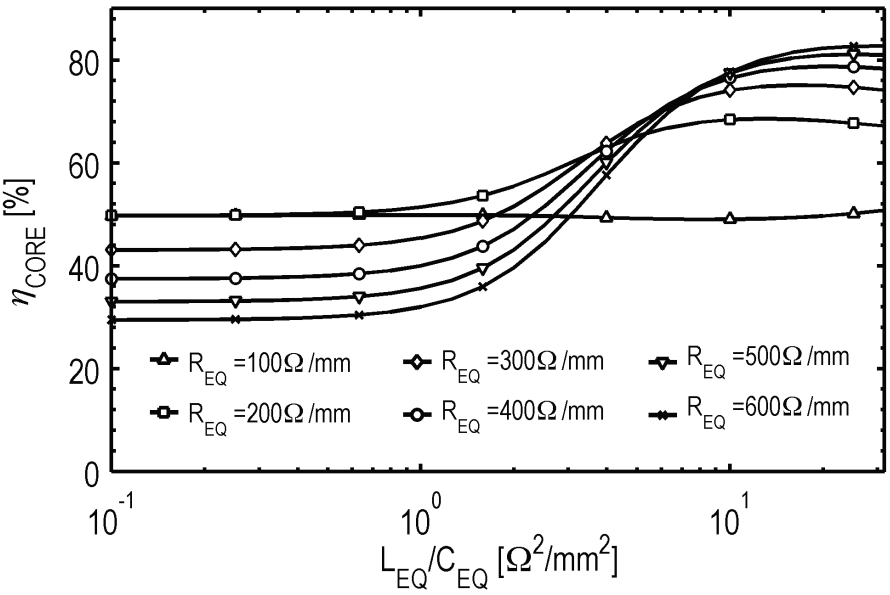


Figure 2.8. Oscillator performance as a function of L_{EQ}/C_{EQ} for $R_P = 0\,\Omega$/mm.

$R_{EQ} = 100\,\Omega$/mm, efficiency approaches 50% and does not depend on L_{EQ}/C_{EQ}. Indeed, in this case R_{EQ} is so low that class-D operation is not achieved and the oscillator operates in class A, with voltage waveforms approaching sinusoids and a relatively high on-resistance $R_{1/2}$ with respect to R_{EQ}. For low L_{EQ}/C_{EQ} the oscillator waveforms are still sinusoids: in this operating point the peak voltage is limited by V_{DD} and higher R_{EQ} reduces the power delivered to the tank P_{TX} faster than the power absorbed from the supply voltage, P_{DD}, thus reducing efficiency with R_{EQ}. This is due to the fact that $R_{1/2}$ is relatively constant and higher than R_{EQ} as long as the oscillator waveforms remain sinusoidal. However, for $L_{EQ}/C_{EQ} > 7\,\Omega^2/\text{mm}^2$ the waveforms change and efficiency starts increasing with R_{EQ}. Higher L_{EQ}/C_{EQ} reduces the quality factor of the resonator, thus increasing the impedance around f_0: this enables the addition of higher voltage harmonics at the transistor's drain, which reduce both the transistor's on-resistance and the current consumption I_{DD}. Therefore, as expected, efficiency increases with the L_{EQ}/C_{EQ} ratio, and

peak efficiency mainly depends on R_{EQ}. Finally, an optimum R_{EQ} exists in these conditions which is shown in Fig. 2.9, where η_{CORE} is plotted as a function of R_{EQ} for $L_{EQ}/C_{EQ} = 20\,\Omega^2/\mathrm{mm}^2$. Indeed at the increasing of R_{EQ} the power delivered to the tank becomes comparable with parasitic losses within the active core and, eventually, efficiency reduces again.

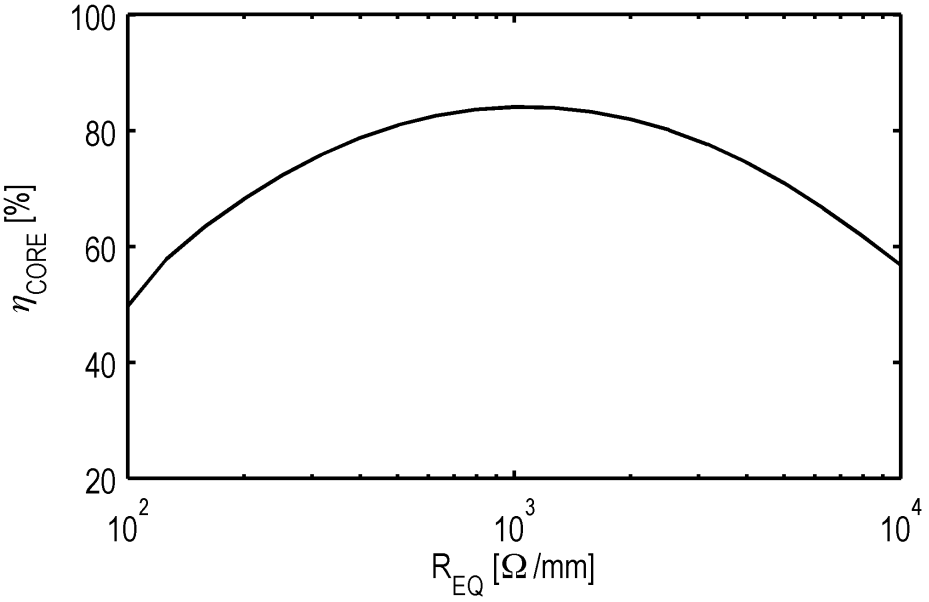


Figure 2.9. Oscillator performance as a function of R_{EQ} for $L_{EQ}/C_{EQ} = 20\,\Omega^2/\mathrm{mm}^2$.

Another fundamental characteristic of this operating mode, that is actually the other side of the picture of class D operation, is the reduction of operating frequency, f_{OSC}, with respect to the self-resonant frequency of the load, f_0. This is shown in Fig. 2.10, where f_{OSC} is shown to change as a function of L_{EQ}/C_{EQ} for different R_{EQ}. The lower the quality factor of the oscillator, the higher is the difference between f_0 and f_{OSC}. This is a well-known effect described by Groszkowski in 1933 for oscillators operating with multiple harmonics [72], and it is cross-linked to the higher efficiency of the topology. Specifically, for a tank with mainly single-ended capacitance as in this case, f_{OSC} is typically lower than f_0, as confirmed by

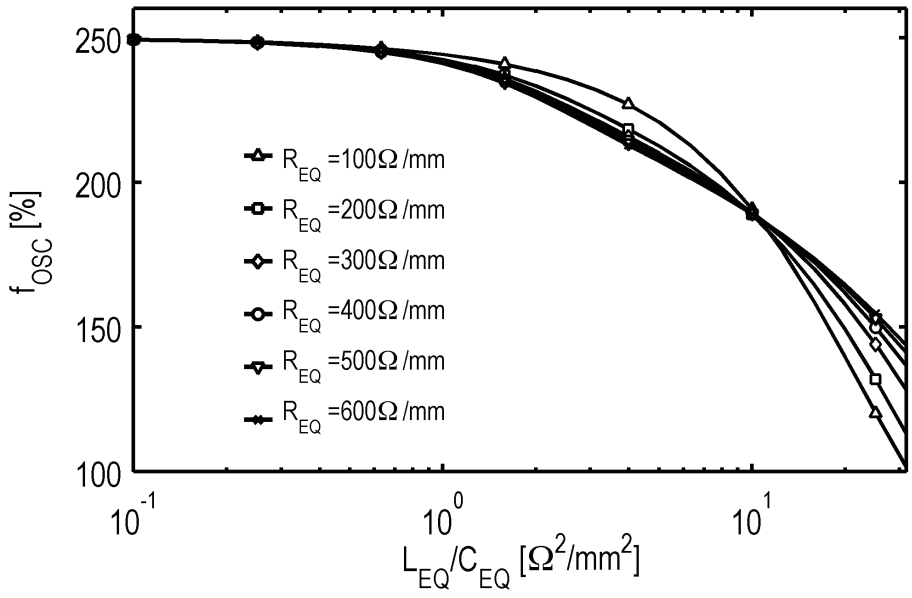


Figure 2.10. Oscillation frequency f_{OSC} as a function of L_{EQ}/C_{EQ} for several R_{EQ}.

theoretical analysis reported in [71]. It is worth noting that if L_{EQ}/C_{EQ} is made very high to increase the active core efficiency, C_{EQ} may become comparable or lower than the active core intrinsic capacitance, say C_P, that is due to transistor's parasitics as well as to the contribution of bias capacitors C_B[5]. Eventually, all of these capacitive contribution from the active core may limit the oscillation frequency for a given RLC equivalent tank, i.e. for a transformer and rectifier implementation.

Oscillator performance - $R_P \neq 0\,\Omega/\mathrm{mm}$**.**

The effect of finite dc resistance R_P must be taken into account for a complete description of system trade-offs. Simulations for increasing R_P are shown in Fig. 2.11 for $L_{EQ}/C_{EQ} = 20\,\Omega^2/\mathrm{mm}^2$. As expected from the previous analysis for $R_P = 0\,\Omega/\mathrm{mm}$, with increasing R_P the efficiency of the active core (defined in Eq. 2.3 as the

[5]Indeed biasing capacitors here are not negligible since in this topology they form a capacitive divider with the transistor's gate capacitances.

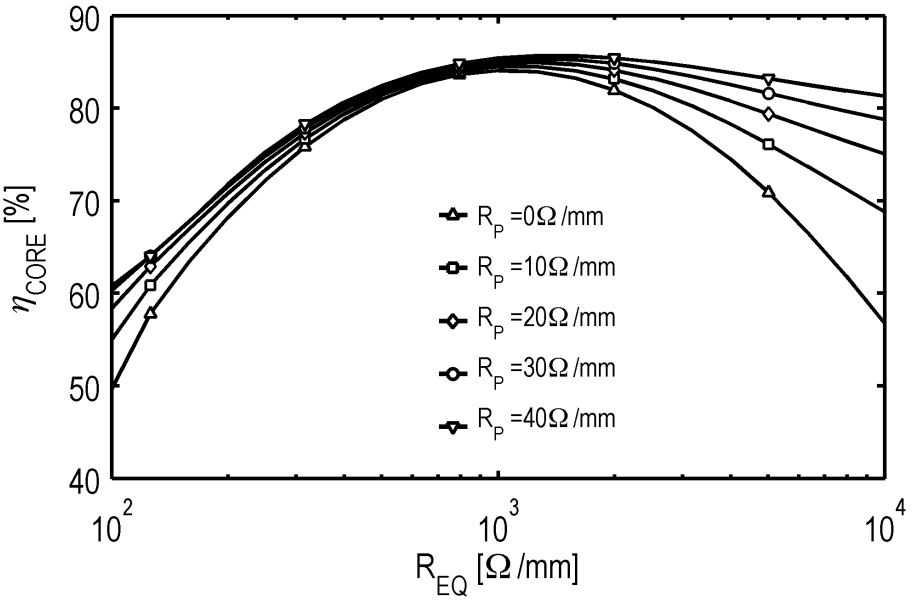


Figure 2.11. Oscillator performance as a function of R_{EQ} for $L_{EQ}/C_{EQ} = 20\,\Omega^2/\mathrm{mm}^2$.

power delivered to the tank with respect to the overall power consumption) increases, provided that L_{EQ}/C_{EQ} is high enough. However, from a system perspective, higher R_P means higher losses in the transformer due to both ac and dc currents and it must be minimized.

It is interesting to see how the power delivered to the tank, P_{TX}, divides between its dc and ac components, which can be described using the following ratio:

$$\eta_{AC/DC} = \frac{P_{TX\_AC}}{P_{TX\_AC} + P_{TX\_DC}}. \tag{2.12}$$

It depends on both resonating tank and active core[6]. Using this definition the overall transformer efficiency, Eq. 2.10, can be expressed as

$$\eta_{TX} = \eta_{TX\_AC} \times \eta_{AC/DC}, \tag{2.13}$$

[6]Keep in mind that the oscillator analysis is performed in terms of *normalized* (Ω/mm) tank impedance.

which highlights how the oscillator operation further affects the transformer performance besides defining the operating frequency. Fig. 2.12 shows $\eta_{AC/DC}$ ratio correspondent to the simulations in Fig. 2.11. Lower R_{EQ} for the resonating tank

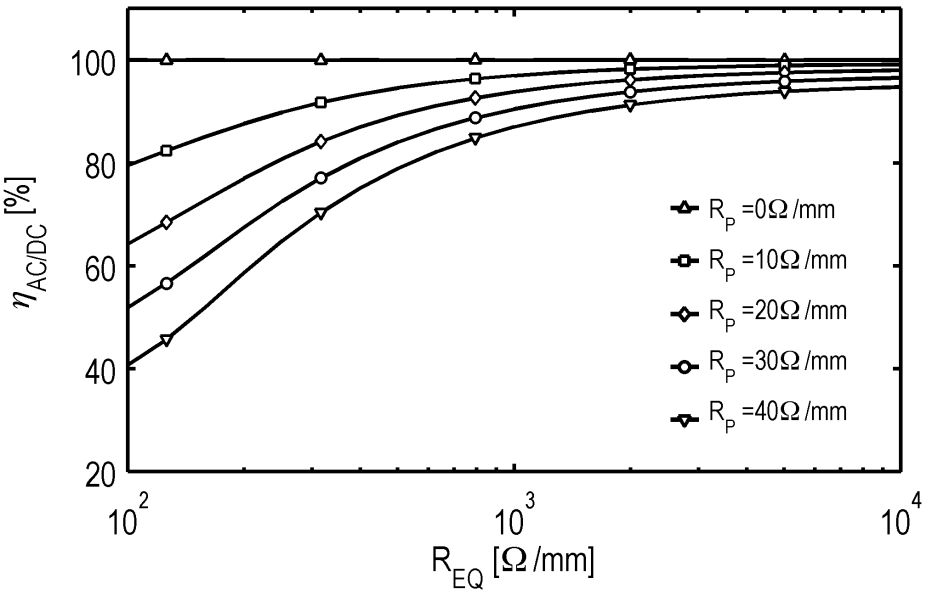


Figure 2.12. Oscillator P_{TX_AC}/P_{TX} as a function of R_{EQ} for $L_{EQ}/C_{EQ} = 20\,\Omega^2/\mathrm{mm}^2$.

mandates lower R_P to do not compromise the transformer efficiency. However in a physical implementation for power transfer R_{EQ} mainly depends on the rectifier impedance and secondary coils design, whereas absolute value of R_P depends on the primary coils and therefore their ratio is limited by the technology BEOL. Finally, both resistances also directly affect the transformer efficiency according to Eq. 2.6, and active core efficiency according to simulations in Fig. 2.8 to 2.11.

2.2.4 Design issues

The analysis carried out in this section is helpful to understand the role of each block and the impact of each block electrical parameter on the efficiency of the other blocks. The main design goal is obviously the maximization of system efficiency.

The rectifier is the simplest block in this context, which shows a well-defined and direct relationship between its size, M, and both power efficiency η_{RECT} and input capacitance C_{RECT}. Consequently, even R_{RECT} increases for a given output voltage and output power.

The transformer response was analyzed in terms of transfer efficiency η_{TX_AC} and input impedance $Z_{TX,IN}$ as a function of rectifier input impedance and transformer's electrical parameters. Of course maximization of quality factors and coupling factors is mandatory and both depend on geometrical parameters but mainly on the available BEOL. Operating frequency must be kept as close as possible to the resonant frequency made up by the secondary coil and the rectifier capacitance, f_{RF2}. Rectifier loading mainly affects η_{TX_AC} through its input capacitance, by moving this peak to lower frequency while shrinking the high-efficiency bandwidth.

The active oscillator core is finally shown to be the most complex and important block in the chain. Its non-linear behavior requires a relatively high tank inductance and minimum external capacitance for a given transistor's width W_A to operate with high efficiency. However high-efficiency operation mandates both low power density, which increases the capacitance C_P seen by the transformer, and a reduction of the oscillating frequency f_{OSC} towards lower frequencies, when compared with the natural resonant frequency at the transformer input, f_0. Both phenomena reduce the transfer efficiency of a given transformer.

Finally, the effect of finite dc resistance of the transformer is shown to increase the active core efficiency while further reducing transformer efficiency, and its exact impact on the latter depends on both transformer and oscillator's characteristics too.

Analytical description of all of these relationships would be quite complex and hence provide very few advantages for system design of this topology. Moreover, these considerations confirm that no significant result can be achieved by designing each system block as a stand-alone circuit. Instead, optimum performance can

be obtained by adopting an iterative co-design procedure between the converter building blocks. Eventually, a proper design strategy is mandatory to perform this co-design due to the large number of free design variables.

2.3 System design

Based on the previous analysis, a co-design procedure was developed, which accounts for main interactions between the dc-dc converter building blocks. It starts from the most important design specification for an integrated dc-dc converter that is its power density, i.e. the ratio of delivered output power to the area occupation: large area entails higher production costs for the IC, which can be partially compensated in many applications by the ease of use of an integrated solution and its reduced board space. At the very end, in most cases costs decide if an integrated solution should be preferred with respect to a traditional discrete counterpart, and therefore an upper bound of $10\,\mathrm{mm}^2$ was set for the overall converter area. This is a quite ambitious target for an integrated inductive step-up converter, which implies a power density of $100\,\mathrm{mW/mm}^2$ for the target power of $1\,\mathrm{W}$ that is not currently reported in the state of the art even for non-isolated implementations.

Power density limits the geometrical design space for the isolation transformer, which is the most area-hungry part of this systems due to constraint on both dc resistance and quality factors for the coils. Although a customized design of the transformer is mandatory to maximize system efficiency, tools for co-simulation between circuital and EM design were not available in the adopted design kit. Therefore a lumped geometrically scalable model of the integrated transformer T_{ISO} was developed and is presented in this section as a fundamental tool for the design of the converter, thus enabling the use of simple parametric circuit simulations to efficiently explore the design space.

Then the co-design procedure adopted for the converter is presented. Its main

purpose is the optimization of the dc-ac conversion efficiency at a given power density, which means optimum co-design between power transistors and isolation transformer in the oscillator. By taking advantage of the aforementioned model, several feasible design configurations for the whole dc-dc converter were found by properly exploring the design space. These solutions were refined by iterating the design procedure and using EM simulations for the transformer only to check the best results. Finally, starting from the best solutions, the system design was completed for integration by also taking into account main electromagnetic (EM) and layout parasitic effects. A similar design procedure was also used in [5], with a proper lumped geometrically scalable model described in Appendix B.2.

2.3.1 Modeling of the stacked isolation transformer

Lumped scalable modeling of integrated transformers has been a research theme since long time, and it is clear that there is no easy way to estimate the key electrical parameters of the transformer starting from geometrical parameters, while providing the required accuracy for power efficiency evaluation in a wide range of design parameters [54]. This accuracy can be obtained by using parametric EM simulations, which however imply high computational effort and long design time.

In the proposed design procedure, the transformer (see Fig. 2.2) was modeled by means of the geometrically scalable lumped model shown in Fig. 2.13, which represents only its half structure, i.e. the single-ended configuration. This approach provides higher level of accuracy with respect to simpler models [74], without the computational costs of EM simulations. As discussed in the previous section, widely adopted formulae developed for transformer-loaded discrete circuits are not useful for this application due to both complex loss and EM coupling mechanisms on silicon [75].

The model in Fig. 2.13 exploits a π-like configuration with scalable expressions

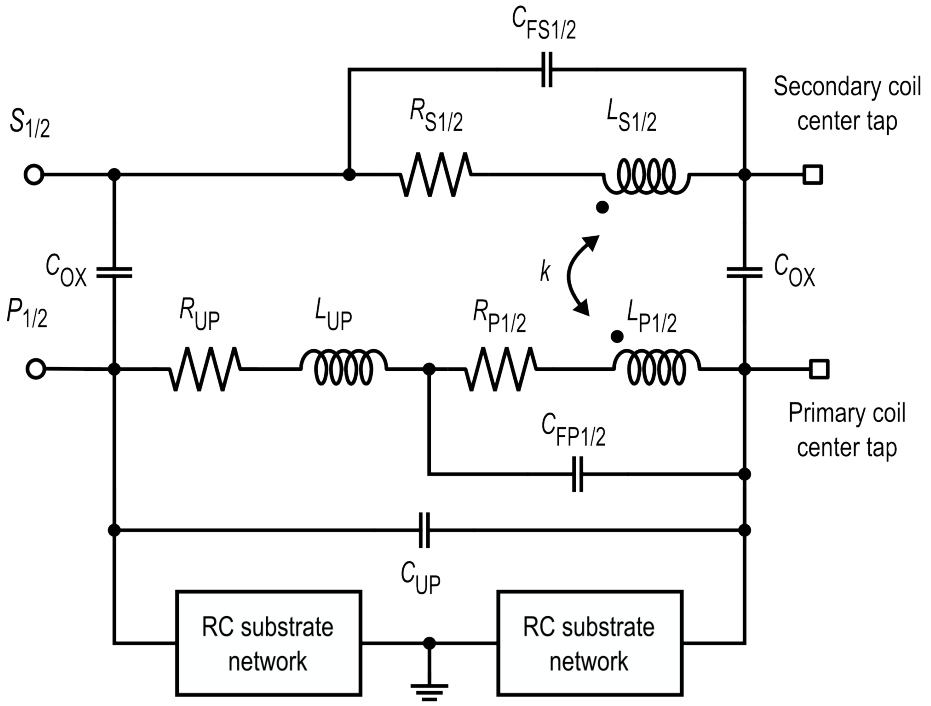


Figure 2.13. Schematic of the lumped geometrically scalable model of the isolation transformer T_{ISO} (half-structure).

for both reactive and resistive components to estimate the self-resonance frequency (SRF) and energy losses of the transformer, respectively, for a wide range of geometrical parameters. In particular, for the inductance values, $L_{P1,2}$ and $L_{S1,2}$, simple analytical expressions for integrated coils are not suited due to both large width and high area required by the transformer compared to typical RF inductors. A set of integrated inductors was implemented and simulated in ADS Momentum. It was found that the following monomial fitting expression introduced in [76] can provide enough accuracy in a wide range of geometrical parameters:

$$L = A \times n^b \times w^c \times D_{OUT}^d \times D_{AVG}^e \tag{2.14}$$

where n, w, D_{OUT} and D_{AVG} are the number of turns, the metal width, the outer diameter and the average diameter of each transformer winding, respectively, while coefficients A, b, c, d, and e are fitting parameters extracted from EM simulations.

It was used for both primary and secondary coil inductances. Model capacitances (i.e., the fringing contributions between each turn of the spiral, modeled by $C_{FP1,2}$ and $C_{FS1,2}$, the underpass capacitance, C_{UP}, and the isolation oxide capacitance, C_{OX}) were calculated with the simplified expression for parallel-plate capacitance, while a typical RC network was adopted to model the silicon substrate [69].

Series resistances $R_{P1,2}$ ($R_{S1,2}$) are the most important parameters of the model for an accurate estimation of transformer losses. Several expressions available in literature were tested and none of them provided the required accuracy. For this reason, a novel expression was exploited that is

$$R = R_{DC} \times \left(1 + \frac{\alpha \left(\frac{f}{f_{CRI}} \right)^2}{1 + \beta \left(\frac{f}{SRF} \right)^2} \right) \times \frac{t}{t_{EQ}} \tag{2.15}$$

Here R_{DC} is the dc resistance of the coil, α and β are fitting factors, f_{CRI} is the critical frequency as defined in [77], which takes into account the crowding effects with respect to the geometrical parameters of the coil, while t and t_{EQ} are the physical and the equivalent thickness of the metal layers, respectively, the latter being used to model the skin effect phenomena [78]. The equation is further improved by a correction term based on a rough estimate of the SRF of the coil, that is:

$$SRF \approx 1/2\pi\sqrt{LC} \tag{2.16}$$

where L can be the primary or the secondary inductance in Fig. 2.13 and C is the equivalent capacitance seen by this inductance. This term including the SRF was meant to account for the equivalent resistance reduction that takes place nearby the self resonance region [79].

The proposed model was properly customized for the adopted transformer configuration (see Fig. 2.2), which was chosen to minimize the length of the bonding wires between the oscillator and rectifier dice, simplify the routing towards the power supply and the LDMOS transistors and maximize the overlap between primary and secondary windings. To this aim, internal and external diameters were set equal for

primary and secondary coils and the number of turns was limited to an integer and half-integer number for secondary and primary coils, respectively. Metal spacing values (s_P for the primary and s_S for the secondary windings) were the minimum available by the process for metal 3 and metal 4, respectively. As a result, we have only three free design parameters for the transformer, i.e. primary coil outer diameter, D_{OUT_P}, width, w_P, and number of turns, n_P, being secondary coil parameters linked by the following constraints:

$$\begin{cases} D_{OUT\_S} &= D_{OUT\_P} = D_{OUT} \\ w_S &= \frac{2w_P-(2n_P-1)(w_P+s_P)-s_S(2n_S-1)}{(2n_S+1)} \\ n_S &= \lfloor G \times n_P + 0.5 \rfloor \\ G &= \frac{\pi}{2}\frac{V_{OUT}}{2V_{DD}} \end{cases} \tag{2.17}$$

Here the approximate relationship $V_{OUT}/V_{OUT\_AC} = 2/\pi$ was used to set the ideal turns ratio G, where V_{OUT_AC} is the voltage at the secondary coil of the transformer. This expression is true for an ideal full-bridge rectifier where the threshold voltage of the rectifier is neglible with respect to the peak input voltage, as it happens in this case where V_{OUT_AC} must be higher than 20 V. The coupling factor k for such power-transfer transformers is very high and almost constant (e.g., 0.9) thanks to the high overlap area between primary and secondary windings compared to the oxide thickness (i.e., about three order of magnitude larger). The soundness of the developed model is well demonstrated by comparison with respect to EM data of 30 geometrically scaled transformers (D_{OUT} from 650 μm to 1900 μm, n_P from 1.5 to 3.5, w_P from 60 μm to 300 μm.). The error distributions of main electrical parameters between model and sim. data is reported in Fig. 2.14. Maximum errors for inductance, Q-factor peak, SRF and k are mostly smaller than 10%, which confirms that the model can be used as a reliable tool within the proposed iterative co-design procedure.

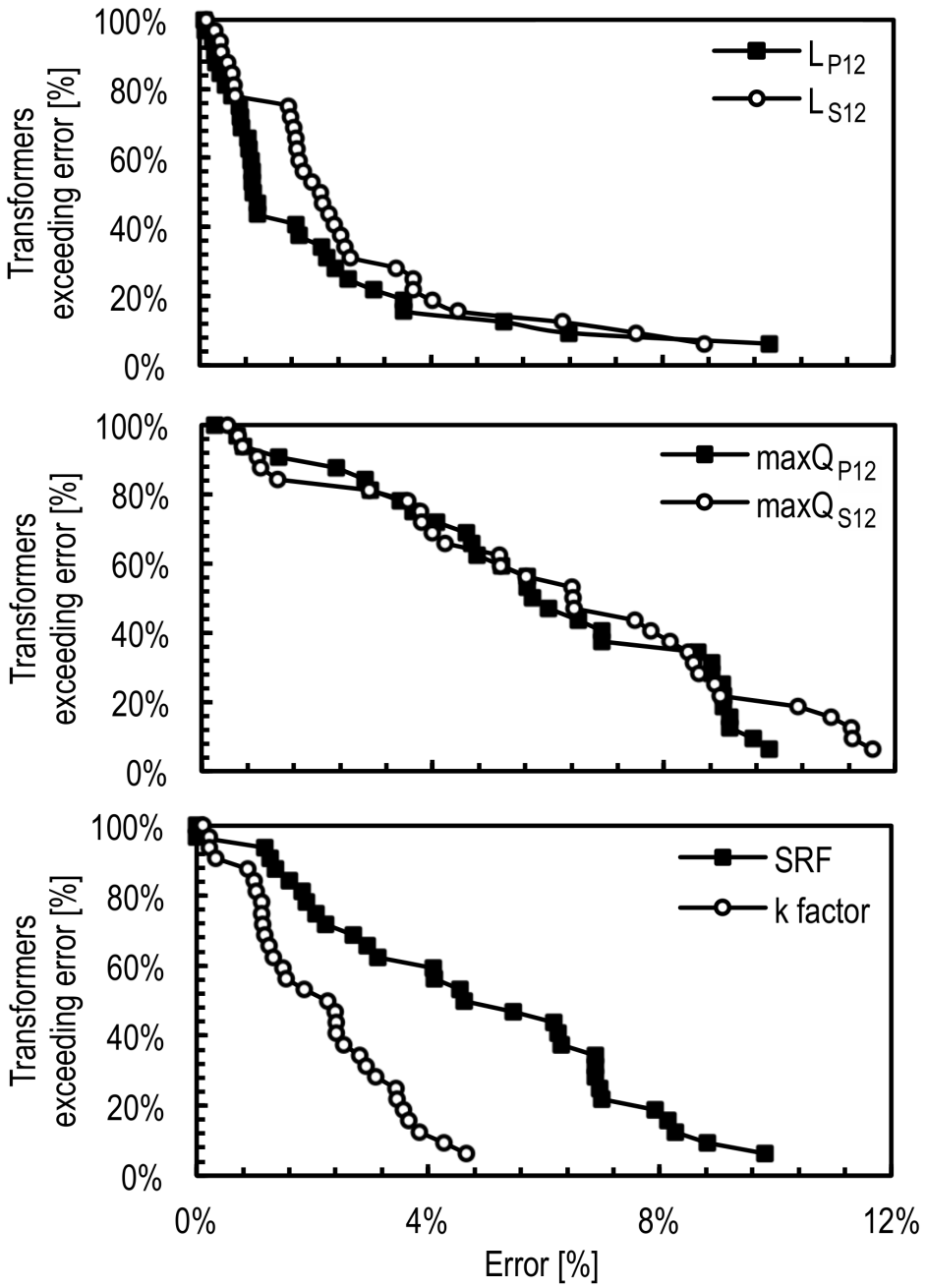


Figure 2.14. Error distributions of the geometrically scalable lumped model calculated with respect to EM simulations.

2.3.2 Co-design procedure and expected results

Firstly, we recall main design parameters of the system. The rectifier design parameter is its multiplicity, M, while only three geometrical parameters define the isolation transformer (i.e., D_{OUT}, n_P, and w_P) thanks to the constraints defined by Eq. 2.17. The design parameters of the oscillator core are the size of the power transistors, W_A, the size of the coupling capacitors C_B, and the biasing voltage V_B, which are linked to the peak drain voltage by the voltage $V_{GS,MAX}$. Since C_B scales with W_A, a basic oscillator cell can be defined which does not depend on the resonant tank. For a given V_B and W_A, this basic cell is defined by C_B. A trial value for C_B can be defined by using an ideal resonating tank: if C_B is chosen to avoid gate-oxide breakdown of the transistors with an ideal tank, this condition guarantees that, for an actual tank, gate-oxide breakdown is never reached, since the higher losses of a real tank reduce the peak drain voltage compared to the ideal tank, thus protecting also the gate-oxide. By sweeping V_B and adjusting C_B, it can be seen that an optimum value of V_B exist, which provides the best trade-off between dc losses and transconductance for oscillator start-up.

The proposed co-design procedure is represented in Fig. 2.15. The main design constraints, P_{OUT}, and the oscillator chip area, are used to set the rectifier multiplicity, M, and the transformer output diameter, D_{OUT}, in the first and second step, respectively. Indeed, M defines both $R_{RECT}//C_{RECT}$ and η_{RECT} and hence the required power at the transformer output, ${P_{OUT,AC}}^*$, while D_{OUT} mainly defines the area of the dc-ac converter. By using the transformer model, the geometrical design space can be explored by sweeping w_P for a given n_P. This guarantees that all the possible transformer implementations for the given area constraint are inspected.

In the third step, optimal design for the active core is obtained for each transformer. Indeed, multiple basic oscillator cells, say N as in the figure, can be connected to the oscillator tank to define the overall active-core size in a similar manner

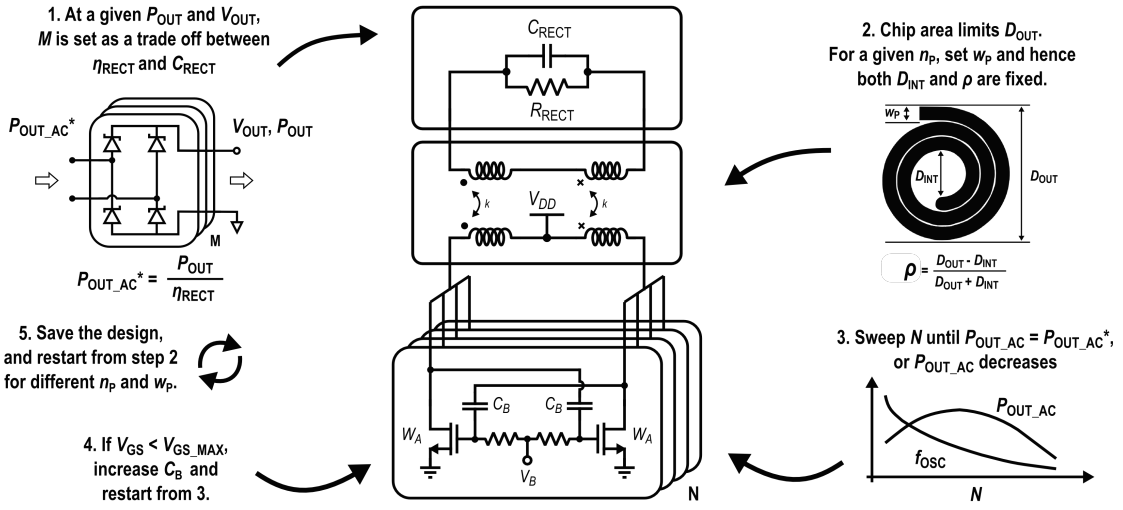


Figure 2.15. Graphic representation of the proposed co-design procedure.

as the number of diodes for the rectifier. From the oscillator point of view, a minimum N is required for the oscillation to take place. However, a viable design is found only if P_{OUT_AC} is approximately equal to $P_{OUT,AC}{}^*$. Indeed, the resonating tank formed by transformer and rectifier impedance is a good approximation for the actual resonating tank only if the required amount of output power is delivered to the rectifier, which corresponds to the power used for the extraction of Z_{RECT}, $P_{OUT,AC}{}^*$. Therefore if $P_{OUT,AC}{}^*$ is not achieved in these conditions, we must increase N above the minimum value, to increase the power delivered to the transformer. According to simulations in Fig. 2.8, the minimum N provides the condition of worst active-core efficiency for the given resonating tank in terms of L_{EQ} and R_{EQ} for a given W_A. If N and hence the overall W_A increase, the equivalent tank impedance seen by each basic cell of the active core increases, as shown in Fig. 2.16. With respect to Fig. 2.8, if we increase both L_{EQ} and R_{EQ} for a given W_A we move in the direction of maximizing the active core efficiency, and hence not only the power delivered to the transformer P_{TX} increases due to higher dc power, but also η_{CORE} increases due to better operating waveforms. On the other hand, from

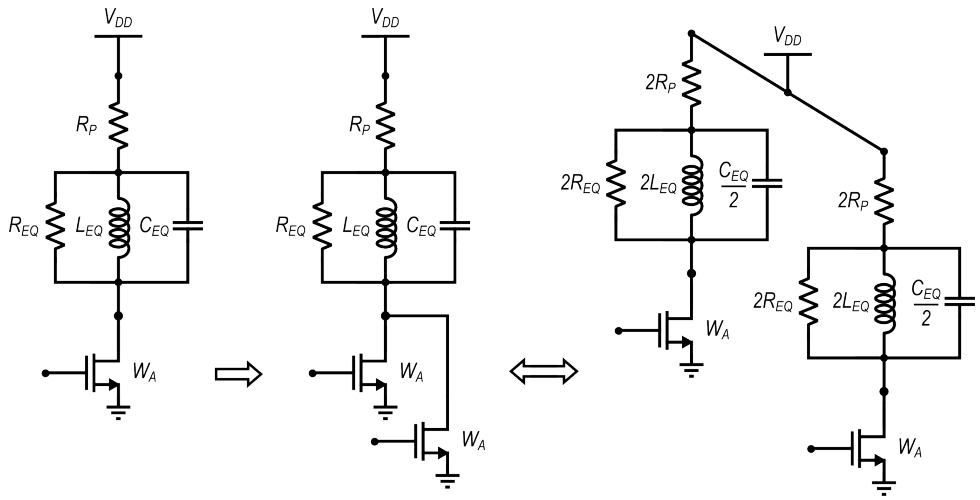


Figure 2.16. Equivalent tank impedance at the increasing of W_A.

a system perspective the parasitic capacitive contribution C_P from the active core increases, thus reducing the resonant frequency f_0 at the transformer input, which reduces f_{OSC}. Similarly a further reduction of f_{OSC} is obtained as a consequence of higher active core efficiency, as already demonstrated in Fig. 2.10. Therefore the output power of the transformer, P_{OUT_AC}, at first increases due to higher active core efficiency, and then at some point it changes its slope due to the reduction of η_{TX_AC} at lower f_{OSC} and starts decreasing. Of course, only the design which guarantees $P_{OUT,AC}{}^*$ with the actual transformer implementation is a good candidate for physical implementation, since other design would not match the input impedance of the rectifier.

This third step can be re-iterated also by adjusting the C_B/W_A ratio to optimize the transistor operating conditions while guaranteeing safe operation, as noted in step four. Once the best design is obtained for the selected transformer, a new one is investigated by restarting the design procedure from step two, to find the best efficiency performance within the allowed geometrical design space.

Typical results of the proposed co-design procedure are described by the charts in Fig. 2.17, which shows a design space search constrained by $P^*_{OUT\_AC} = 1.25\,\mathrm{W}$ and

$D_{OUT} = 1.33\,\text{mm}$. A basic cell width of $W_A = 330\,\mu\text{m}$ was used, with $V_B = 1.1\,\text{V}$,

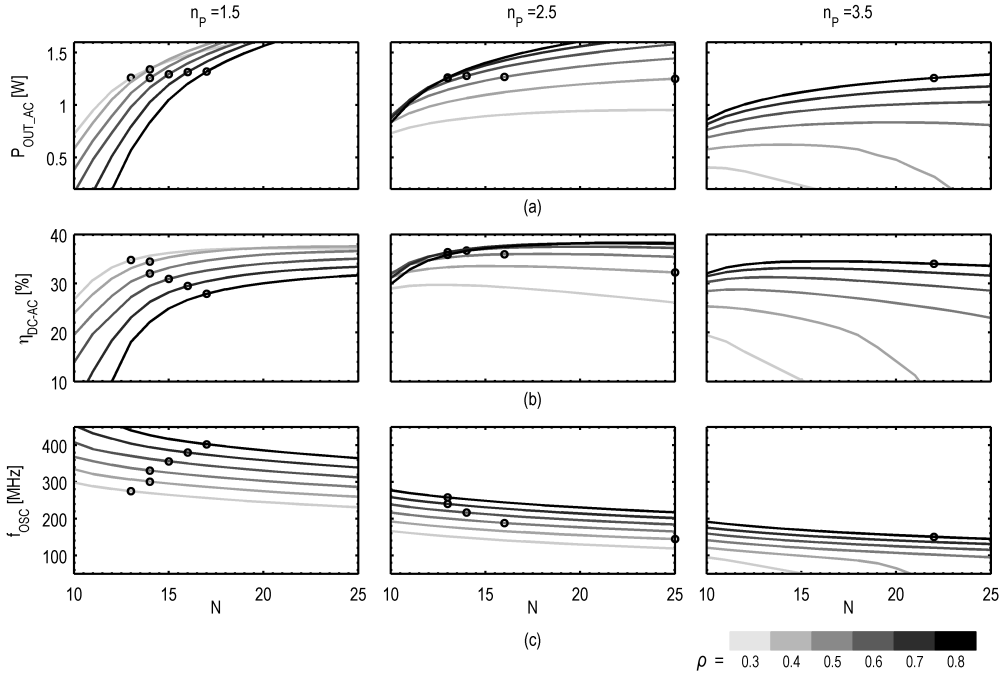


Figure 2.17. Typical results of the co-design procedure in Fig. 2.15 : (a) output ac power, P_{OUT_AC}, (b) dc-ac efficiency, η_{DC-AC}, (c) oscillator frequency, f_{OSC}.

while C_B/W_A is kept fixed at $3\,\text{pF/mm}$ here to better highlight the role of the sole transformer design parameters. Figs. 2.17(a) to (c) show P_{OUT_AC}, η_{DC-AC}, and f_{OSC}, respectively, for three increasing n_P. These charts show six curves, each one corresponding to a different transformer implementation with different fill-factor, ρ, which is the geometrical parameter better related to the ac spiral losses [80]. The curves are drawn as a function of the multiplicity N, while possible design solutions (i.e., the ones that reach P_{OUT_AC}*) are highlighted by markers in Fig. 2.15 and also listed in Table. 2.2 for the sake of clarity.

Displayed results well demonstrate the inherent design complexity due to the integrated implementation of the transformer. The required output power is obtained for all the investigated n_P. Although most valid solutions are achieved for $n_P = 1.5$, primary coils inductances L_P are quite low in this case. Moreover, due

Table 2.2. Summary of optimized designs from Fig. 2.17

n_P	ρ	w_P [μm]	L_P [nH]	N	P_{OUT_AC} [W]	$\eta_{DC\text{-}AC}$ [%]	f_{OSC} [MHz]
1.5	0.3	154	3.2	13	1.26	34.8	275
	0.4	190	2.7	14	1.34	34.5	301
	0.5	222	2.3	14	1.26	32.1	331
	0.6	250	2.0	15	1.30	30.9	356
	0.7	275	1.7	16	1.32	29.5	380
	0.8	296	1.5	17	1.32	27.9	403
2.5	0.4	127	6.9	25	1.25	32.2	144
	0.5	**148**	**5.8**	**16**	**1.27**	**36.0**	**194**
	0.6	**166**	**5.0**	**14**	**1.28**	**36.7**	**217**
	0.7	**183**	**4.3**	**13**	**1.26**	**36.4**	**240**
	0.8	197	3.8	13	1.26	35.9	258
3.5	0.8	148	7.1	22	1.26	34.0	151

to the area constrained design procedure, the use of larger w_P to reduce the series losses degrades ρ, while further decreasing L_P, which also reduces power efficiency of both transformer and active core. Therefore, for $n_P = 1.5$ maximum η_{DC-AC}, is lower than 35%. On the other hand, for $n_P = 3.5$ only one solution is found, mainly due to the higher dc losses of primary coils. This is related to a very high ρ value and achieves an η_{DC-AC} of 34%. Most promising solutions are instead obtained with $n_P = 2.5$. An optimum range of w_P and hence ρ (i.e., $0.5 < \rho < 0.7$) is found, which maximizes efficiency with values better than 36%. This is the result of the best trade off between dc and ac series losses of primary windings as well as active core operation. Starting from these solutions, the design flow was iterated by increasing the sampling points closer to the optimal points and adjusting the C_B/W_A ratio, as described in Fig. 2.15. For each design cycle the best solutions were further checked with EM simulations. Finally, the design was completed by including the rectifier and parasitics due to bonding wires and both ground and power supply

plane. The design parameters of the proposed system are summarized in Table. 2.3, while Table. 2.4 shows main expected results. The final efficiency of each block can be estimated as follows, according to simulations:

- $\eta_{RECT} = 84.1\%$
- $\eta_{TX} = 48.2\%$, with $\eta_{TX\_AC} = 57.3\%$
- $\eta_{CORE} = 75.5\%$

It is apparent that the transformer is the weakest block of the chain.

Table 2.3. Design parameters for the proposed converter.

Block	Parameter	Value	Unit
Oscillator Core (N=16)	W_A	5.28	[mm]
	C_B	16.6	[pF]
	V_B	1.1	[V]
Isolation Transformer	w_P	146	[µm]
	D_{OUT}	1330	[µm]
	n_P	2.5	turns
	L_P; L_S	6; 52 @ f_{OSC}	[nH]
	Q_P; Q_S	2.6; 7 @ f_{OSC}	
	k	0.884	
Rectifier	M	40	diodes

2.3.3 Micrographs

The micrographs of the fabricated power oscillator and the full-bridge diode rectifier are shown in Fig. 2.18 and Fig. 2.19, respectively. The oscillator die size is 3.3 mm ×

Table 2.4. Expected performance.

Converters	Output power	Power efficiency	Oscillation frequency
dc–ac $R_{RECT} = 220\ \Omega$ $C_{RECT} = 3.6$ pF	1.12 W	35.5%	198 MHz
dc–dc $V_{OUT} = 20$ V	0.93 W	30.6%	194 MHz

2.6 mm, mainly due to the isolation transformer. The LDMOS active core is placed at the bottom of the die a with the ground plane while a large metal plane is used to provide the power supply connection to the primary coil center tap. Off chip parasitics were minimized by using multiple bonding wires for both V_{DD} and ground.

The rectifier has an actual size of $950\,\mu$m $\times$ $725\,\mu$m. The overall silicon area of the two dice is about 9.3 mm^2.

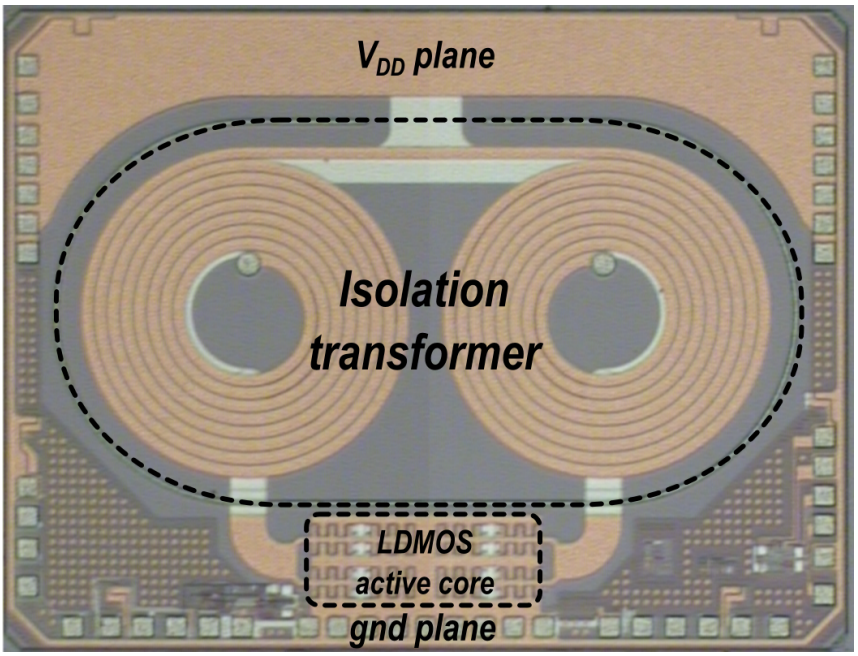


Figure 2.18. Micrograph of the power oscillator die.

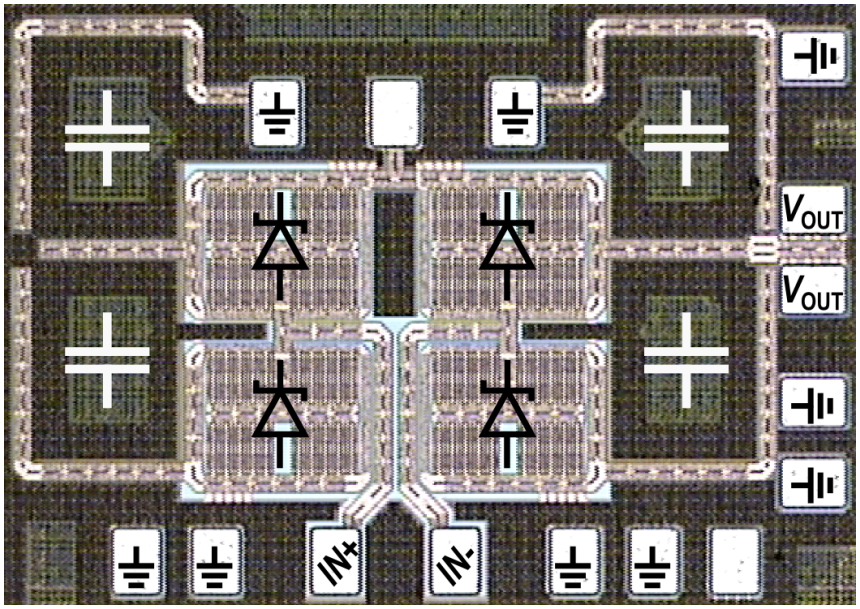


Figure 2.19. Micrograph of the power rectifier.

2.4 Measurement results

This section reports measured results for the proposed systems. Experimental characterization was carried out in two phases.

First, the complete system was assembled on the evaluation board, as shown in Fig. 2.20. Here two bonding wires directly connect the secondary coil of the

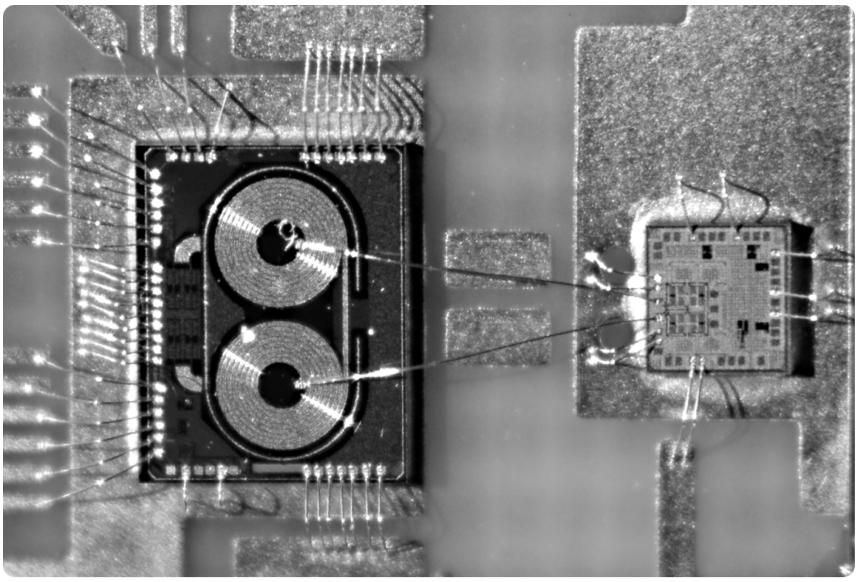


Figure 2.20. Micrograph of the overall dc-dc converter assembled on board.

transformer to the rectifier input pads. The dc-dc characterization was performed with two different versions of the adopted technology process: a second version of the power oscillator was made available, which differs from the standard one for the thickness of the primary coils metallization. Specifically, in the thick-coils version metal layers from metal 1 to metal 3 where increased by 50 % to evaluate the impact of its resistivity on the performance of the converter. The converter was characterized at several dc output voltage, V_{OUT}, by means of a semiconductor parameter analyzer, for supply voltages of $5\,\mathrm{V} \pm 5\,\%$. It was also tested at different output power levels by using on-chip on-off power control and with different measurement time to highlight the effects of self-heating. At least four samples were

tested for each measurement, and reported data are averaged values, if not specified. However, a consistent reduction of the output power was observed when compared measured results with expected values for the standard technology, independently of the operating temperature of the system.

Afterwards, due to the high complexity of the system including two non-linear blocks such as the rectifier and the oscillator, a second extensive characterization was necessary to better understand the reason of the reduced performance. However, it was not possible to characterize the performance of the power rectifier due to the lack of instrumentation. Therefore, the performance of the oscillator and the integrated transformer were evaluated. Specifically, on-wafer characterization of transformer parameters were carried out for the test-structures shown in Fig. 2.21, by means of a Cascade Microtech probe station and an HP8155 network analyzer. Finally, the

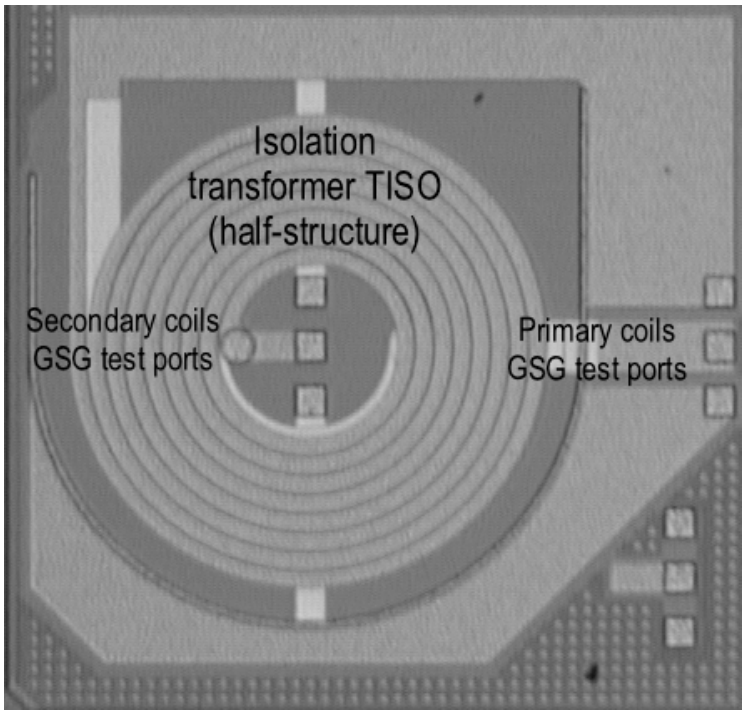


Figure 2.21. Micrograph of the test-chip with highlighted the isolation transformer T_{ISO} (half-structure).

performance of the dc-ac converter was carried out by mounting the power oscillator die on a test board along with a passive discrete network as equivalent output load (i.e., a resistance R_L in parallel to a capacitance C_L), as shown in Fig. 2.22. The

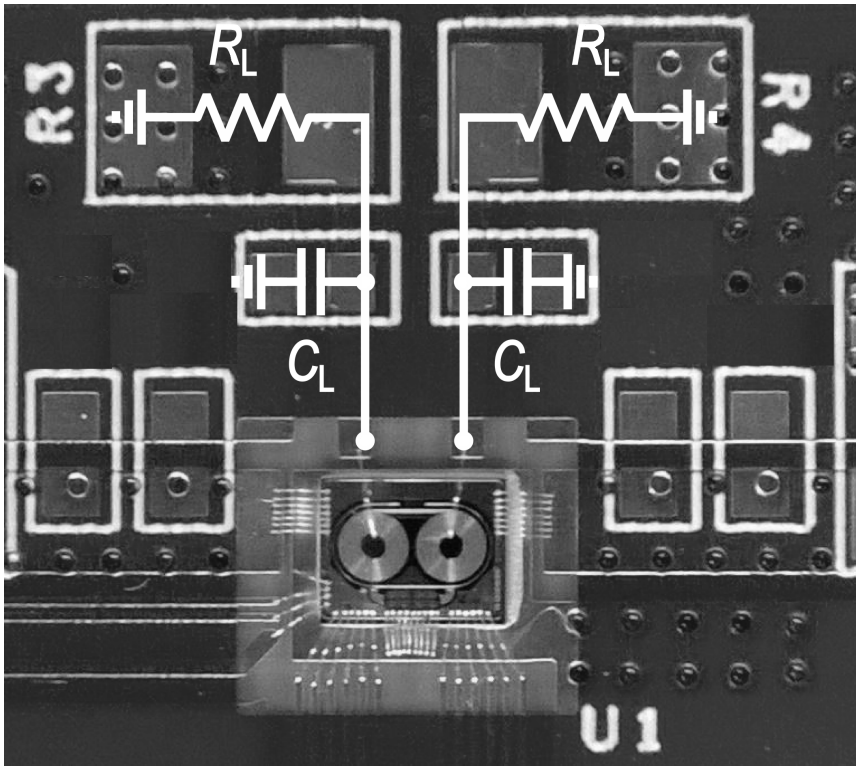


Figure 2.22. Micrograph of the dc-ac converter assembled on board.

output voltage, V_{OUT_AC}, at the secondary winding of the isolation transformer was captured by means of a high impedance active probing system. Both dc-ac and transformer measurements were carried out only for the standard metal version of the oscillator chip. As a result it was possible to attribute the measured discrepancies to the available LDMOS model, as discussed in the following.

2.4.1 DC-DC converter

Fig. 2.23 shows dc output power, P_{OUT}, and power efficiency, η, as a function of the output dc voltage, V_{OUT}, for both standard and thicker metal back end. Efficiency increases with V_{OUT}, thanks to a better performance of both the LDMOS and the rectifier at higher oscillating voltages. With standard metallization P_{OUT} and η are around 780 mW and 27.6 %, respectively, in nominal conditions, (i.e., $V_{OUT} = 20$ V). The exploitation of thicker primary coil allows both P_{OUT} and η to be improved by about 200 mW and almost two percentage points, respectively, approaching outstanding values of 980 mW and 29.6 % in nominal conditions.

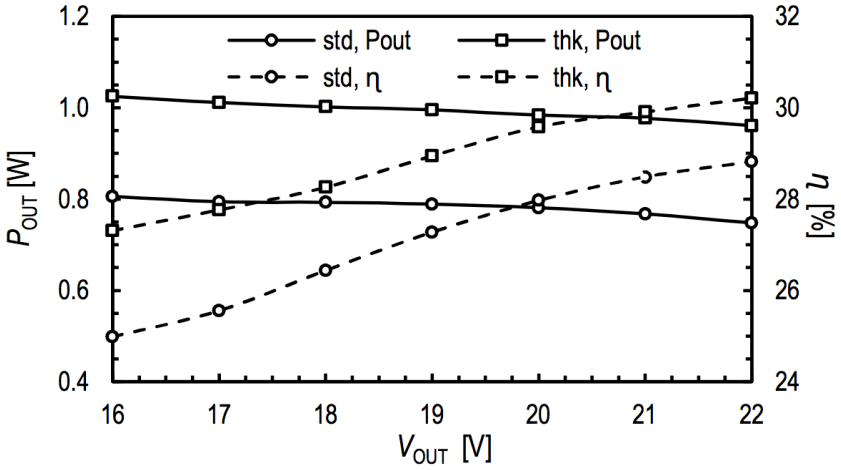


Figure 2.23. Output power, P_{OUT}, and power efficiency, η, as a function of the output voltage V_{OUT}.

Fig. 2.24 shows P_{OUT} and η as a function of time for both standard and thicker back-end. These measurements were used to evaluate the degradation of dc-dc performance due to thermal effects. It can be seen that for both versions performance reach the steady state after around 100 s, with a loss in terms of both power and efficiency of around 10%.

Measurements in Fig. 2.25 confirm that the power efficiency is quite constant with respect to the output power when the available on-chip turn-off circuitry is used for

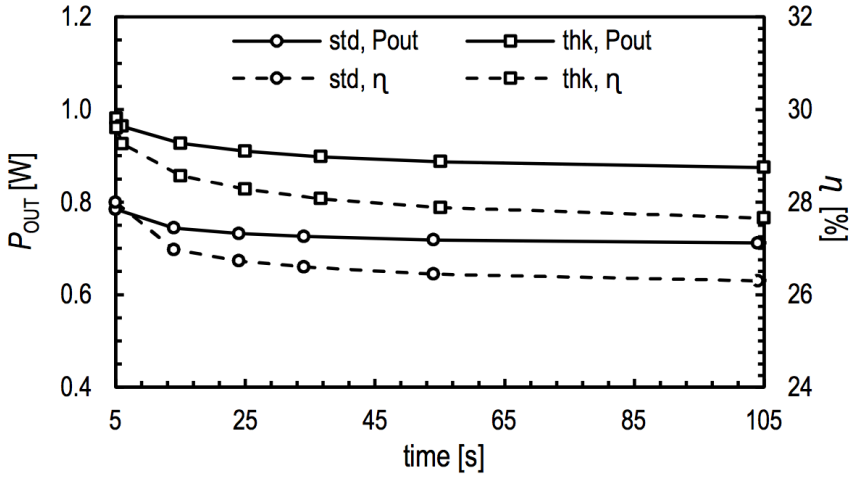


Figure 2.24. Output power, P_{OUT}, and power efficiency, η, as a function of the measurement time.

power control. A PWM modulation with fixed switching frequency of 200 kHz and variable duty-cycle was here used to modulate the averaged output power of the converter. Both pulsed (i.e., measurement time of 5 s) and continuous (measurement time 100 s) curves are reported to better highlight the thermal effects, which, of course, are more important when the output power is higher. Measurements confirmed that at $V_{OUT} = 20$ V the proposed system is still able to deliver a dc output power of 710 mW and 880 mW with an efficiency of around 26 % and 27.8 % for the standard and the thicker metal back-end, respectively.

Finally, the sensitivity of the converter with standard metallization was evaluated with respect to both biasing and supply voltage for one sample. Fig. 2.26 shows that peak power is almost constant with the biasing voltage, V_B. Efficiency however decreases for higher V_B due to higher dc losses. Actually, it must be pointed out that, once started, the oscillator is able to sustain the oscillation voltage even for $V_B = 0$ V with increased efficiency due to reduced dc losses. This fact could be exploited to further increase the performance of the system. However, for V_B lower than 1.1 V the start-up time increases: in Fig. 2.26 this can be noticed since for $V_B = 0.7$ V and $V_B = 0.9$ V only nine measurement points are available, which

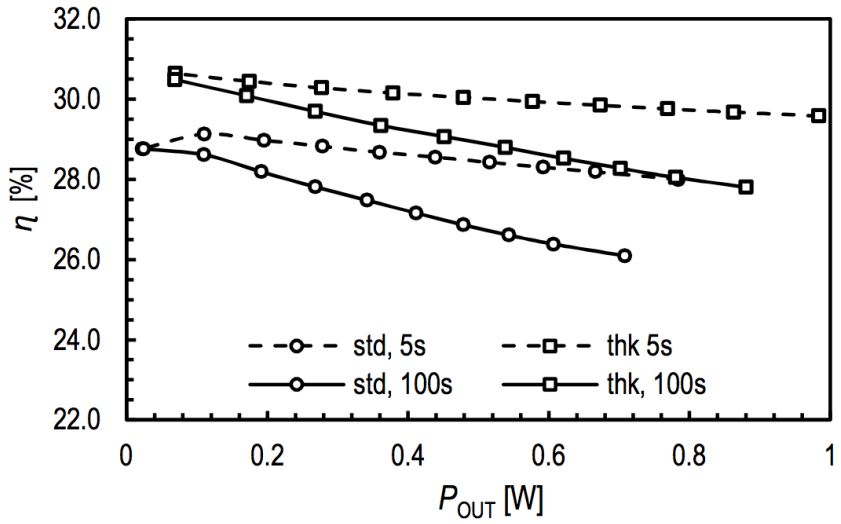


Figure 2.25. Power efficiency, η, versus output power, P_{OUT}, ($V_{OUT} = 20\,\mathrm{V}$).

means that the oscillator is not able to start within the lower PWM duty-cycle on-time, i.e. $10\% \times T_{PWM}$. This suggests that a start-up circuit could be required to guarantee operation with higher temperatures or if lower V_B are to be exploited to increase efficiency. Besides, this confirms that the design value of $V_B = 1.1\,\mathrm{V}$ is the optimum value for robust operation at room temperature.

Fig. 2.27 on the other hand shows the great sensitivity of both output power and power efficiency with respect to the supply voltage, as a consequence of the voltage-controlled operation of the class-D oscillator. As expected, for lower V_{DD} the output power reduces almost quadratically, whereas power efficiency increases: indeed, if the oscillation voltage is strong enough to drive the transistors in saturation, their on resistance $R_{1,2}$ is roughly the same as the one with higher V_{DD}, and hence the efficiency benefits of the lower resistive losses due to reduced drain current. Similarly, for higher V_{DD} the efficiency reduction can be attributed to increased dc losses: indeed, for a small increase of input power and voltage levels the rectifier efficiency do not change a lot and can be well compensated by the higher efficiency of the transformer for lower load impedance, whereas higher peak currents in both

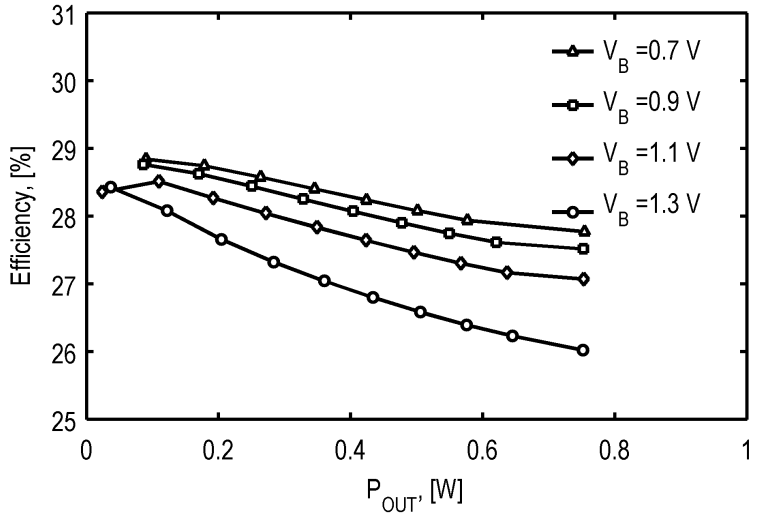


Figure 2.26. Power efficiency, η, versus output power, P_{OUT}, for different biasing voltages V_B ($V_{OUT} = 20\,\mathrm{V}$).

transistors and primary coils dc resistances reduce efficiency.

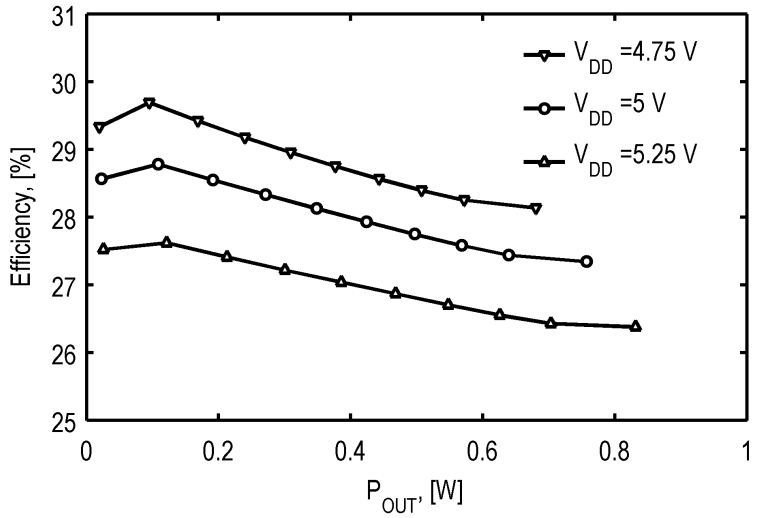


Figure 2.27. Power efficiency, η, versus output power, P_{OUT}, for different supply voltages V_{DD} ($V_{OUT} = 20\,\mathrm{V}$).

2.4.2 Isolation transformer

Five samples of the isolation transformer were characterized from different wafers. Characterization was performed both in frequency and in temperature showing negligible variation between samples of the available lot. Fig. 2.28 shows a comparison between measured and simulated EM data for the test structure. The series inductance $L_{P1,2}$ ($L_{S1,2}$), series resistance $R_{P1,2}$ ($R_{S1,2}$), and quality factor $Q_{P1,2}$ ($Q_{S1,2}$) are reported for primary (and secondary) coil. Discrepancy between EM simula-

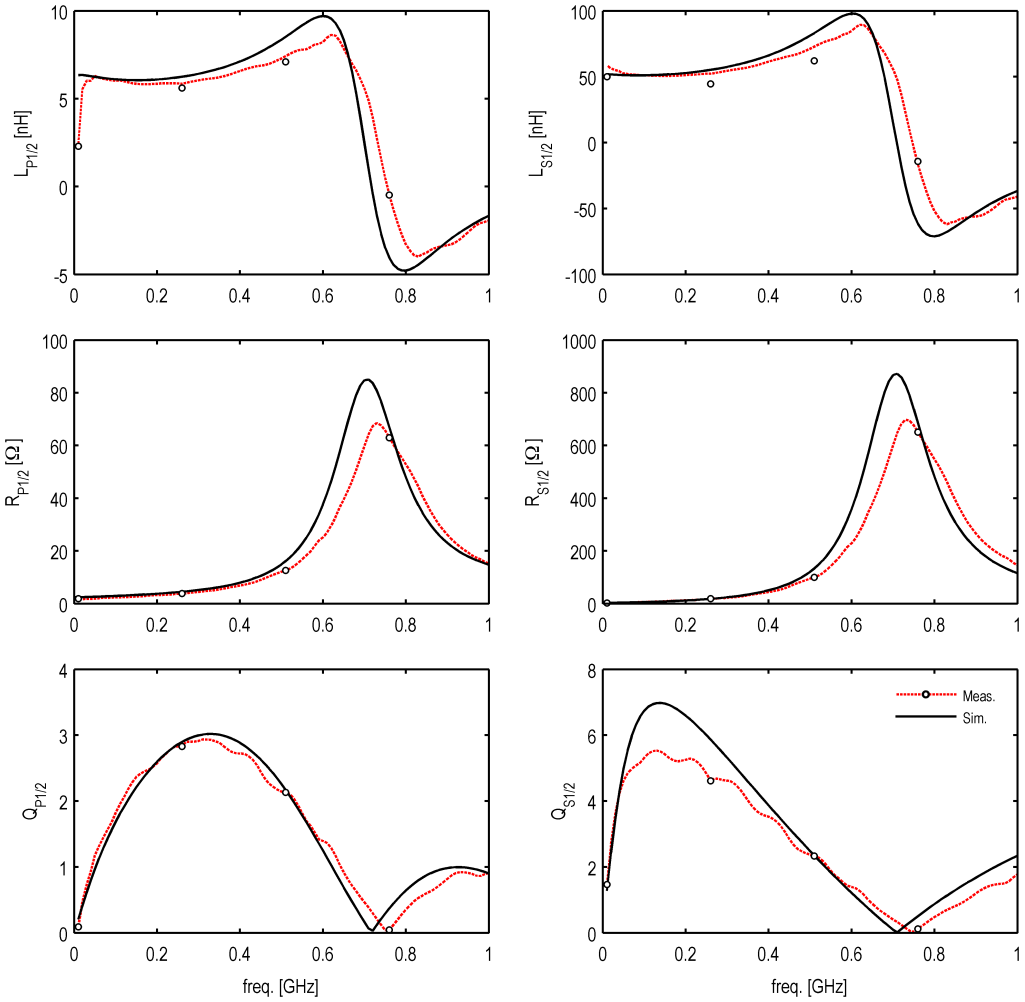


Figure 2.28. Narrowband parameters of the isolation transformer - measurements vs. simulation.

tions and measurements for the inductances and resistances and, especially, for the peak of the secondary coil's quality factor, $Q_{S1/2}$, can be attributed to the lack of proper series de-embedding structures, which were not integrated due to integration area constraints. Wide-band measurements in Fig. 2.29 confirm the correctness of measurement setup.

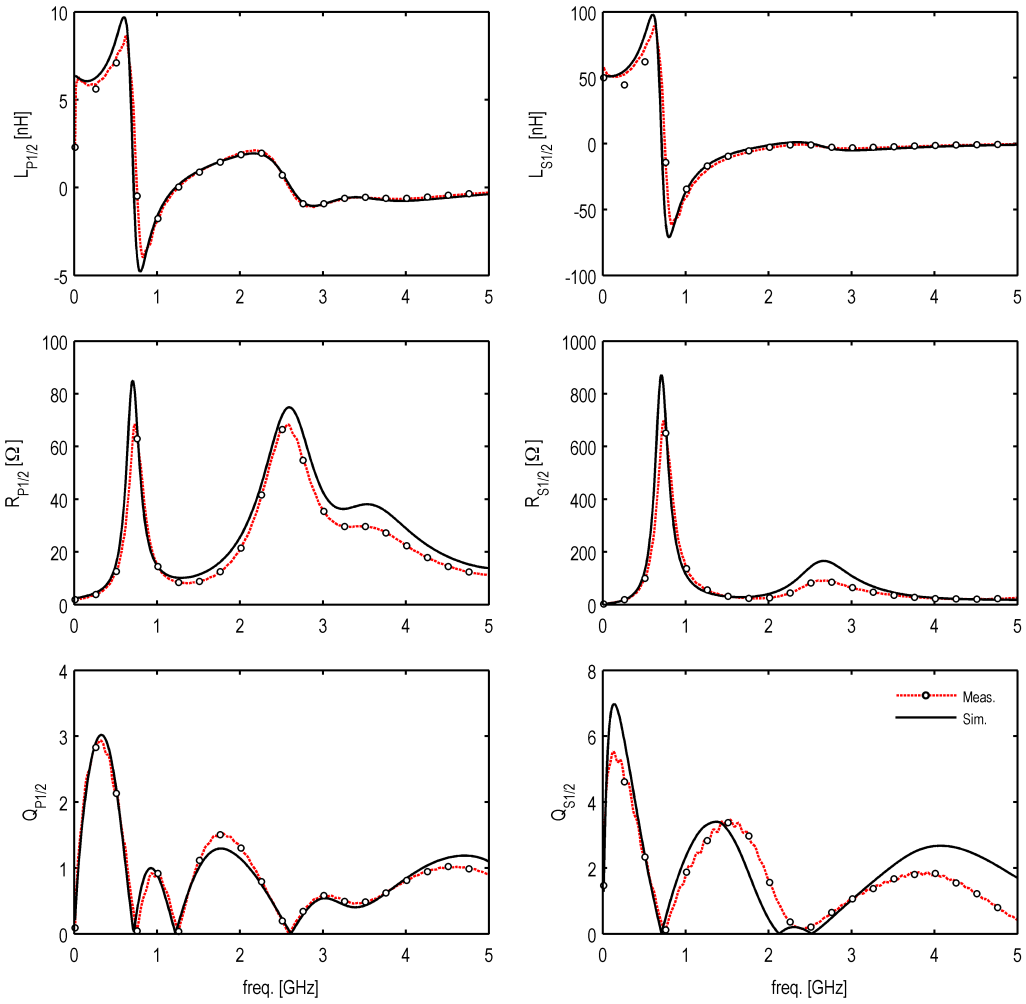


Figure 2.29. Wideband parameters of the isolation transformer - measurements vs. simulation.

Based on these measurements, it can be concluded that the evaluation of transformer parameters was done correctly at the design time. Similar conclusions then

hold for the evaluation of on-chip parasitics, which were evaluated adopting the same EM simulation setup.

2.4.3 DC-AC converter

In the following, measurements of the dc-ac converters are reported as a function of the external lumped load, $R_L//C_L$.

Measurements vs. R_L without C_L.

Figs. 2.30 to 2.32 shows output power, P_{OUT_AC}, power efficiency, η_{DC-AC}, and oscillation frequency, f_{OSC}, respectively, measured at the secondary winding of the isolation transformer as a function of load resistance, R_L, and without load capacitance, C_L. Markers show the cumulative measured points, whereas the trace is a least-square fitting of data.

In this configuration the oscillating frequency is mainly defined by parasitic capacitance at the primary coils, that is much higher than the parasitic capacitance that loads the secondary coil. Accordingly, Fig. 2.32 shows that the oscillating frequency has a weak dependence on the load resistance, which increase the oscillation voltage and hence reduces the averaged non-linear capacitance at the transistor's drain. P_{OUT_AC} is almost constant between 190 Ω and 300 Ω, while the efficiency increases linearly in the same range, reaching a peak of around 30.5 %. According to simulations the increasing of R_L reduces transformer efficiency. Therefore, the increasing of efficiency with R_L observed in this this region is mainly due to increasing active core efficiency, which compensates for the increasing transformer losses. After the peak both output power and power efficiency decrease, according to the increased tank impedance and the reduction of transformer efficiency.

Fig. 2.33 show the measured voltage waveforms at the output coils for three different load resistances. The x-axis is normalized with respect to the oscillation

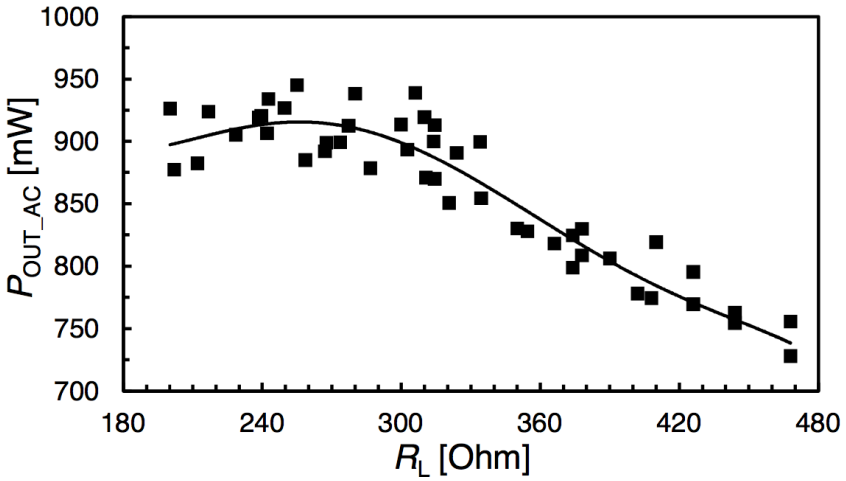


Figure 2.30. Output power measured at the transformer secondary winding as a function of load resistance R_L without external C_L.

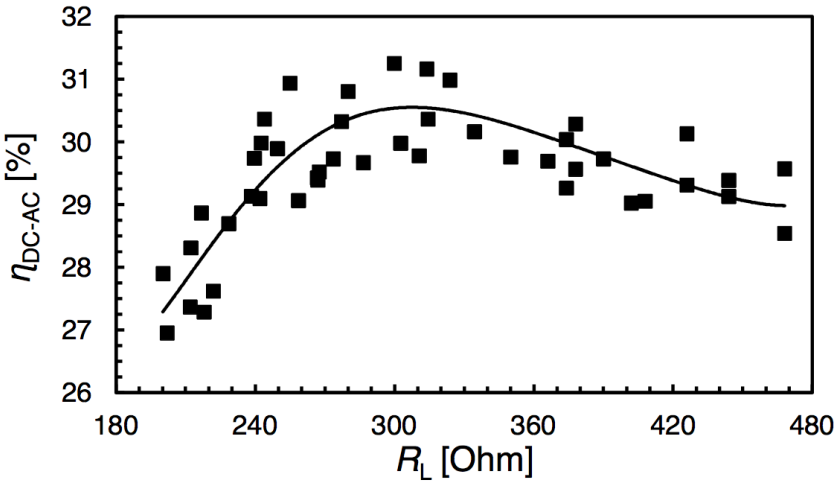


Figure 2.31. Power efficiency measured at the transformer secondary winding as a function of load resistance R_L without external C_L.

period. The peak of the waveform as well as its frequency increase with R_L.

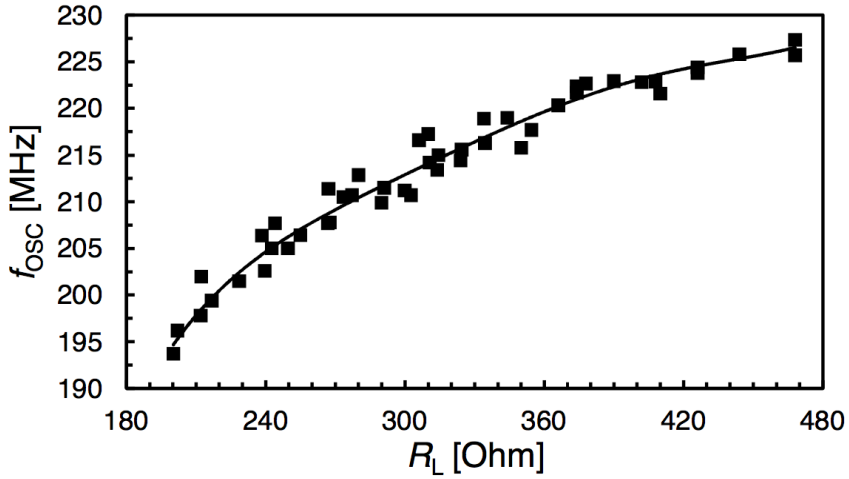


Figure 2.32. Oscillation frequency measured at the transformer secondary winding as a function of load resistance R_L without external C_L.

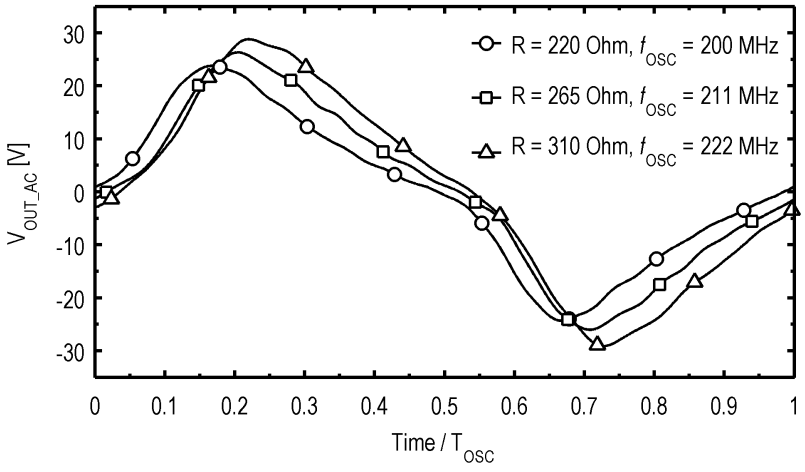


Figure 2.33. Output voltage measured at the transformer secondary winding for three values of load resistance R_L without C_L added.

Measurements vs. $R_L//C_L$

When the load capacitance is added both efficiency and output power increase as a consequence of the fact that the output resonance at the secondary coils, f_{RF2}, moves to lower frequency. Figs. 2.34 to 2.36 show output power, P_{OUT_AC}, power efficiency, η_{DC-AC}, and oscillation frequency, f_{OSC}, respectively, measured as a function of load capacitance, C_L, for three load resistances R_L relatively close to the simulated rectifier efficiency. Both P_{OUT_AC} and η_{DC-AC} are improved by C_L, showing a peak of 1064 mW and 35%, respectively, at $C_L = 5\,\text{pF}$ for $R_L = 310\,\Omega$. As expected from the analysis in section 2.2, the system exhibits high robustness with respect to C_L with more than 30% efficiency in a range of $\pm 2\,\text{pF}$ around the optimum C_L: the equivalent capacitance due to C_L becomes dominant and changes the operating frequency of the oscillator. However, for load networks similar to the simulated input impedance of the rectifier a reduction of both output power and efficiency can be noticed. It is about 6.5% and four percentage points, respectively, when compared to expected values of Table. 2.4, i.e. $P_{OUT\_AC} = 1120$ mW and $\eta_{DC-AC} = 35.5\%$ for $R_L = 220\,\Omega$ and $C_L = 3.6\,\text{pF}$.

By comparing the oscillation frequency with and without external C_L it can be concluded that the estimate of rectifier input capacitance is accurate, however a discrepancy is noticed: compared to simulations, a 15.5% reduction of f_{OSC} is measured, which therefore can be only attributed to an inaccurate estimation of LDMOS active core capacitive contributions. Indeed, the evaluation of these effects is a well known problem that requires large signal RF characterization and modeling, which were not available at the time of design [81].

Finally, Fig. 2.37 shows measured waveforms for $R_L = 220\Omega$ and different C_L, showing how the shape of these waveforms and hence operating class of the active core do not change considerably for small changes in C_L.

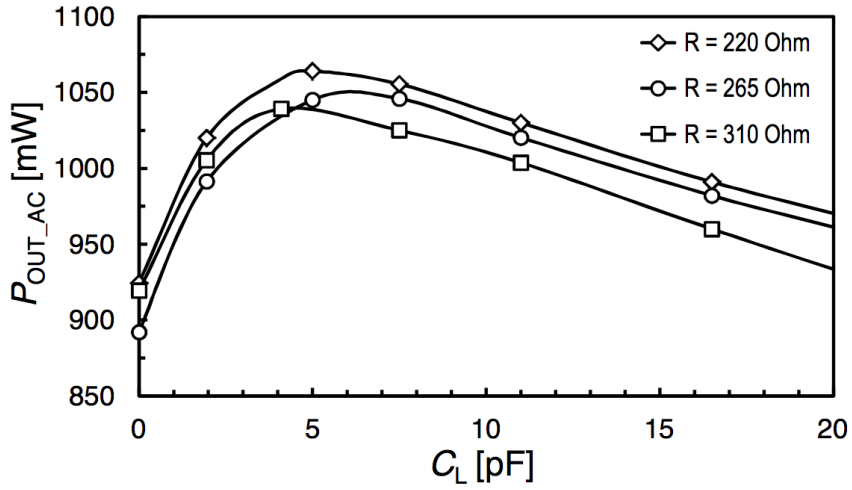


Figure 2.34. Output power measured at the transformer secondary winding as a function of load capacitance C_L for different R_L.

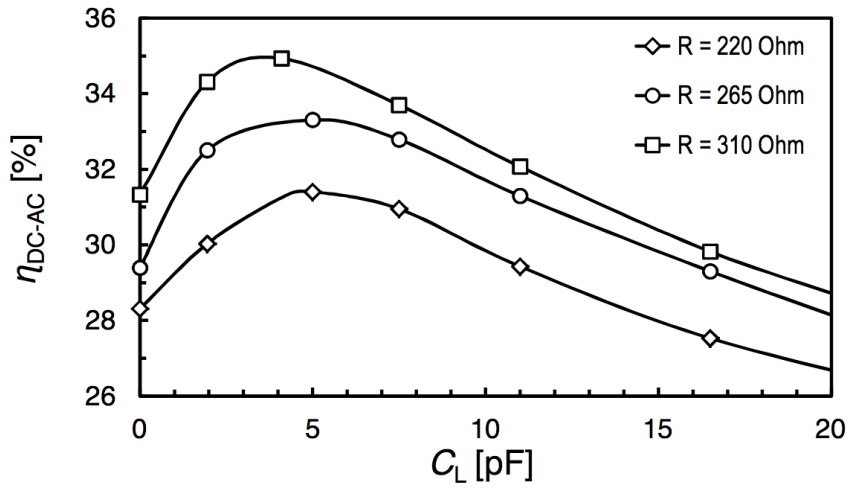


Figure 2.35. Power efficiency measured at the transformer secondary winding as a function of load capacitance C_L for different R_L.

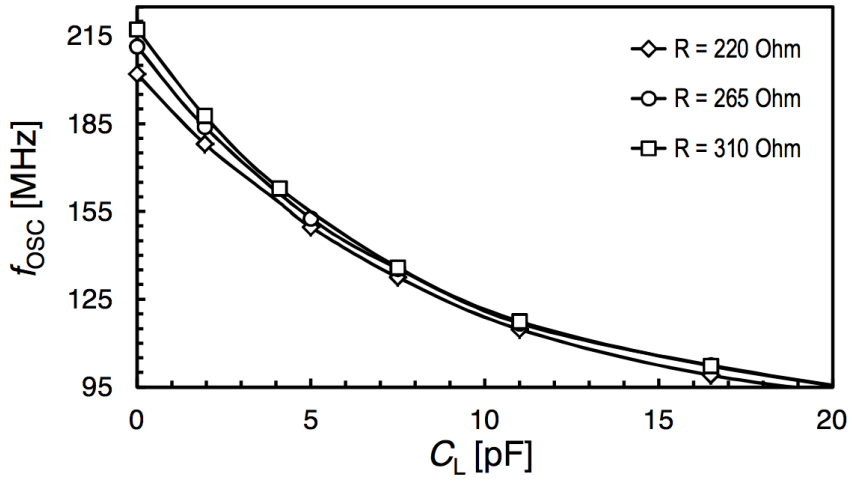


Figure 2.36. Oscillation frequency measured at the transformer secondary winding as a function of load capacitance C_L for different R_L.

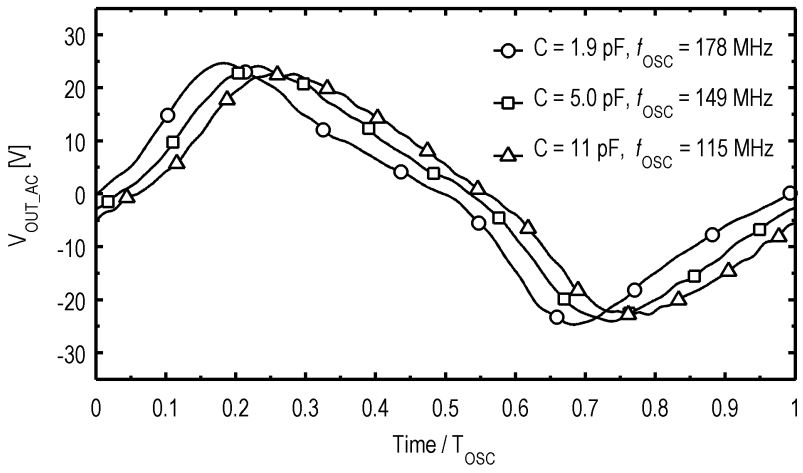


Figure 2.37. Output voltage measured at the transformer secondary winding for three values of load capacitance C_L ($R_L = 220\,\Omega$).

2.5 Comparison with the state-of-the-art

Thanks to the proposed design procedure, this work advances the state of the art of fully integrated, inductive, step-up converters for both peak power and power density, even without the improved metal back-end or with thermal effects included. For the sake of clarity, a comparison with most representative works is carried out in Table. 2.5. Both pulsed and steady-state measurements are shown. Specifically, the

Table 2.5. Comparison with state-of-the-art integrated step-up converters.

Ref.	Savio, ISCAS03	Richelli, JSSC04	Wens, ESSCIRC07	Chen, PESC08	This Work (Standard metals)	This Work (Improved metals)
Topology	Fly–back	Boost	Boost	Resonant	Resonant	Resonant
Operating frequency	1.4 GHz	120 MHz	100 MHz	160 MHz	165 MHz	168 MHz
Voltage Gain	4.44	3.75	1.83	3	4	4
Maximum Power	**6.4 mW**	**3.6 mW**	**150 mW**	**275 mW**	**710 / 780 mW**	**880 / 980 mW**
Efficiency	**19%**	**28%**	**63%**	**25%**	**26 / 28%**	**27.8 / 29.6%**
Power Density	**50 mW/mm^2**	**2.1 mW/mm^2**	**67 mW/mm^2**	**-**	**76 / 83 mW/mm^2**	**94 / 105 mW/mm^2**
Galvanic Isolation	**no**	**no**	**no**	**5 kV**	**5 kV**	**5 kV**
V_{OUT}	8	6	3.3	15	20	20
Technology	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS[a]	0.6-µm HV-CMOS, Schottky[b]	0.35-µm BCD, Schottky	0.35-µm BCD, Schottky
Area	0.127 mm^2	1.69 mm^2	2.25 mm^2	-	9.3 mm^2	9.3 mm^2

[a]Bond–wire inductor. [b]Post–processed micro–transformer, thick Au metals, thick gate oxide.

works from Savio, Richelli, and Wens, i.e. Refs. [82], [83], and [84], respectively, are the sole examples of CMOS based fully integrated inductive step-up converters, while the work of Chen, Ref. [57], is the sole example of SiP integrated step-up converter providing also galvanic isolation. The work of Wens achieves the highest efficiency by using bonding wire inductance, but the power density is lower compared to this work

and the integration approach is not compatible with galvanic isolation. The work of Chen achieves galvanic isolation, but relies on a post-processed back-end with very thick Au metals. Although the power density is not reported, his implementation uses three dice to implement the power transfer and hence its integration level is lower when compared to this work. Besides its output power is more than three times lower in spite of the high-quality BEOL.

Chapter 3

A 40 Mbps/23 mW data/power transfer system

One of key outcome of the state of the art presented in Chap. 1 is that an integrated isolator providing both data and power transfer could extremely useful in wide range of applications. Being isolated sensor interfaces the main target of such a system, two of its principal parameters are the bit rate from the isolated side, i.e. the downstream data link, and the available isolated supply current, I_{OUT}. Data rate in the range of tens to hundreds of Megabit per second are required to guarantee sufficient bandwidth and/or oversampling ratio for the sensor. Even if low frequency signals must be measured this high bandwidth can prove useful when cyclic redundancy check (CRC) codes and data communication protocols are taken into account, or when high signal-to-noise ratio (SNR) is demanded for a $\Sigma\Delta$ modulator, for example. Further to the output current, the cascaded sensor can benefit from scaled technologies to improve speed and costs. This means that a relatively low output voltage is not a problem, whereas the absolute value of available output current plays a key role, being the current consumption directly related to speed and noise performance of mixed-signal circuitry. Power efficiency is not a main concern for

these systems due to the low level of output power involved [28]. An additional useful feature demanded to the system is the availability of a slower upstream link, i.e. from the primary side to the isolated side, therefore implementing bidirectional communication. Such a link can be extremely useful whenever control data must be sent to the isolated side, for example to send configuration bits or to implement system test and diagnostics.

This chapter deals with the implementation of the data link of a data/power transfer system, which was also integrated and characterized. A downstream data rate around 20 Mbps and an output current higher than 10 mA were chosen as reasonable targets to be addressed by the system. Taking into account the dropout voltage of a series regulator, the output voltage of the system, V_{OUT}, should be higher than 1.5 V if a supply voltage around 1.2 V is required for the sensor.

3.1 System description

From the architectural point of view, the power link of the proposed system is basically the same described in Chap. 1.2, with proper changes made to perform the required bi-directional data transfer, as shown in Fig. 3.1. It must be pointed out that this architecture exploits a single transformer to implement both power and data transfer, differently from state-of-the-art solutions which employ a separate transformer for each link. This innovative aspect led to a patent application, since several cost advantages and high integration level can be obtained [68].

System implementation

Fig. 3.2 shows the actual implementation of the system with a transistor-level description of the power link. Due to the low output power required, the same CMOS current-reuse transformer-coupled oscillator adopted in [5] and briefly described in App. B was used, whereas the rectifier adopts a traditional CMOS topology. Both

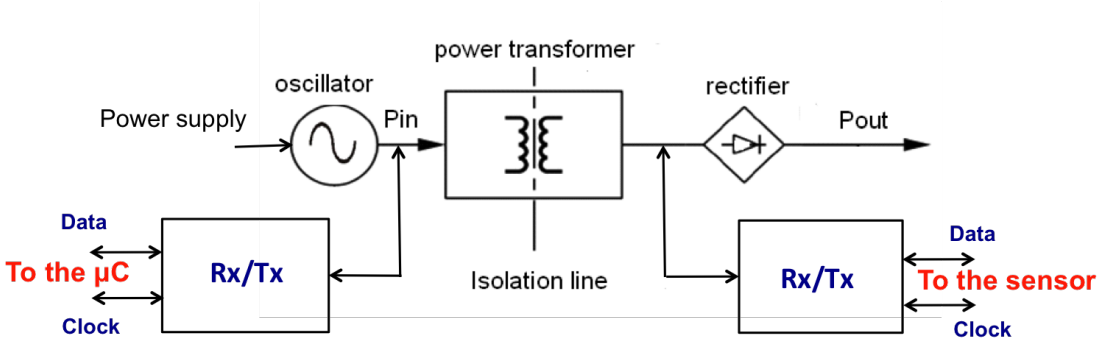


Figure 3.1. Proposed architecture for isolated data/power transfer.

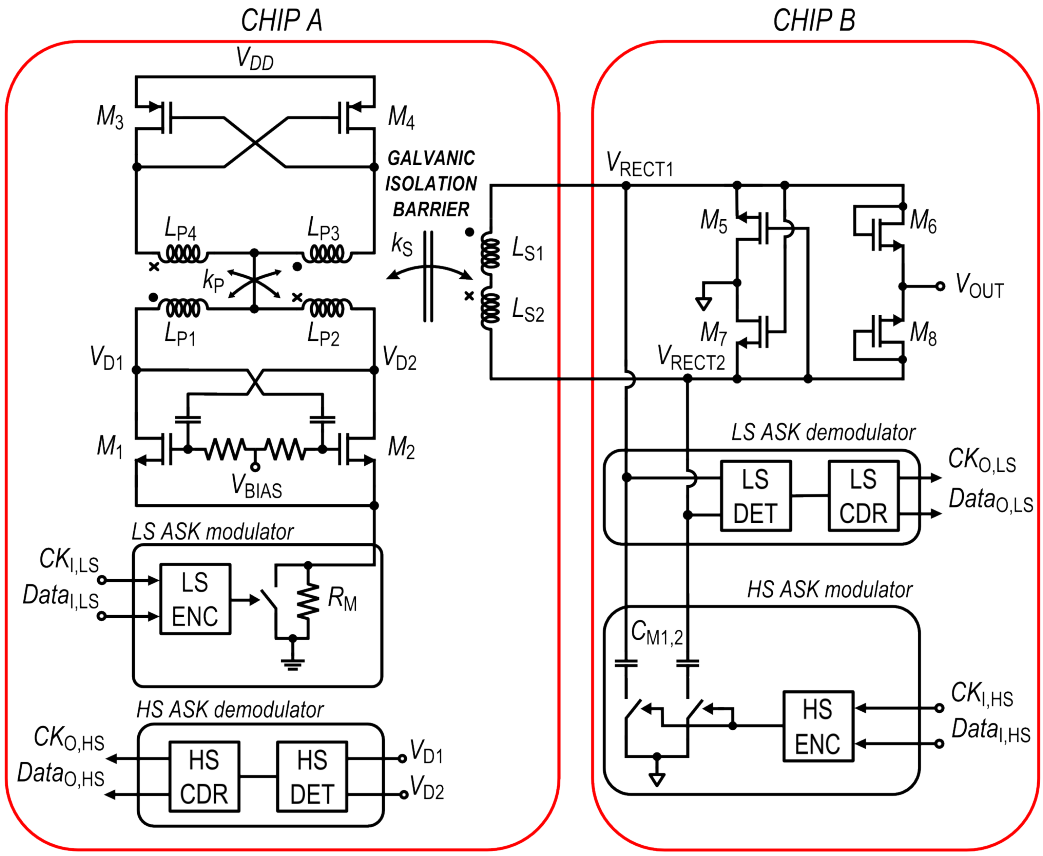


Figure 3.2. Simplified schematic of the isolated data/power transfer system [17] ©2016 IEEE.

dice exploit the same BCD technology described in Chap. 1. Specifically, the supply voltage was set to 3 V to comply with typical micro-controllers supply voltages, and hence 0.35-μm/3-V devices were used for both oscillator and signal circuitry, whereas the rectifier adopts 0.8-μm/5-V devices for the sake of robustness. More details on the power link of the system can be found in [17].

Data transfer link

Further to the data transfer link, the key concept is that data transfer is performed in this system by means of an amplitude-shift-keying (ASK) modulation of the voltage signal at the transformer's coils. It is characterized by the modulation index, h, that is defined as

$$h = \frac{A_{MAX} - A_{MIN}}{A_{MAX}}, \tag{3.1}$$

where A_{MAX} and A_{MIN} are the maximum and minimum amplitudes of the RF power signal. In the following, we denote with high-speed (HS) signals and circuitry related to the downstream link, whereas the ones related to the upstream link are denoted as low-speed or LS.

HS modulation is performed through impedance variation at the secondary coils of the transformer, by using capacitors $C_{M1/2}$ and the respective series-connected switches. The LS modulation is performed through the series resistor R_M which reduces the current and hence the oscillation amplitude of the power oscillator. Lowest h_{HS} is mandatory to do not affect power transfer to the sensor side. Specifically, the HS link adopts $h_{HS} \approx 5\,\%$, measured at the NMOS oscillator's primary windings terminals, $V_{D1/2}$, while a $h_{LS} \approx 25\,\%$ was chosen at the design time as a conservative choice. It is measured at the rectifier's input terminals, $V_{RECT1/2}$. The modulated ASK signal is recovered and converted to rail-to-rail digital signals through the HS and LS ASK detectors, depicted as HS_DET and LS_DET in Fig. 3.2.

PWM modulation

To easily achieve both clock and data transfer with a single link, two encoding blocks, HS_ENC and LS_ENC, perform pulse-width modulation (PWM) coding of the bit stream before the ASK modulators. Similarly, clock and data recovery of the HS and LS bit streams is performed by two decoding blocks, HS_CDR and LS_CDR, connected after the corresponding ASK detectors.

Further to the coding scheme, the duration of the bit, T_{BIT}, is kept constant, with $T_{BIT} = 1/R$ and R is the corresponding HS/LS bit rate, while the bit value is coded into the duration of the high level of the envelope, as shown in Fig. 3.3(a). The encoders, HS_ENC and LS_ENC, are simple digital gates which exploit an 8× oversampling clock reference to implement the PWM stream. The decoders, HS_CDR and LS_CDR, adopt a simple delay-based architecture to recover the bitstream. It is conceptually similar to [1, 2] except for the delay implementation, which is done using digital counters and a second 8× oversampling clock reference.

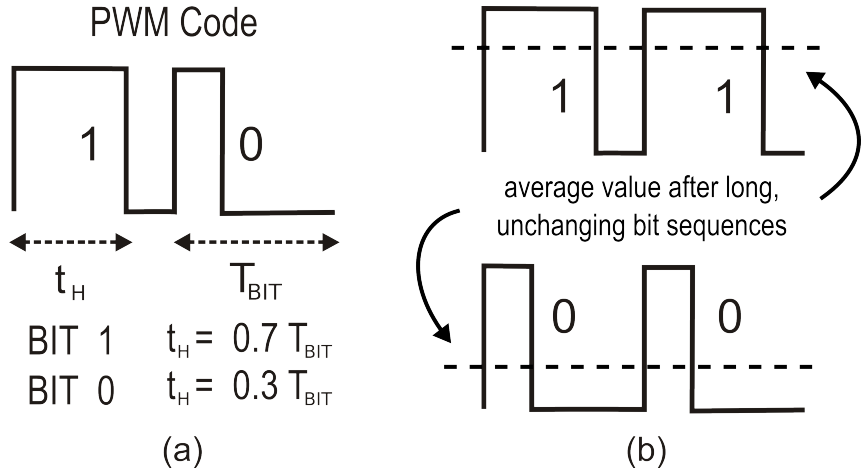


Figure 3.3. (a) PWM coding scheme adopted. (b) Degradation of the detector's noise margin after long sequences of ones or zeros.

Such a coding scheme was chosen due to the straightforward implementation of clock and data extraction circuitry, although this choice considerably affects the

complexity of the ASK detectors. This is due to the fact that bit symbols in PWM have different average value, which means that long sequences of ones and zeros shift the average value towards opposite values of the envelope signal and hence they reduce the noise margin of the detectors, as shown in Fig. 3.3(b). High sensitivity and gain are required to achieve very steep rising/falling edges, which is mandatory to minimize the error due to shifts of the average value. Moreover, the very wide bandwidth of PWM modulations as well as the adopted delay-based detection scheme pose several constraints on the bandwidth of the ASK detectors, especially the HS one [85]. System-level simulations show that at least the third harmonic of the envelope signal must be preserved to avoid significant performance degradation of the adopted CDR decoding blocks. Consequently, the design of the ASK detectors becomes one of the central parts of the proposed system, and it is the subject of this chapter.

3.2 High sensitivity and low power ASK detectors

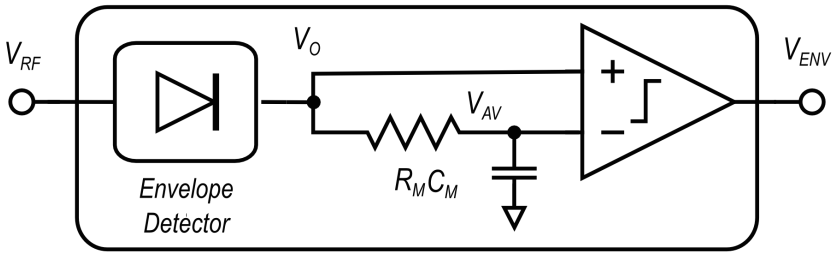


Figure 3.4. Traditional architecture of an ASK detector.

The most popular ASK-detector architecture consists of an envelope detector (ED), followed by a low-pass filter, and a comparator, as shown in Fig. 3.4. V_{RF} is the RF ASK-modulated input signal. The low-pass filter $R_M C_M$ works as an average detector, whose output signal, V_{AV}, is compared with the actual envelope

signal V_O by the comparator, thus obtaining the rail-to-rail digital signal, V_{ENV}. The comparator is often a critical block of the ASK detector. Indeed, its finite gain, offset voltage, and limited common-mode input swing affect the detector sensitivity, which is defined as the minimum envelope variation that can be resolved by the ASK detector. Further to the envelope detector, it can be implemented with passive or active non-linear circuits, by exploiting their even order non-linearities. A straightforward solution is the passive topology shown in Fig. 3.5(a), which is based on a simple diode rectifier [86]. It does not require a bias current but suffers from low input impedance and poor sensitivity. A widespread topology is the common-drain (CD) detector depicted in Fig. 3.5(b) [87]. Its characteristics are simplicity, high input impedance, controlled current consumption, and good input swing, but its conversion gain is also lower than one. Moreover, its output impedance is quite low, which mandates signal processing in the voltage domain to avoid further reduction of signal amplitude and hence signal-to-noise ratio [88].

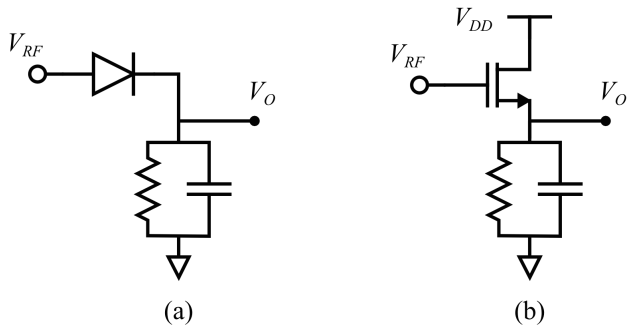


Figure 3.5. (a) Passive, and (b) Common-Drain envelope detectors.

To better understand the trade-offs and the design issues of the HS detector, Fig. 3.6 shows its typical input signal. Specifically, Fig. 3.6(a) shows the typical voltage waveform of the PWM-coded, ASK-modulated signal at the NMOS oscillator drains, $V_{D1/2}$ (see Fig. 3.2), for one HS bit period, $T_{BIT,HS}$. Ideally, this signal remains quite low for half the RF period, to increase the power efficiency when

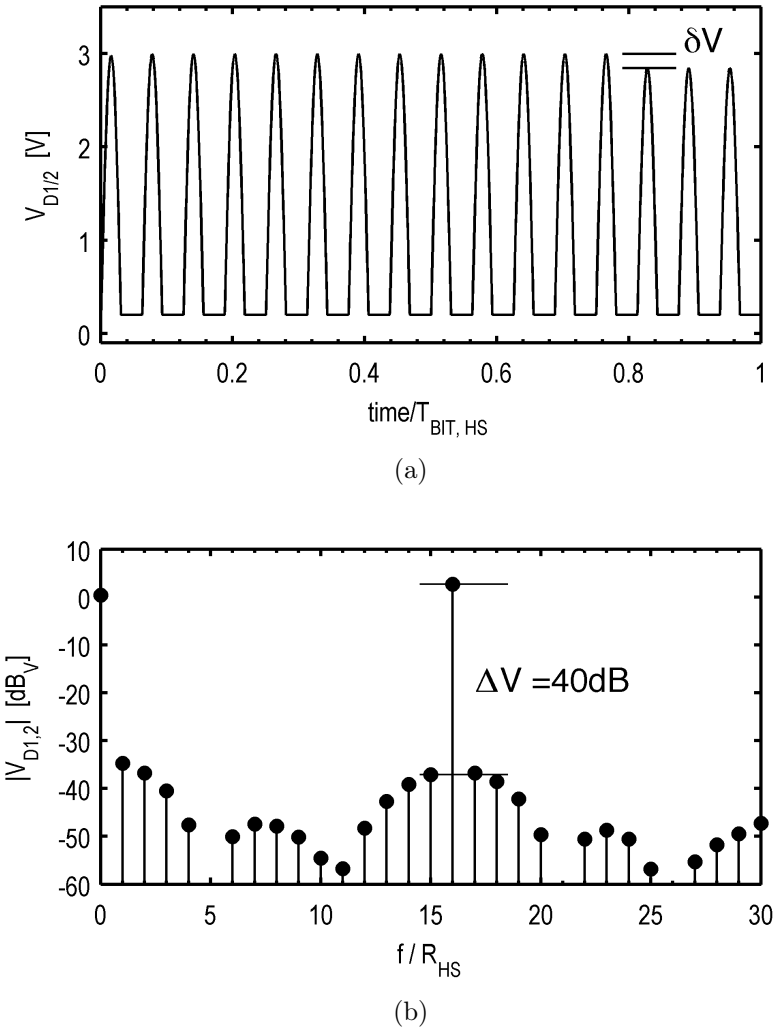


Figure 3.6. Typical (ideal) waveform of the modulated signal at the NMOS oscillator drains, $V_{D1/2}$ (see Fig. 3.2): (a) time domain, (b) frequency domain.

$M_{1/2}$ is on (see Fig. 3.2) and has a sinusoid shape for half the RF period, when the oscillator transistor $M_{1/2}$ is off [71]. A very low ASK modulation is noticeable, here denoted as δV: the envelope signal is around 150 mV over 2.8 V_{PP}, or 5 % of the peak-to-peak signal[1]. Correspondly, Fig. 3.6(b) shows the spectrum of the same voltage waveform. The RF frequency is 320 MHz, i.e. $16 \times R_{HS}$ while the bit rate,

[1]Actually this is not the traditional meaning of the modulation index, being this waveform not symmetric. Still it fits with Eq. 3.1 and therefore it was considered as h_{HS}.

R_{HS}, is 20 Mbps. Spectrum voltages are shown in $\mathrm{dB_V}$, whereas the frequency in the x-axis is shown in terms of R_{HS}. It is worth noting that the first harmonic of the envelope signal is around 40 dB lower then the RF carrier signal, but the frequency content of the signal is quite rich: actually, the third harmonic of the envelope is only 5 dB lower than the first one.

This spectrum is down-converted by the even order non-linearity of the envelope detector, and hence another main issue is worth to be mentioned, that is the high-level of uncertain in the input signal. Fig. 3.6 shows ideal waveforms, which may differ from the actual ones in the operating system. This is due to the high variability of rectifier input impedance and oscillator waveforms with respect to parasitics, process variations and output voltage, which do not provide a clear indication of the waveforms shape and magnitude. On the other hand it is well-known that the conversion gain of envelope detectors also depends on the shape of the RF carrier, thus complicating system design. Although common-drain based detectors may perform well in the proposed system, two novel topologies were instead preferred for the sake of robustness.

3.2.1 Common-Source ASK detector with adaptive biasing

The most interesting solution for high sensitivity and low power consumption for the ED is the common-source (CS) configuration, Fig. 3.7(a): when operated in large signal, the even-order non-linearities of transistor M_0 produce an additional dc drain current that is proportional to the even powers of the input RF signal. If the RC load is designed to cut-off RF frequencies but preserve enough bandwidth to accommodate for the RF envelope signal one, this circuit works as an active envelope detector. This topology exhibits high input and output impedance and hence can provide high conversion gain, but in this case it suffers from an average current consumption which greatly vary with both process, supply voltage, and

temperature (PVT) variations, which highly affect the non-linearity of the transistor. This drawback can lead to envelope distortion, high power consumption, and output saturation, since high uncontrolled gain can force the output node to ground when PVT tolerances are taken into account. Same sensitivity applies with respect to the input signal swing, which can easily saturate the output voltage. This is true especially if low-h ASK modulation must be dealt with, where A_{MAX} and A_{MIN} are closely spaced and their difference can reach the order of the transistor's threshold voltage tolerance.

Accordingly, there are very few examples of CS EDs in literature. In [89] the CS configuration is proposed for the first time, as a high-gain detector for a built-in-self-test circuit. In [90] it is adopted for a millimeter-Wave (mmW) receiver, however the gain increment with respect to the CD ED is smaller than 4 and the operation is restricted to OOK inputs. Similar results in terms of conversion gain are achieved in [91]. In [92] a class-AB biasing is proposed to enhance the non-linearity and gain of the input pair, but a transformer is required and the current consumption is not controlled (i.e., a diode-connected transistor is used to clamp the output voltage). All of these implementations suffer from high variability of the output current, and hence the high gain that the CS stage can provide must be limited to prevent saturation.

Recently, a novel CS high-sensitivity ASK detector architecture has been introduced [18]. This work was done in the early stage of my Ph. D. studies and it was meant to add ASK demodulation capability to a previously developed, RF-powered, batteryless transceiver [93]. It exploits an adaptive-biasing technique to avoid the aforementioned limitations of the CS ED topology, thus achieving high sensitivity with low current consumption. Generally speaking, its conceptual schematic is shown in Fig. 3.7(b) for a full-wave input stage. The peculiar feature of this topology is the use of a feedback loop to control the average output voltage of the common source stage and hence its average output current. The circuit is made up of a CS

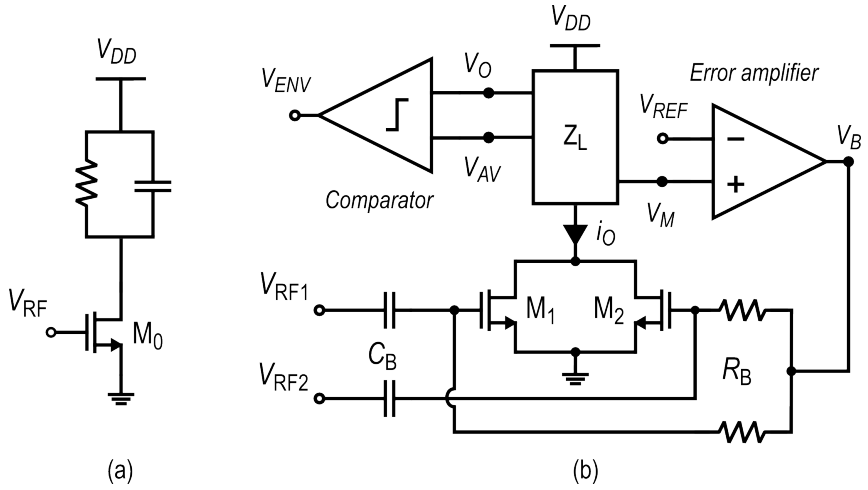


Figure 3.7. (a) Traditional common source envelope detector. (b) Common-source based ASK detector with adaptive biasing [18].

ED, which includes a feedback loop with an error amplifier, and a comparator. The differential RF input, $V_{RF1,2}$, is ac-coupled to the detector by means of a high-pass filter, $R_B C_B$. The output current of the input pair, i_O, is a non-linear function of both V_{RF}, and V_B. It flows into a load network, Z_L, that is used to generate three output signals, that are the envelope signal, V_O its average voltage, V_{AV}, and a voltage proportional to the average voltage, V_M. The feedback loop including the envelope detector and the error amplifier sets voltage V_M to the value of reference voltage V_{REF} and defines accordingly the RF input bias voltage, V_B. This configuration provides several advantages with respect to open-loop CS detectors, i.e. [18]:

- the power consumption is controlled,
- the circuit is robust against PVT tolerances,
- the conversion gain is quite constant for low-h.

Therefore, it was chosen for both the HS and LS detector to guarantee the required sensitivity while ensuring system functionality in a wide range of operating conditions.

3.2.2 High-Speed detector

As shown before, main issues of the HS detector are the strong RF harmonics and the low modulation index. In this context, the high output impedance of the CS detector can be profitably exploited to simplify filtering and amplification of the envelope signal. The simplified schematic of the HS detector is shown in Fig. 3.8. The input signal ($V_{D1/2}$) is halved by using a resistive divider made up by R_{B1-2}

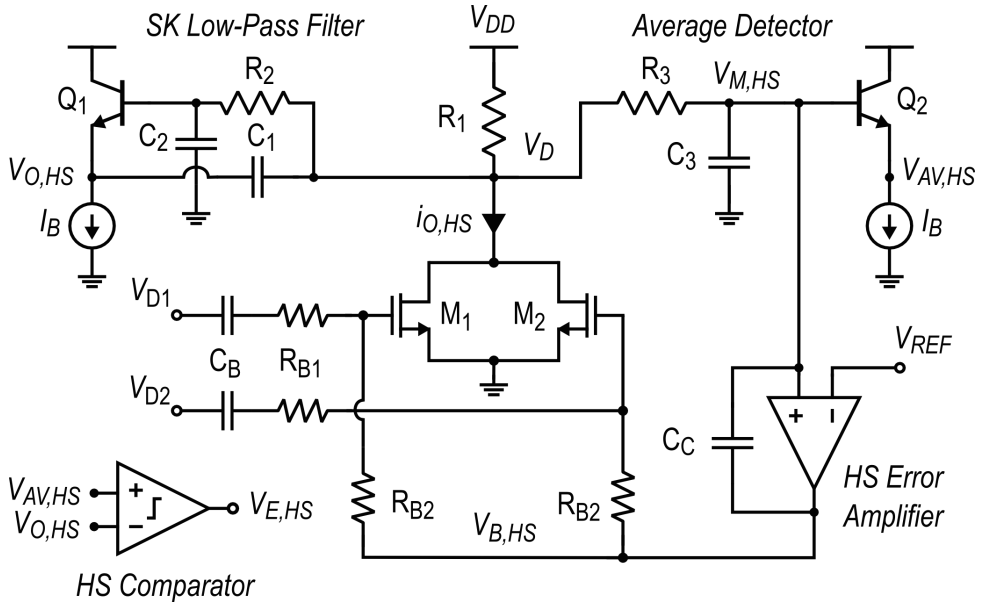


Figure 3.8. Simplified schematic of the HS detector.

and ac-coupled through capacitors C_B to the gate voltages of the input pair, $M_{1/2}$. A simple load resistor, R_1, was preferred to implement wide-band current-to-voltage conversion at the drains of $M_{1/2}$, V_D, due to capacitive parasitics. However, the RF components at this node are still quite high. Therefore, a current-mode, Sallen-Key, low-pass filter is implemented, including resistors $R_{1,2}$, capacitors $C_{1,2}$, and the bipolar transistor Q_1 as active device. A second-order transfer-function with 90-MHz cut-off frequency was chosen. Current-mode signal processing is enabled by the high output impedance of the input stage.

The detector is completed by a replica circuit, including R_3, C_3, and Q_2, which provides the average voltage $V_{AV,HS}$ to the HS comparator, for signal amplification and full-swing envelope rescuing, and the feedback voltage $V_{M,HS}$ to the HS error amplifier, to close the adaptive-biasing loop. Finally, the reference voltage V_{REF} is obtained with a reference current generator and a scaled replica of R_1, not shown in the figure, to ensure PVT accuracy for the system.

Analysis of the loop gain

As already discussed in [18], in this biasing scheme the loop gain, $T_{HS}(j\omega)$, must be designed to do not corrupt the envelope transfer function. Its exact dc value is not a main concern to control the average output current, whereas its gain-bandwidth product must be generally lower than the lowest envelope frequency. The loop implementation and its compensation scheme define how the loop gain affects the envelope transfer function. Indeed, it is worth recalling that $i_{O,HS}$ contains the envelope signal, an average value, which depends on both V_B and the RF signal, and RF harmonics of the input signal. Therefore the conversion gain G_C can be expressed as the product of $i_{O,HS}$ and the equivalent impedance seen at node V_D. In this implementation the output voltage is $V_{O,HS}$, therefore we will look at the trans-impedance $Z_{L,HS} = V_{O,HS}/i_{O,HS}$, which describes how the output current $i_{O,HS}$, produces the output voltage $V_{O,HS}$ and hence is proportional to the conversion gain. Of course it also depends on the loop gain shape.

To better illustrate this point, Fig. 3.9 shows the magnitude of the loop gain, as well as the closed-loop $Z_{L,HS}$, the latter expressed as $20log_{10}(Z_{L,HS}/1\,\Omega)$. Its shape can be intuitively explained with the following:

- At dc $T_{HS}(0)$ attenuates the load impedance R_1, thus rejecting changes in the average value of $i_{O,HS}$.

- At low frequency $T_{HS}(j\omega)$ reduces and hence $Z(j\omega)_{L,HS}$ grows up to R_1 after

the unity-gain frequency.

- At mid and high frequencies $Z_{L,HS}$ is about R_1, and then it follows the Sallen-Key transfer function with a $-40\,\mathrm{dB/decade}$ response.
- At very-high frequencies the attenuation of the filter with respect to R_1 is bounded to around $-30\,\mathrm{dB}$ by the feedforward across Q_1, due to its parasitic capacitances and reduced $\beta(j\omega)$.

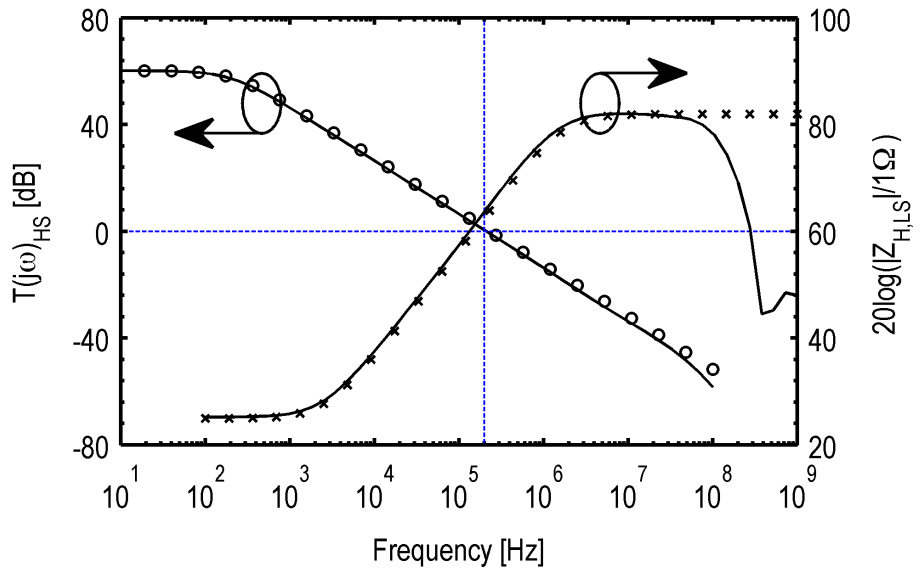


Figure 3.9. Loop gain $T_{HS}(j\omega)$, and closed-loop trans-impedance $Z_{L,HS}$, of the HS detector.

This analysis is confirmed by the following simplified loop gain expression,

$$T_{HS}(s) \approx \frac{g_{m1,2}R_1 g_{mA} r_{oA} \times (1 - s\frac{C_C}{g_{m1,2}}\frac{r_{o1}}{R_1})}{1 + s(r_{oA}C_C[1 + g_{m1,2}R_1] + r_{o1}[C_C + C_3]) + s^2 r_{o1} r_{oA} C_C C_3} \tag{3.2}$$

and by the closed-loop expression of $V_{O,HS}/i_{O,HS}$ that can be approximated as:

$$\frac{V_{O,HS}}{i_{O,HS}} \approx \frac{R_1}{1 + T_0}\frac{1 + sa_1 + s^2 a_2}{1 + sb_1 + s^2 b_2} \tag{3.3}$$

$$
\begin{aligned}
T_{0,HS} &= g_{m1,2} R_1 g_{mA} r_{oA} \\
a_1 &= R_3(C_3 + C_C) + r_{oA}(2C_B + C_C) - g_A r_{oA} R_3 C_C \\
a_2 &= R_3 r_{oA}(C_3 + C_C)(2C_B + C_C) - r_{oA} R_3 C_C^2 \\
b_1 &= \frac{r_{o1}(C_3 + C_C)}{T_{0,HS}} + \frac{r_{oA}(2C_B + C_C)}{T_{0,HS}} + \frac{C_C}{g_{oA}} - \frac{C_C}{g_{m1,2}} \frac{r_{o1}}{R_1} \\
b_2 &= \frac{R_1 r_{oA}(C_3 + C_C)(C_B + C_C)}{T_0} - \frac{C_C^2}{g_{oA}} \frac{r_{o1}}{g_{m1,2} R_1},
\end{aligned}
$$

where $g_{m1,2}$ and g_{mA} are the transconductances of transistors $M_{1,2}$ and the error amplifier, respectively, r_{oA} is the output resistance of the error amplifier and r_{o1} is defined as $R_1 + R_3$. In this expression the transistor Q_1 as well as the effect of $R_{B1,2}$, of the Sallen & Key filter, and of parasitic capacitances at V_D were neglected for the sake of simplicity. Calculated values from Eq. **??** are shown by markers over the respective traces in Fig. 3.9.

Compensation of the loop gain was achieved through capacitor C_C, which exploits the Miller effect across $M_{1,2}$ to produce a dominant pole. However, this is not enough to guarantee correct operation in this circuit and a high absolute value of C_3 is required to eliminate the second pole due to Miller effect: Indeed, without C_3 a short-circuit would occur between V_D and $V_{B,HS}$ at high frequency, thus destroying the load impedance and hence the conversion gain of the detector. Miller compensation is enabled by the high value of $C_3 = 7.5\,\mathrm{pF}$, which effectively shorts $V_{M,HS}$ to ground at high frequencies. A correspondingly high value of $C_C = 7.5\,\mathrm{pF}$ was made necessary also to overcome the detrimental effect on $Z_{L,HS}$ of the high-frequency doublet produced by $R_{B1,2} C_B$. A phase margin of 78° is achieved at a unity-gain frequency of 200 kHz. The system maintains stability in a wide range of input signals, as confirmed by Spectre RF periodic-steady-state (PSS) stability simulations.

The error amplifier is the traditional stacked mirror topology shown in Fig. 3.10, which was chosen to maximize the output swing of the biasing voltage $V_{B,HS}$. The input stage works in weak inversion and the mirror ratio was set to one third to

reduce its overall transconductance, $g_{mA,HS}$. I_{EA} is around 8 μA.

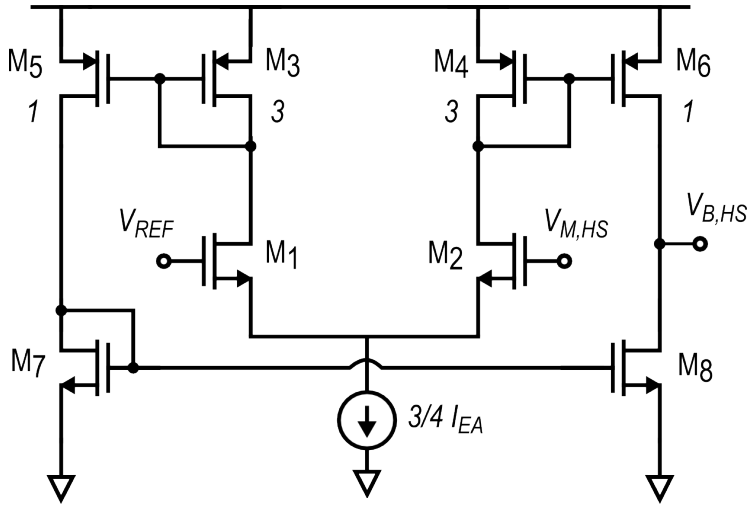


Figure 3.10. Schematic of the HS error amplifier.

Conversion gain and large-signal performance

The overall current consumption of the detector[2], I_{DD}, and the simulated conversion gain provided by the input pair and R_1, $G_{C,HS}$, are shown in Fig. 3.11 for a 20 MHz, 5% square-wave modulated ASK input signal with the shape reported in Fig. 3.6(a) which emulates the oscillator's waveforms at the NMOS drain terminals, $V_{D1/2}$ (see Fig. 3.2). The gain is calculated as the peak-to-peak output signal with respect to the peak-to-peak envelope signal, that is 5 % of the peak voltage A_{PK}, and hence it includes losses of the resistive divider. The peak input signal is reported in the x-axis, i.e. for an input signal with $A_{PK} = 3\,\mathrm{V}$, its envelope is around 150 mV. The gain is around 3.7 dB, therefore the output signal is around 200 mV. It is evident that the current consumption is constant in the whole simulated range. The conversion gain is also quite constant for input voltages between 750 $\mathrm{mV_{PK}}$ to 3.5 $\mathrm{V_{PK}}$ and is

[2]Including biasing.

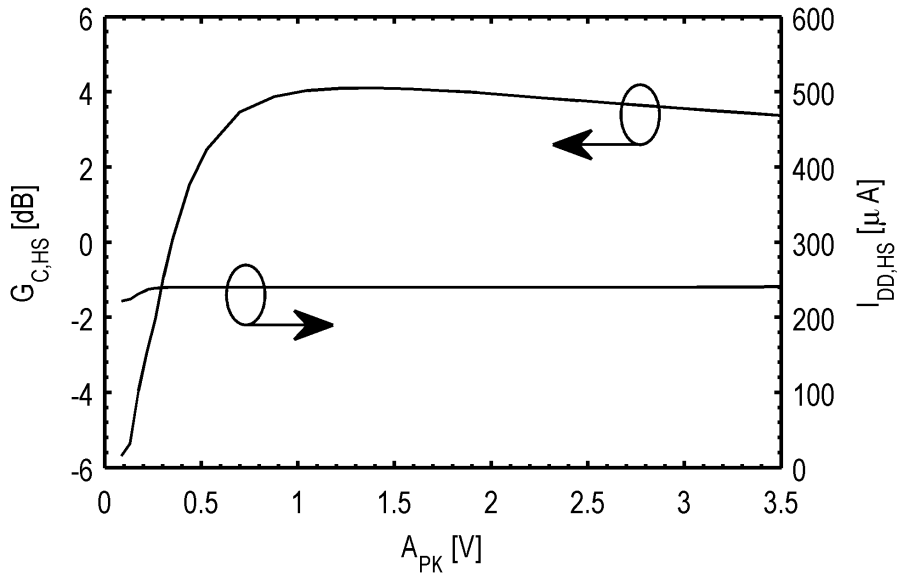


Figure 3.11. Simulated current consumption and conversion gain of the HS detector for a 5% modulated input signal, as a function of the peak input voltage, A_{PK}, for the waveform in Fig. 3.6(a).

around 4 dB. Both are effects of the adaptive biasing approach which provides high robustness with respect to the input signal amplitude. The output signal swing after the current-to-voltage conversion is sufficient to overcome the voltage offset produced by the input stage of the comparator, the current offset of $Q_{1/2}$, as well as their small voltage attenuation. This gain enables the use of Q_1 to implement the Sallen & Key filter, instead of a wide-band, power-hungry amplifier. The action of the adaptive biasing can be seen in Fig. 3.12 where the adaptive biasing voltage V_B is shown as a function of A_{PK}.

Finally, the schematic of the comparator is shown in Fig. 3.13. It consists of two resistively-loaded differential pairs followed by a differential-to-single-ended converter. The first stage takes advantage of a bipolar input pair to minimize the voltage offset. At the output of the SK filter the signal swing is low enough to avoid saturation (IP_2) issues for the first stages, whereas its envelope component is high enough to overcome the input-referred voltage offset. The simple low-pass characteristic

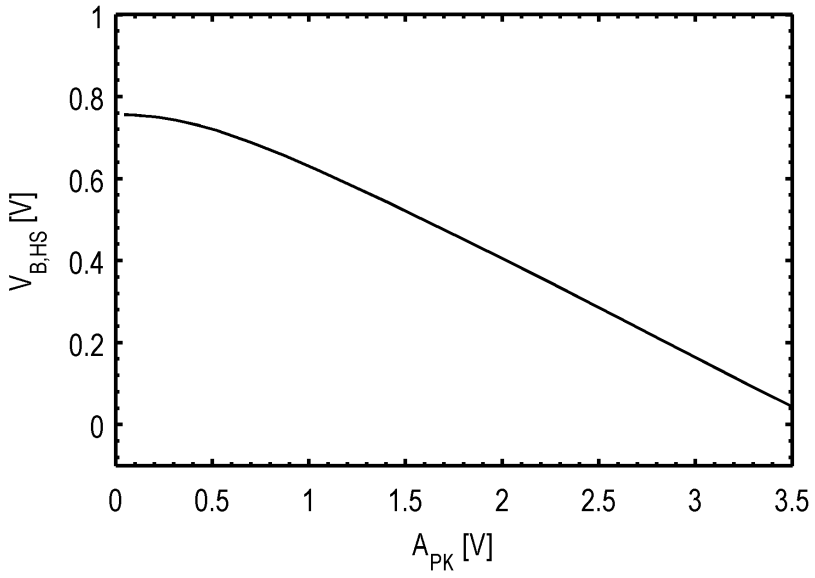


Figure 3.12. Simulated bias voltage of the HS detector for a 5% modulated input signal, as a function of the peak input voltage, A_{PK}.

of the two amplification stages easily provides a few dB's of attenuation which is required to completely suppress the RF signal before the differential-to-single-ended converter. The overall current consumption of the comparator, I_C, is around 100 μA.

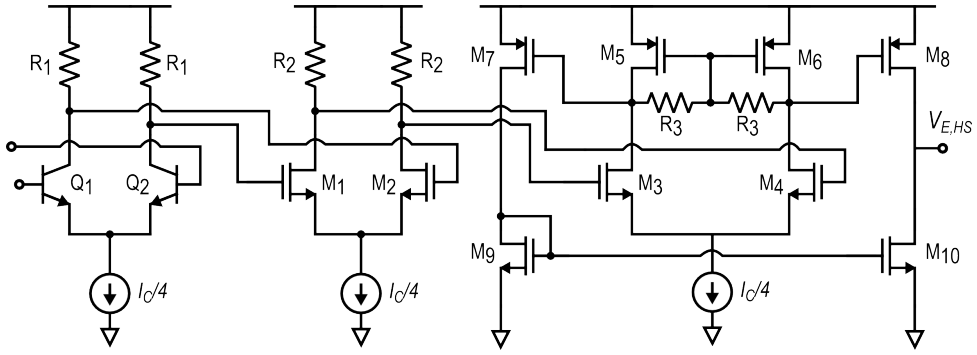


Figure 3.13. Schematic of the HS detector comparator.

Main design parameters of the HS detector are summarized in Table. 3.1.

Table 3.1. Summarized design parameters and simulated performance of the HS detector.

Parameter	Value	Unit
R_1	18	$k\Omega$
$R_{2,3}$	41	$k\Omega$
$R_{B1,2}$	7	$k\Omega$
C_1	40	fF
C_2	20	fF
$C_{3,C}$	7.5	pF
C_B	1	pF
I_B	25	μA
$W_{1/2}$	16	μm
$L_{1/2}$	0.75	μm
G_C @ $h_{HS} = 5\%$	4	dB
I_{DD}	250	μA
Silicon Area	0.054	mm^2

3.2.3 Low-Speed detector

Differently from the HS detector, the LS one has to deal with much lower envelope frequencies, which were estimated in the Mbps range. We chose 1 Mbps as a reasonable upstream bit rate, thus filtering the RF harmonics is quite easy. On the other hand, three different issues arise that are the current consumption of the detector, the relatively lower supply voltage, (i.e. the isolated output voltage V_{OUT}) and the size of the compensation capacitor. Reducing the current consumption is mandatory for the LS detector due to the low efficiency of the power link, and it is easy to obtain by increasing the load resistance of the input pair, but for low-voltage operation and small die area a completely different topology becomes mandatory.

Fig. 3.14 shows a simplified schematic of the LS detector. It is worth nothing that

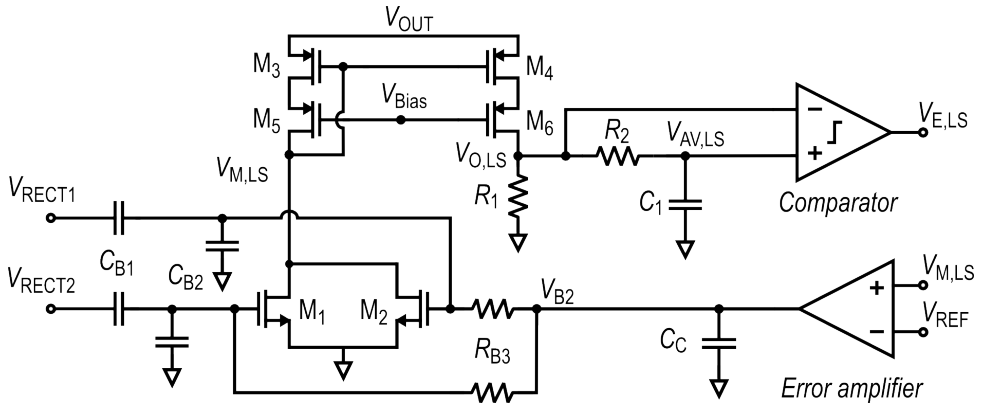


Figure 3.14. Simplified schematic of the LS detector [17] ©2016 IEEE.

at the rectifier input the voltage can be much higher than the supply voltage, e.g. up to $4\,\mathrm{V_{PK}}$, due to the voltage drop on the rectifying devices. A capacitive divider made up by $C_{B3,4}$ was chosen to reduce the input voltage of a factor four while minimizing the resistive loading of the input stage. To cope with the low output voltage without compromising the dynamic of the output node a low-voltage mirror cascode, M_{3-6}, is used to copy and mirror the output current $i_{O,LS}$ while providing a $5\times$ current gain. A high resistive load, R_1, was used for the final voltage-to-current

conversion at the output node, $V_{O,LS}$, whereas low-pass filter R_2C_1 is used to recover the average voltage for the comparator, $V_{AV,LS}$. The feedback signal for the error amplifier, $V_{M,LS}$, comes from the low-impedance gate of M_4, which provides several advantages.

Indeed, the robustness of the topology and its area efficiency increases with respect to the HS detector, since the pole of the average detector R_2C_1 is outside the loop gain path [94]. This is demonstrated in Fig. 3.15, where the current-to-voltage transfer function, $Z_{L,LS} = V_{O,LS}/i_{O,LS}$, and the loop-gain magnitude of the LS detector, $T_{LS}(j\omega)$ are depicted. They can be expressed as follows, if the parasitic

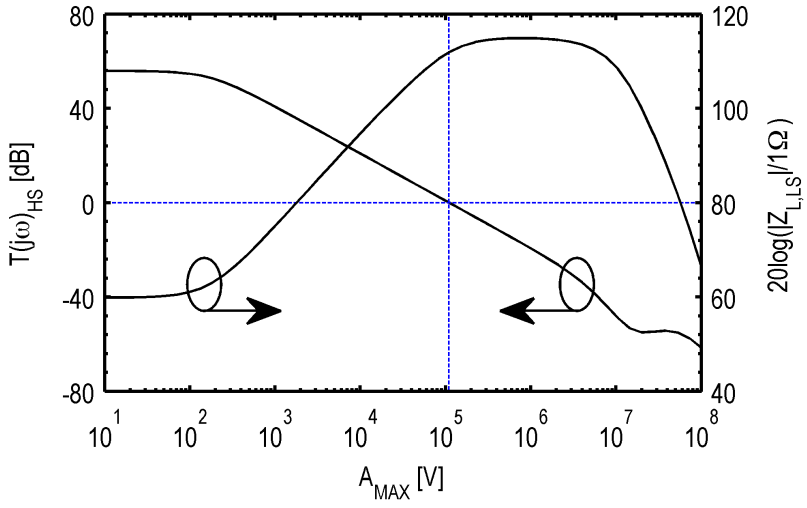


Figure 3.15. Loop gain $T_{LS}(j\omega)$, and closed-loop trans-impedance $Z_{L,LS}$, of the LS detector.

capacitance at $V_{M,LS}$ and $V_{O,LS}$ is neglected:

$$T_{LS}(s) \approx \frac{T_{0,LS}}{1+sr_{oA}C_C} \tag{3.4}$$

$$\frac{V_{O,LS}}{i_{O,LS}} \approx \frac{g_{m4}}{g_{m3}}\frac{R_1}{1+T_{0,LS}}\frac{1+sr_{oA}C_C}{1+s\frac{r_{oA}C_C}{1+T_{0,LS}}}, with \tag{3.5}$$

$$T_{0,LS} = \frac{g_{m1,2}}{g_{m3}}g_{mA}r_{oA}.$$

Here symbols have the same meaning of Eq. 3.4. Eq. 3.5 and 3.6 predict that the

unity-gain frequency of $T_{LS}(j\omega)$ corresponds to the high-pass corner frequency of $Z_{L,LS}$, which is in contrast with Eq. 3.2 and 3.4, where the former must be quite lower than the latter to guarantee stability (see Fig. 3.9). Therefore, for the target bit rate of the LS detector, Miller compensation would require prohibitively larger compensation capacitors, besides raising stability issues.

Although the single pole transfer function, the compensation capacitor C_C is still required to define and control the lower bounds for the LS bit rate. It was set to 7.5 pF, which leads to both a unity-gain and a high-pass frequency of 110 kHz with lower area occupation with respect to the HS detector. The error amplifier is again a stacked-mirror topology biased in sub-threshold with one-third mirror ratio. Its schematic is the same as the one in Fig. 3.10, with ($I_{OTA} = 2\,\mu$A). Higher channel lengths were used for the transistors with respect to the HS error amplifier to further minimize voltage offset .

It is worth noting the much higher trans-impedance gain of this circuit when compared to the HS detector, thanks to the higher load resistance ($R_4 = 150\,\text{k}\Omega$) and the current mirror amplification. For lower h_{LS} the overall conversion gain $G_{C,LS}$ is as high as 10 dB including the capacitive divider losses, as shown in Fig. 3.16 for $h_{LS} = 5\,\%$ and $V_{OUT} = 2.5\,\text{V}$. The input waveform of the rectifier is similar to the oscillator's one in Fig. 3.6(a) and hence it was used also for the design of the LS detector. For higher modulation indexes or lower supply voltages output swing saturation occurs and the gain reduces, being around 6 dB for $h_{LS} \approx 25\%$ and $A_{PK} = 4\,\text{V}$ in this case. The input-dependent bias voltage $V_{B,LS}$ is shown in Fig. 3.17.

Fig. 3.18 shows the schematic of the LS comparator. It is a simple resistor-loaded differential pair followed by a differential-to-single-ended converter for the sake of robustness. Its current consumption is 6 μA and accounts for 24 % of the overall current consumption of the detector, that is lower than 30 μA in dynamic conditions. Main design parameters of the LS detector are reported in Table. 3.2.

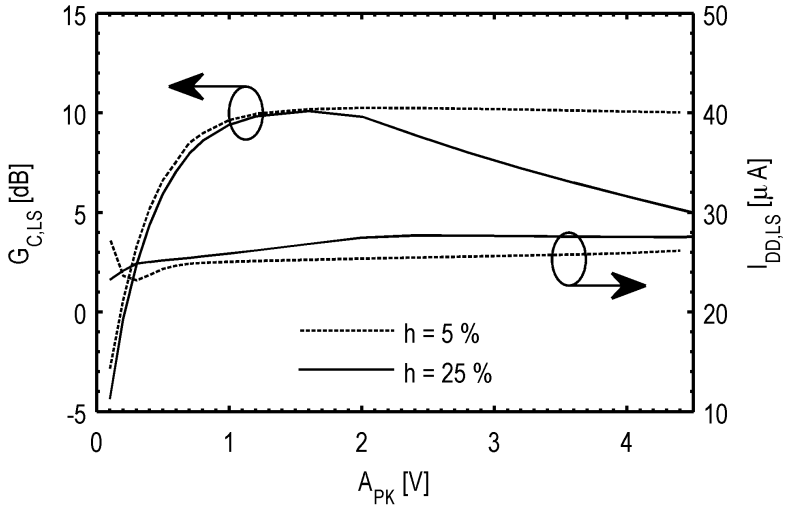


Figure 3.16. Simulated current consumption and conversion gain of the LS detector for a 5% and a 25% modulated input signals, as a function of the peak input voltage, A_{PK}, for the waveform in Fig. 3.6(a).

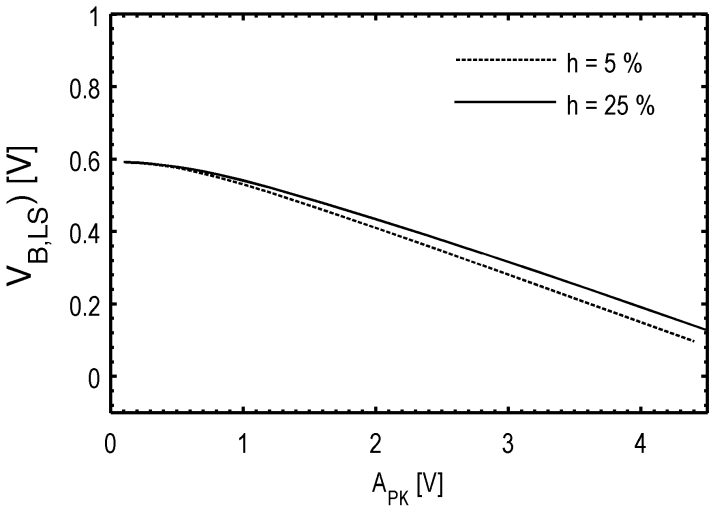


Figure 3.17. Simulated bias voltage of the LS detector for a 5% and a 25% modulated input signals, as a function of the peak input voltage, A_{PK}.

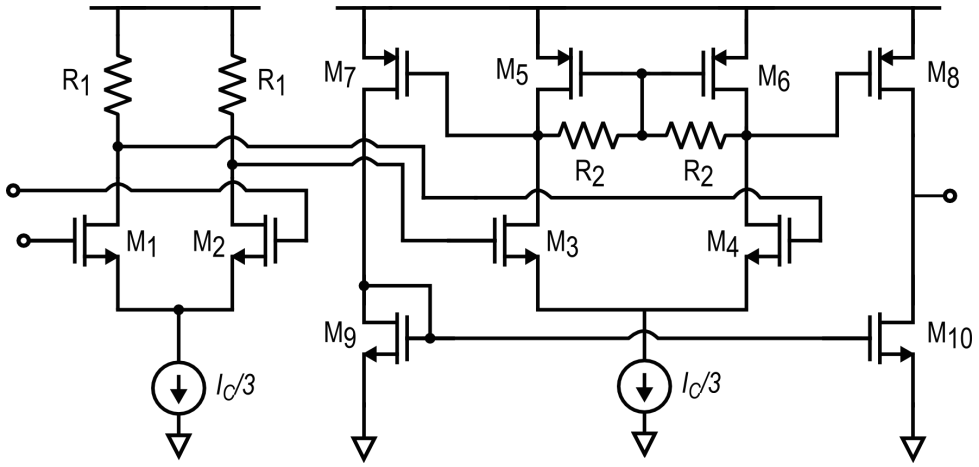


Figure 3.18. Schematic of the LS detector comparator.

Table 3.2. Summarized design parameters and simulated performance of the LS detector.

Parameter	Value	Unit
R_1	125	$k\Omega$
R_2	1	$M\Omega$
C_{B1}	100	fF
C_{B2}	400	fF
$C_{C,1}$	7.5	pF
$W_{1/2}$	12	μm
$L_{1/2}$	0.5	μm
G_C @ $h_{HS} = 5\%$	10	dB
I_{DD}	25	μA
Area	0.038	μm^2

3.3 Measurement results

The proposed detectors were integrated in the adopted BCD technology and measured in different operating conditions within the overall data/power transfer system. A micrograph of the two chips assembled on-board is shown in Fig. 3.19 with main blocks high-lighted. The chip are directly attached and wire-bonded on a FR4 printed circuit board for test purposes. It is worth noting the relative size of the isolation transformer and the direct connection between the secondary coil and the rectifier's input pads. The rectifier die has the same area of the oscillator die, being pad-limited due to the high number of internal signals which were taken off-chip for monitoring and configuration.

Four samples of the whole system were tested at different supply and output voltages showing sufficient output current to power up a wide range of sensors. More details on the power transfer performance of the systems are found in [17].

In this section the performance of the data transfer is reported, which was assessed by bit-error-rate (BER) measurements.

3.3.1 Measurement setup

Due to the lack of proper instrumentation for BER measurements, a customized set-up was used to estimate the BER of the data links, i.e. their quality. This is typically measured in terms of the highest bit-rate that the system can process while providing a BER lower than 10^{-3}.

The physical setup is described in Fig. 3.20. When each data link is active, the system requires two synchronized signals, here shown as $Data_{IN}$ and CK_{IN}, representing the input data and the respective clock signal for synchronous communication. They were generated by using the in-phase and in-quadrature baseband signals of a Agilent E4438C ESG vector signal generator (VSG), i.e. I_{OUT} and Q_{OUT} respectively. Two 8× oversampling reference clocks, CK_{REF}, are required by the

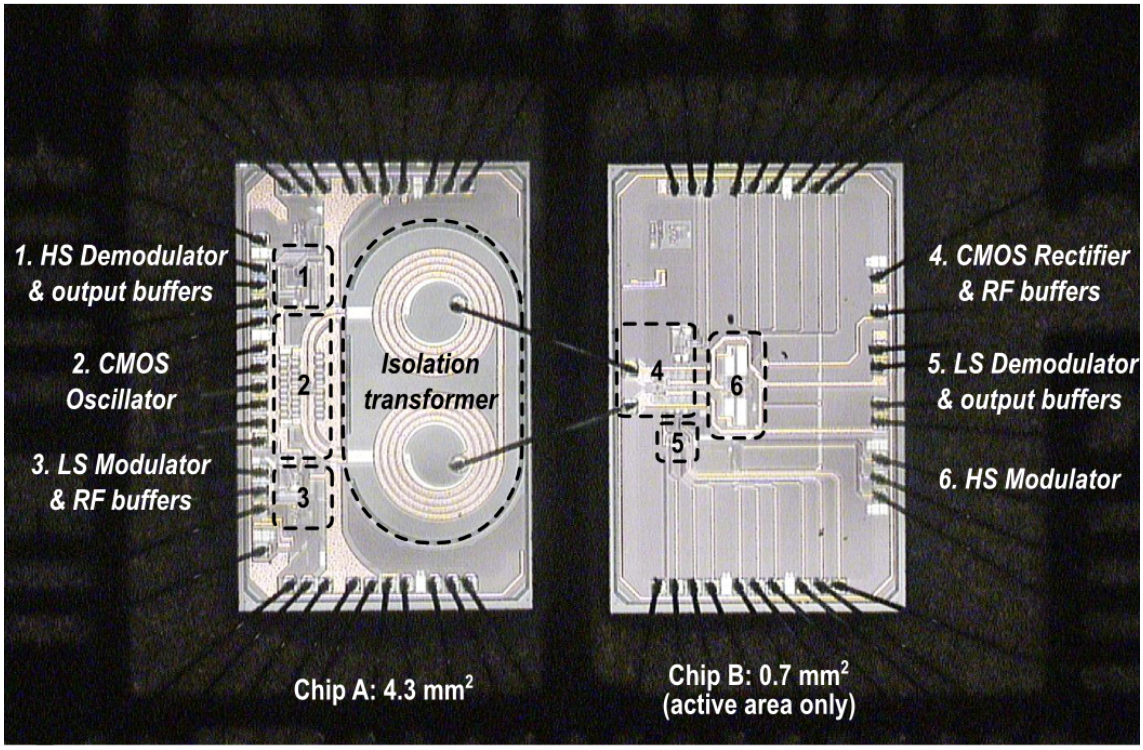


Figure 3.19. Micrograph of the CMOS isolated power/data transfer system [17] ©2016 IEEE.

HS/LS_ENC and HS/LS_CDR to perform PWM modulation and demodulation. They were provided by an Agilent 81160A and an Agilent N5171B signal generators. Finally, a digital sampling oscilloscope, Agilent MSO9104A, was connected to the demodulated data and clock recovery outputs of the HS/LS_CDR block, here shown as D_{OUT} and CK_{OUT}, through a digital input active probe. It acquires also the input signals $Data_{IN}$ and CK_{IN}. All the measurement instruments were connected to a PC with Labview through a GPIB bus and a GPIB to Ethernet adapter, for automated measurements. Input and output voltages for the two chips were forced and measured during measurements, respectively, with an HP 4156C semiconductor

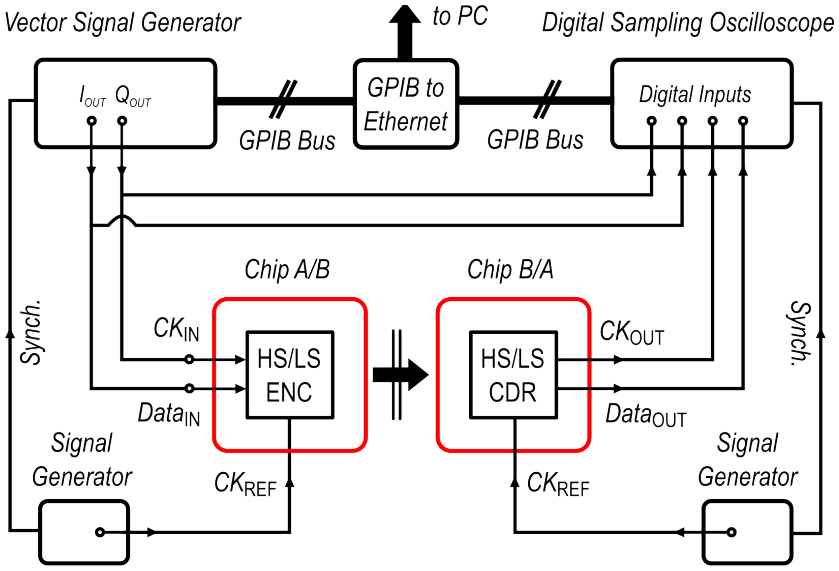


Figure 3.20. Simplified description of the BER measurement setup.

parameter analyzer.

A customized LabView software was used to perform the measurements. Fig. 3.21 shows the simplified flow-chart diagram of the measurement system software. Due to the limited speed of the GPIB as well as limited memory buffers of both Ethernet adapter and oscilloscope, BER measurements were performed in discrete steps. First a random bit vector, B, is generated and split in smaller vectors, whose size M depends on the bit rate, and on the oscilloscope memory buffer, as well as on its sampling frequency. Then the vector signal generator is programmed to provide $Data_{IN}$ and CK_{IN} signals to the first chip and the oscilloscope start sampling the digital inputs. After the memory buffer of the oscilloscope is filled data are transferred to LabView for a post-processing where $Data_{IN/OUT}$ signals are sampled in correspondence of the respective $CK_{IN/OUT}$ signals to recover two digital bitstream. Finally the input and output bit-streams are compared: bit errors are counted and stored and the measurement starts again until enough bits or errors are counted. Tests were generally performed to measure at least 10^5 bits.

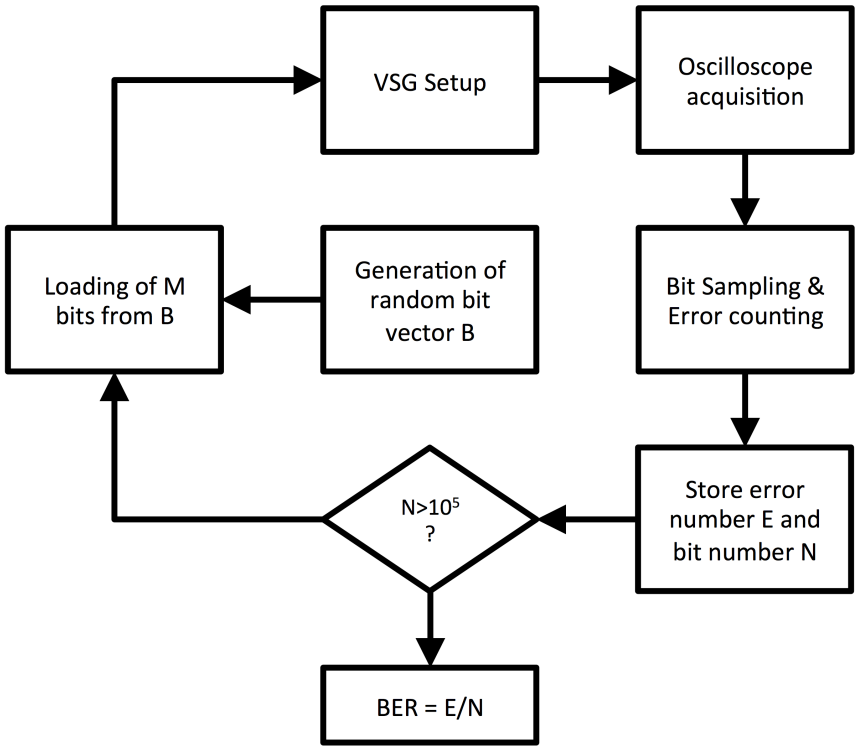


Figure 3.21. Simplified flow-chart diagram of the BER measurement system.

3.3.2 High-Speed data transfer

Figures 3.22, 3.23, and 3.24, show the key measured data-link waveforms for minimum, nominal and maximum R_{HS} bit-rate. Both input and output clock and data signal are shown as well as the envelope signal at the comparator output, $V_{E,HS}$, and the analog detector's output signals, $V_{O,HS}$ and $V_{AV,HS}$. The output signal of the drain node is also shown. It was measured by exploiting an RF output buffer and it is plotted normalized with respect to its peak value to make the ASK modulation noticeable. The time axis is normalized to the bit-rate to easily recognize each bit period.

The lower bound for R_{HS} is around 2.5 Mbps, since a BER of 3.63×10^{-3} was measured at $R_{HS} = 1$ Mbps. The relatively low bit-rate, comparable with the low cut-off frequency of $Z_{L,HS}$ in this case, gives enough time to the average value $V_{AV,HS}$

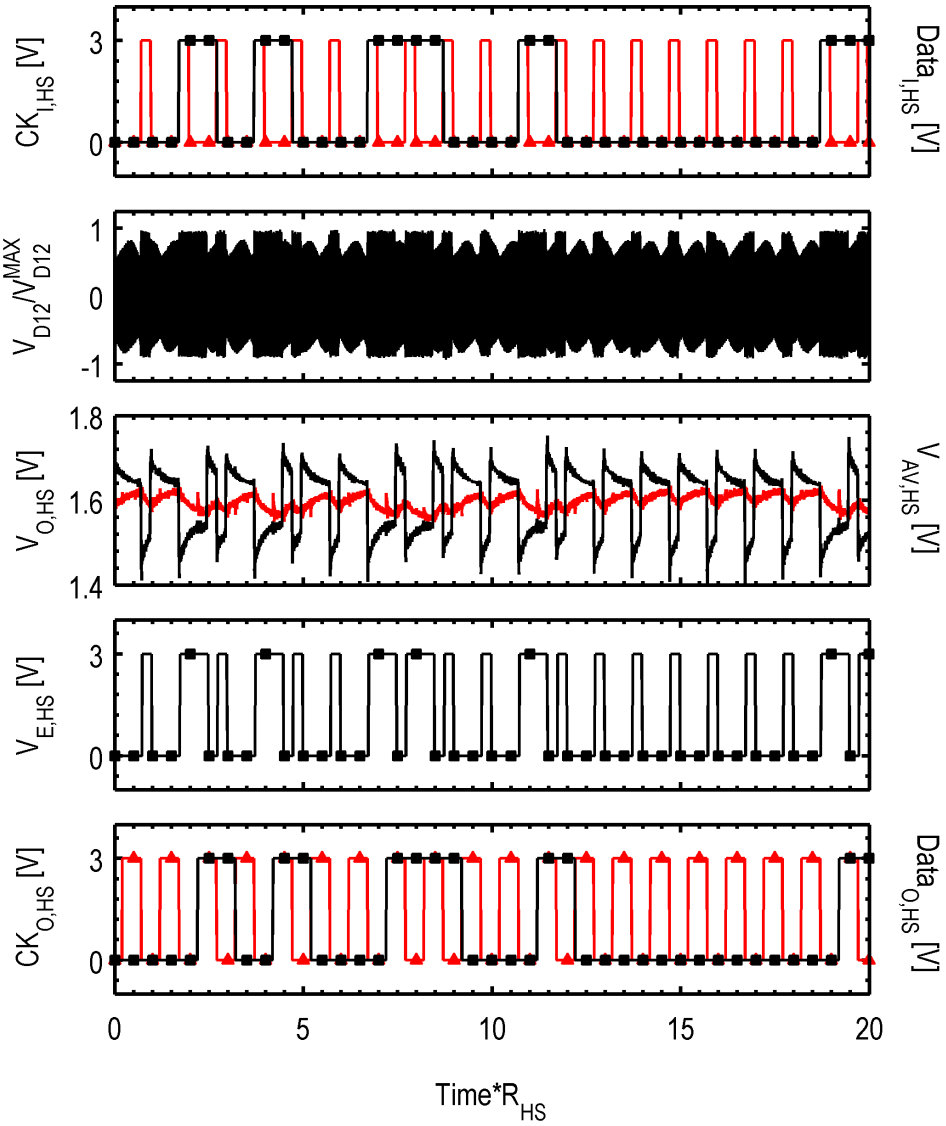


Figure 3.22. Measured HS data link waveforms at 2.5 Mbps.

and output voltage $V_{O,HS}$ to converge. The RF signals in the figure appear distorted due to aliasing, since the sampling frequency of the oscilloscope had to be kept low enough to capture a wide acquisition time.

The output swing for the nominal 20-Mbps bit-rate is around 250 mV, which is slightly higher when compared to simulated values due to non-idealities in the

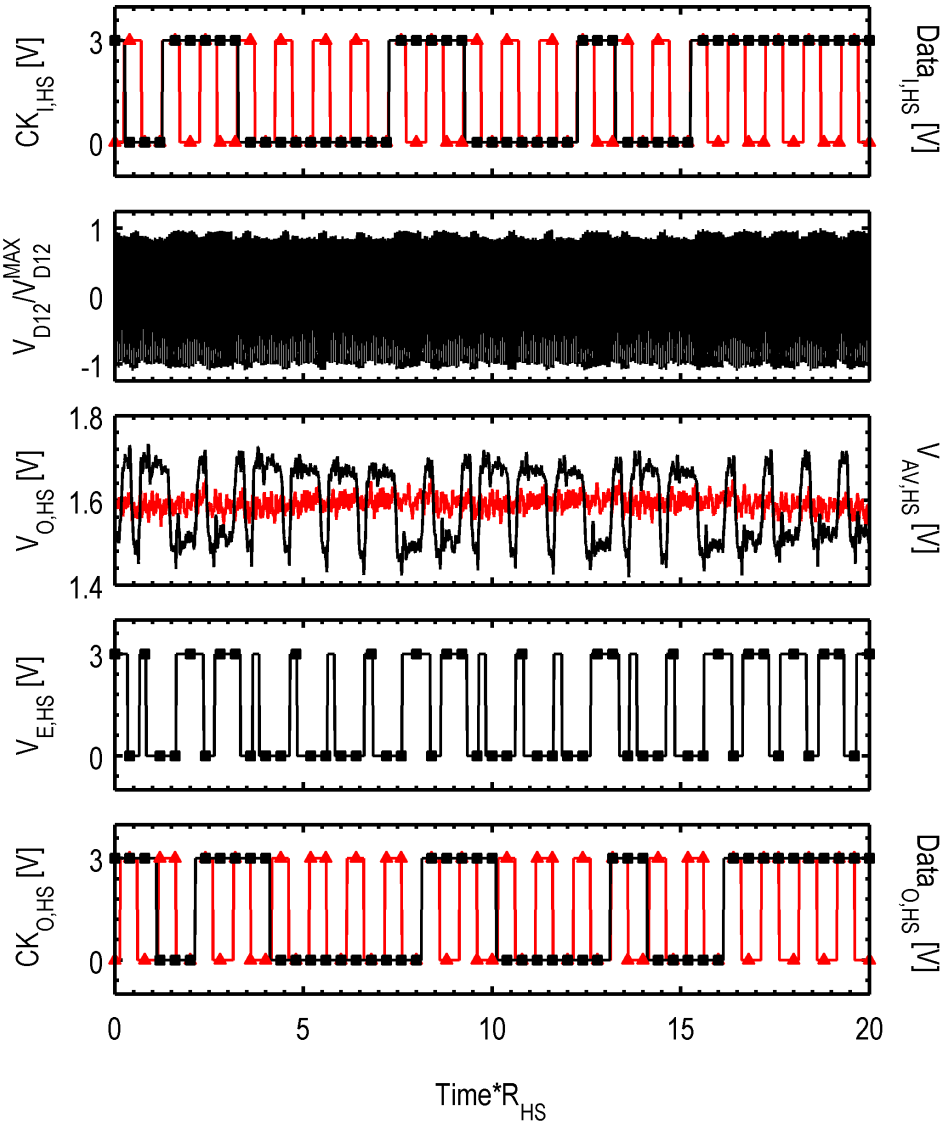


Figure 3.23. Measured HS data link waveforms at 20 Mbps.

oscillator's waveforms with respect to the simplified model in Fig. 3.6.

The upper bound for R_{HS} was actually limited to 40 Mbps by the measurement setup, due to the lack of a second oversampling clock reference synchronized with the VSG, although noise margin at this bit rate is already quite low, as shown in Fig. 3.24. It can be noticed also in the PWM waveform, where some zero-coded bits

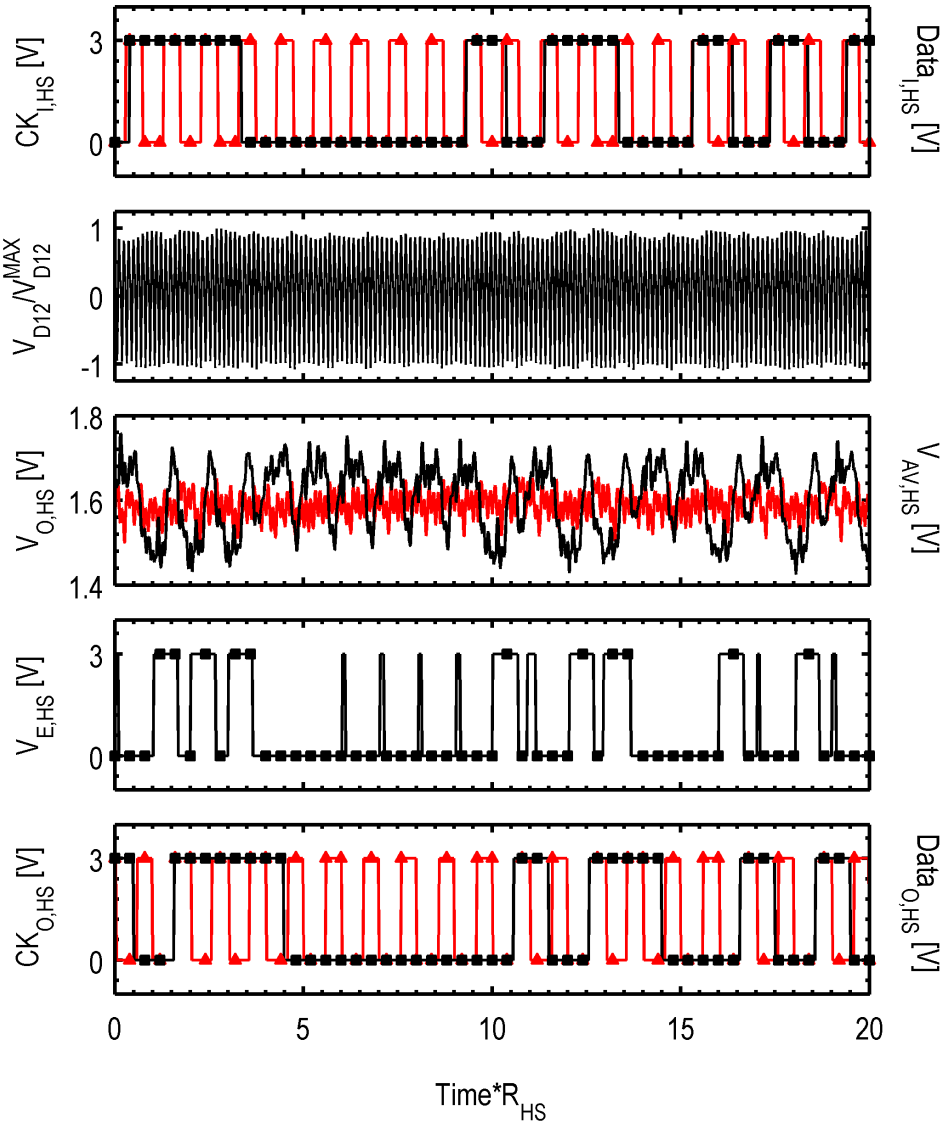


Figure 3.24. Measured HS data link waveforms at 40 Mbps.

are so short that the relatively low sampling frequency of the oscilloscope is not able to capture them.

3.3.3 Low-Speed data transfer

Finally, Fig. 3.25, 3.26, and 3.27 show the key measured data-link waveforms for minimum, nominal, and maximum R_{LS} bit-rate. The latter was estimated in 3 Mbps since the BER is around 2.89×10^{-3} at $R_{LS} = 6$ Mbps.

Lower bound for R_{LS} is 150 kbps: in this case the bit rate is comparable with the loop bandwidth and hence the error amplifier works in slew-rate at the beginning of each bit: it is almost fast enough to compensate for the envelope signal, although $V_{O,LS}$ and V_{AV} never cross each other because of the single-pole loop-gain transfer function, which shows no overshoot nor ringing when the slew-rate condition ends.

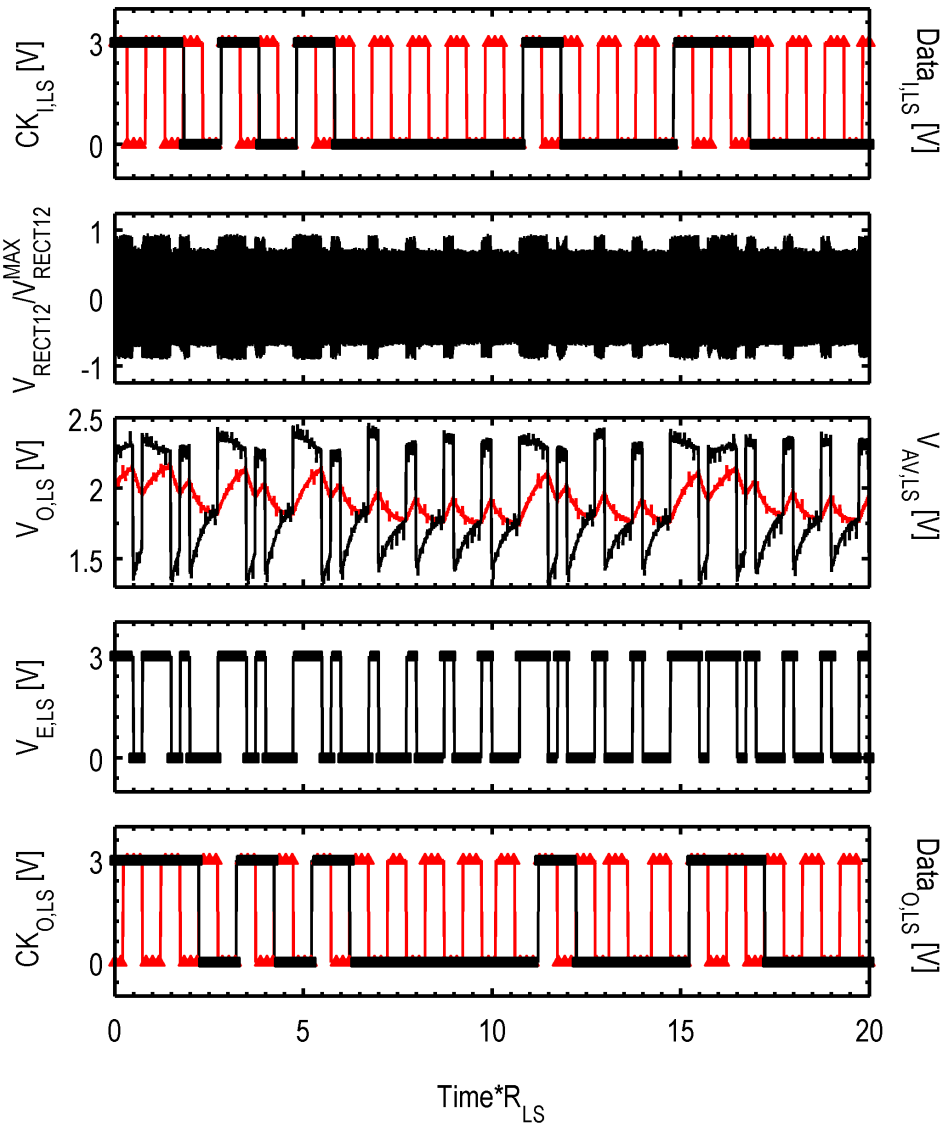


Figure 3.25. Measured LS data link at 150 kbps.

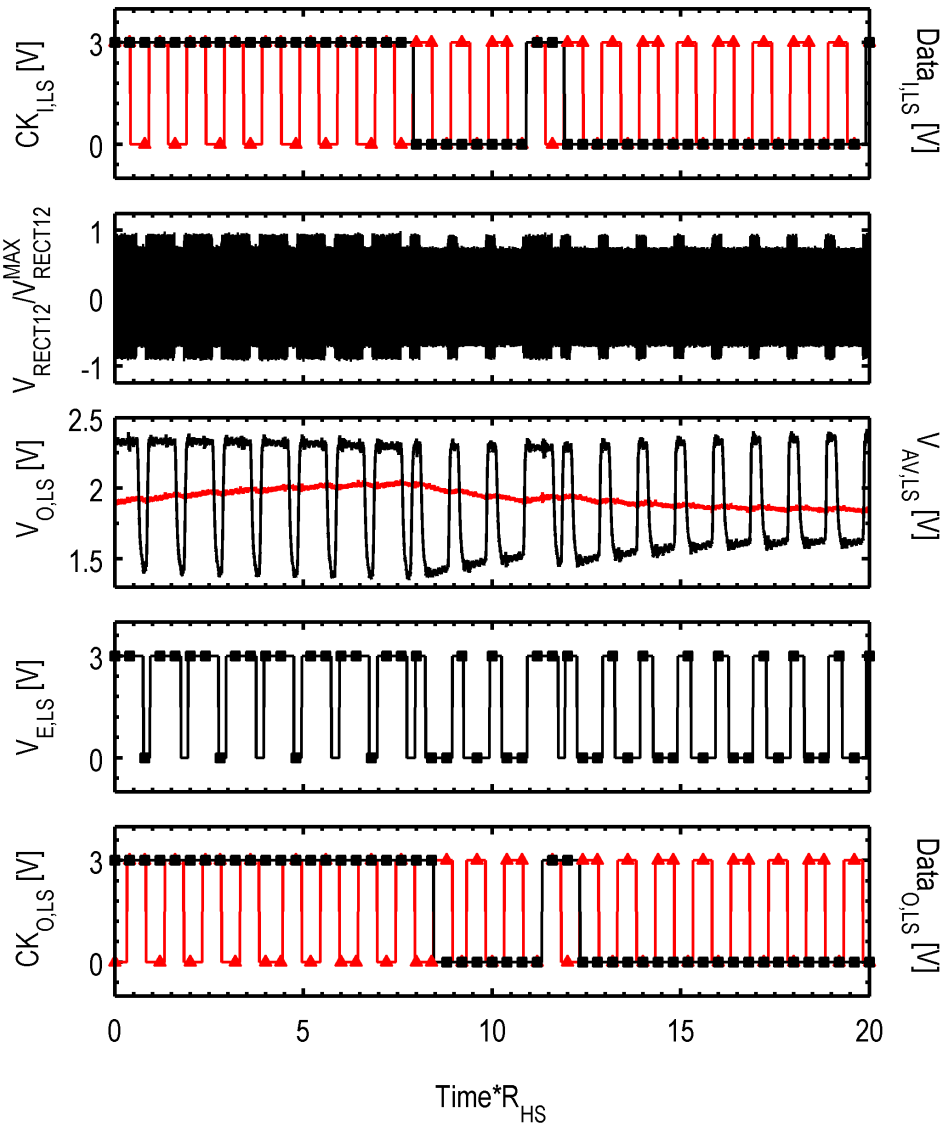


Figure 3.26. Measured LS data link at 1 Mbps.

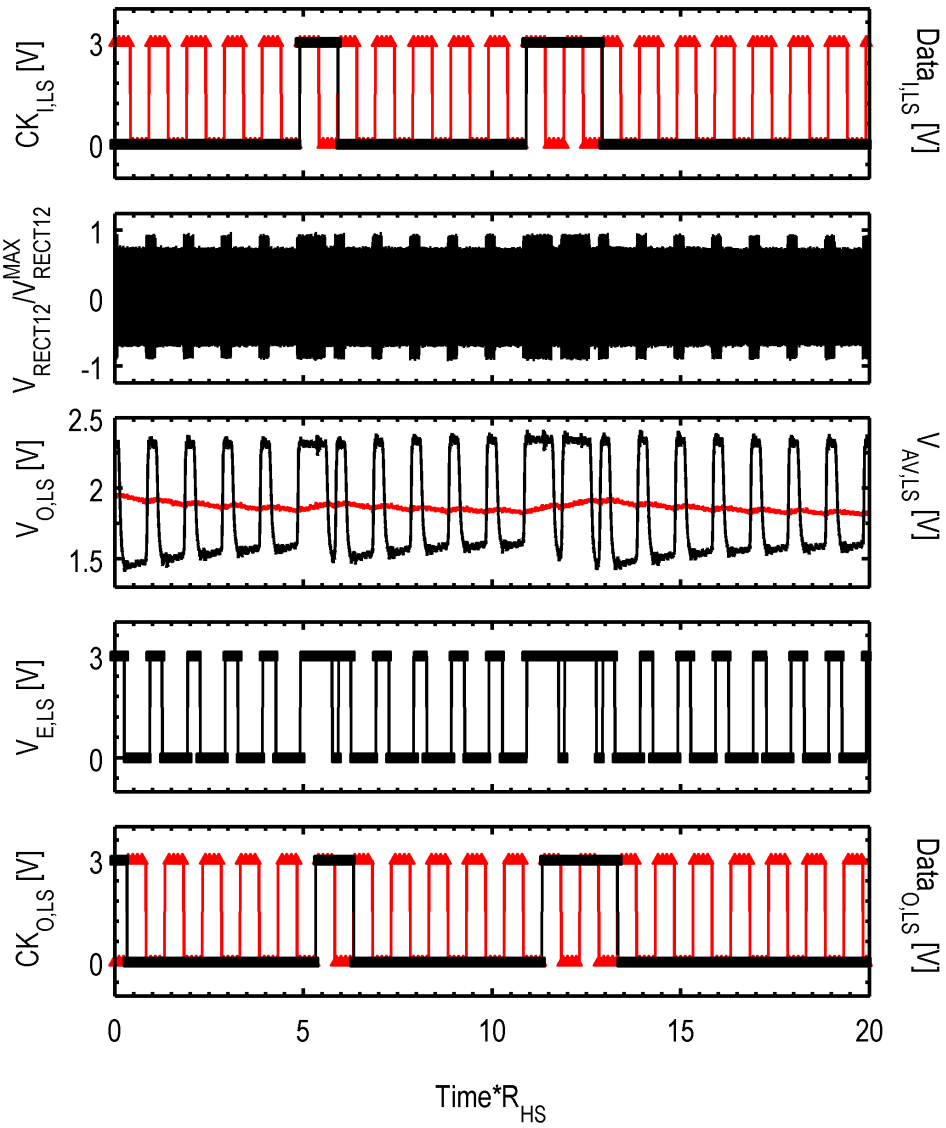


Figure 3.27. Measured LS data link at 3 Mbps.

Chapter 4

Conclusion

This chapter summarizes main results and outcomes of this work, while open questions and possible future works are also discussed.

Power transfer systems

In Chap. 2 the design and characterization of a galvanically isolated, watt-level, step-up, dc-dc converter in silicon technology is reported. A thorough analysis of the power efficiency of the system shows that design for power transfer in current silicon technologies is not trivial and a co-design approach is mandatory to properly exploit the fully integrated approach and achieve meaningful results. A lumped, geometrically scalable model for integrated transformers is introduced with a novel empirical expression for the series resistance of the coils. A co-design procedure is also proposed to fully exploit the integrated approach by taking into account the interactions between building blocks, which takes advantage of the aforementioned transformer model, and the power density constraint that dictates the cost of the converter.

The result of this work is a system that, in spite of the adoption of standard metal layers, achieves better or similar power-transfer performance compared to

state-of-the-art commercial products that, on the other hand, adopt post-processed transformers with polyimide dielectrics and 6-μm thick Au metals for the coils, implemented as a third, single die in a system in package configuration. Therefore, the highest level of integration has been achieved since only two dice were used without any post processing steps. Peak output power and power efficiency are higher than 710 mW and 26%. It was also demonstrated that with minor improvements in the back-end-of-line (BEOL) technology they can reach peak values around 1 W and 30%. Achieved results show that, thanks to the proposed design procedure, this work also advances the state of the art of fully integrated inductive step-up converters for both peak power and power density, even without the improved metal back-end or including thermal effects.

Besides these main achievements, App. B describes also my contributions on the design of two more dc-dc converters which only need for CMOS devices instead of the LDMOS adopted in my main work.

The following conclusions can be drawn:

- For the first time, this work shows the feasibility of galvanically isolated power conversion up to 1 W, with power efficiency up to about 30%, in a fully integrated implementation.

- This work greatly advances the state of the art of fully integrated inductive step-up converters in terms of both output power and power efficiency with outstanding power density, apart from providing on-chip galvanic isolation.

- Experimental characterization also demonstrates that significant improvements in terms of power density and power efficiency can be achieved by exploiting optimized metal back-end and proper device modeling.

Data transfer systems

In Chap. 3 the design of the receiver of a data/power transfer system providing on-chip galvanic isolation is discussed. The proposed system has been integrated and successfully characterized in the available silicon technology, thus demonstrating for the first time both power transfer and half-duplex, bi-directional data communication by means of ASK modulation, while providing also galvanic isolation and using only a single integrated isolation transformer in the aforementioned technology. The implementation of such a system involved several circuit and system-level issues, that were properly addressed at design time.

Two novel common-source based ASK detectors with adaptive biasing were introduced (apart from the first one, introduced in [18] for different purposes) and shown in this work to provide half-duplex data communication with high level of robustness. In spite of the many drawbacks of the adopted PWM coding, this circuitry performed very well during all measurement conditions, particularly the LS detector, which introduces a robust and area-efficient topology. The HS detector easily covered two times the nominal system bandwidth of 20 Mbps, being actually limited by the measurement setup. Modulation index of only 5% in this case limits the reduction in output power and power efficiency due to ASK modulation, therefore increasing system performance.

To the best of the author's knowledge this is the first reported system able to integrate all those function by using only two silicon chips, and hence it could represent a serious breakthrough in the field of fully integrated interfaces for sensor applications.

Open issues

Due to the relatively low time and limited resources, the following open questions remain to be addressed to increase performance and reliability of the power converters:

- Thermal issues - due to the relatively low power efficiency, they should be included in the developed co-design procedure for a more optimized design; furthermore, apart from reducing efficiency, high operating temperatures may also affect the start-up time of the oscillators.

- Start-up circuitry - as discussed, it may be necessary to enable operation at high temperature or very small duty cycle; moreover, measurements show that lower biasing voltage can further increase power efficiency but, in this case, a start-up circuit becomes mandatory for reliable operation.

- Closed-loop control - output power control by means of on-off switching was found to effectively modulate the output power without compromising power efficiency; a proper feedback loop exploiting this feature should be included to control the output voltage, thus increasing reliability and functionality of the converter.

- Protection circuitry - due to the peculiar applications of these converters, ruggedness is a key requisite; system robustness must be verified in real-life applications and use-cases and proper protection circuitry should take care of this aspect, if required.

However, most of these open issues have already been dealt with in literature, e.g. several feasible closed-loop control schemes have been developed in the past for fully-integrated dc-dc converters, while protection and start-up circuitry for oscillators are well-known topics of radio-frequency IC design.

Further to the data/power transfer system, fully operation with common-mode voltage transients is the biggest challenge to be addressed: such events are commonly encountered within the target applications of this system. Parasitic coupling between coils is always present and common-mode transients cause common-mode currents to flow through the transformer's terminals. The relatively small size of the isolation transformer helps to reduce these currents. Their exact amount should be measured with a custom experimental set-up and proper common-mode feedback loops should be arranged, if required, to protect sensitive circuitry and preserve the data-communication link. Eventually, the data-detection strategy could be further improved.

Conclusion

Key results demonstrated in this work show that, by using proper architectures and design techniques, power transfer with on-chip galvanic isolation, as well as data/power transfer, are both feasible with current silicon technology. Moreover, measured power-transfer performance is shown to exceed state-of-the-art devices which rely on high-quality passive devices.

Few open issues remain before complete and practical systems are obtained, and they can be dealt with by introducing proper control circuitries, some of them already well-known in literature. Performance is shown to be mainly limited by the technology BEOL and measurements also quantify the incremental performance which can be attained by improving its quality. Specifically, metal thickness defines the resistivity and maximum current of transformer coils, thus affecting the minimum coil's metal width for a given power target. Higher thickness could be exploited to reduce either transformer area, which is proportional to both costs and parasitic capacitance and affects power density, or power losses, thus increasing peak performance and reliability. For example, many already available BEOL such as the ones currently adopted in RF-CMOS or millimeter-wave technologies could immediately

increase the performance and hence desirability of these systems, whose introduction in the mass market could have a serious impact in many industrial and consumer applications.

Acknowledgements

This section is mandatory to thank all those people which did more than their job within the context of my Ph.D. activity.

Firstly I would like to thank Dr. Egidio Ragonese. He definitely did more than its job: most positive outcomes concerning my publications are due to its results-oriented mindset, and, especially, to its incredible patience when dealing with people. The latter is something that is not so common or required in my opinion and hence it is worth to be mentioned.

Then I would like to thank all the people that I had the chance to meet at the RFADC for the fun moments shared during these years: this includes all my Ph.D. colleagues, as well as all the ST employees and the bachelor and master students. I wish all the best for their future. Particularly, I would like to mention Dr. Giorgio Maiellaro and thank him for his valuable advices. A special thank to Dr. Giuseppe Papotto is also necessary, for both his technical and non-technical advices and fruitful discussions: he is for sure the most skilled and professional employee in RFADC.

Finally, a thank to my parents and especially to Veronica is not required here: their role is much more important and not limited to this work, of course.

Appendix A

Simplified expressions for RC-loaded transformers

Simple expressions are derived in this appendix for a qualitative analysis of power efficiency and input impedance of transformer loaded circuits.

The simple linear lumped model in Fig. A.1(a) can be used as a starting point. The transformer is here modeled by coupled inductors, L_P and L_S, with finite coupling factor k and finite series resistances, R_P and R_S. It is loaded by an RC-parallel impedance, $R_{RECT}//C_{RECT}$. An equivalent circuit of Fig. A.1(a) is shown in Fig. A.1(b), where the following identity is exploited:

$$n = \frac{1}{k}\sqrt{\frac{L_S}{L_P}} \tag{A.1}$$

By neglecting the series resistance of the secondary coil, R_S, a first simplified model is obtained that is shown in Fig. A.1(c). For this circuit straightforward calculations lead to the following expressions for the input impedance seen by the current generator, $Z_{IN,TX}$, and transfer efficiency η_{TX_AC}, defined as the output power with respect to the input ac power (Eq. 2.5):

$$Z_{IN,TX} \approx R_P + j\omega(1-k^2)L_P + \left(j\omega k^2 L_P\right) // \left(\frac{R_{EQ}}{(1+j\omega C_{EQ}R_{EQ})}\right), \tag{A.2}$$

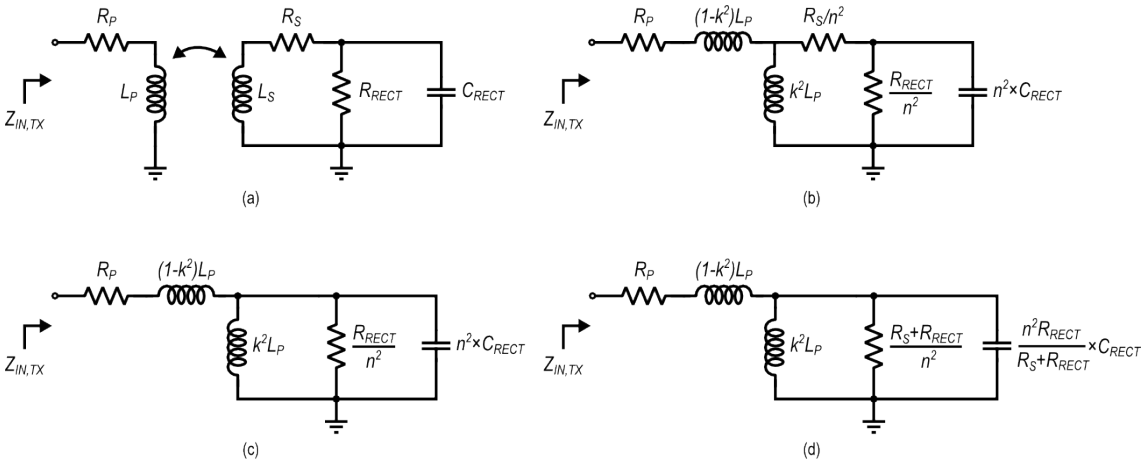


Figure A.1. Linear lumped transformer model: (a) Traditional topology, (b) equivalent representation without coupled inductors, (c) and (d) simplified models.

$$\eta_{TX\_AC} \approx \frac{\omega Q_{EQ} L_{EQ}}{\omega Q_{EQ} L_{EQ}\left(1+\frac{R_P}{R_{EQ}}\right)+R_{EQ}\left(\omega^2 L_{EQ} C_{EQ}-1\right)^2} \tag{A.3}$$

where

$$C_{EQ} = C_{RECT} \times n^2, \tag{A.4}$$

$$R_{EQ} = \frac{R_{RECT}}{n^2}, \tag{A.5}$$

$$L_{EQ} = L_P \times k^2, \tag{A.6}$$

$$Q_{EQ} = \frac{\omega L_{EQ}}{R_P}, \tag{A.7}$$

as shown in the figure. It is also worth nothing that in this circuital form parasitic capacitance at the secondary side of the coils can be easily taken into account since it would appear in parallel with the output capacitance C_{EQ}.

To include the effect of R_S on the network and improve accuracy, an equivalent impedance for the secondary load can be exploited instead. As shown in Fig. A.2, Z_2 shows a good approximation of the impedance Z_1, which is the one loading the secondary coil L_S, from dc up to the high-frequency zero due to R_S and C_{RECT}. By using this substitution the simplified model in Fig. A.1(d) is obtained. In this case

Eq. A.4 and Eq. A.5 become:

$$C_{EQ} = C_{RECT} \times \frac{R_{RECT}}{R_{RECT} + R_S} \times n^2 \text{ and} \tag{A.8}$$

$$R_{EQ} = \frac{R_{RECT} + R_S}{n^2}, \tag{A.9}$$

respectively.

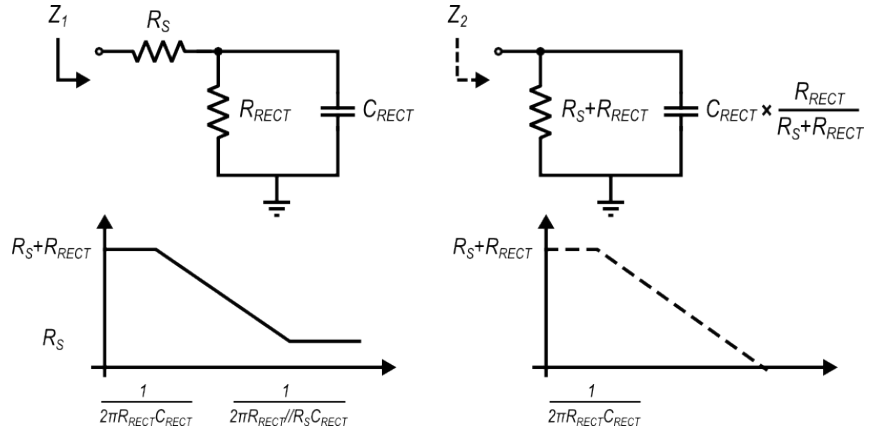


Figure A.2. Modeling of the load impedance.

This model provides a better approximation of $Z_{IN,TX}$ since maintains both dc resistance and the frequency of the first pole and hence reduces the error in calculation of both losses on R_P and transfer efficiency towards R_{EQ}. On the other hand, it distorts the way how the output power delivered to R_{EQ} is split between R_S and R_{RECT}. Since we are interested in the power delivered to the latter, the following correcting factor can be added for transfer efficiency evaluation:

$$\frac{R_{RECT}}{R_{RECT} + R_S} \times \frac{1}{(1 + \omega^2 C_{EQ}^2 R_S R_{RECT})} \tag{A.10}$$

This factor is the analytical description of how output power of the secondary coil L_S splits between R_S and R_{RECT} for the circuit in Fig. A.1(a). Taking this correction into account, the final expression for efficiency is found that is:

$$\eta_{TX\_AC} \approx \frac{\omega Q_{EQ} L_{EQ} \times \frac{R_{RECT}}{R_{RECT}+R_S} \times \frac{1}{(1+\omega^2 C_{EQ}^2 R_S R_{RECT})}}{\omega Q_{EQ} L_{EQ} \left(1 + \frac{R_P}{R_{EQ}}\right) + R_{EQ} \left(\omega^2 L_{EQ} C_{EQ} - 1\right)^2}, \tag{A.11}$$

This expression is simple enough for a qualitative understanding on how R_{RECT} and C_{RECT}, as well as transformer's electrical parameters, affect the transfer efficiency. By the way, it also provides enough accuracy for pen and paper calculations in a wide range of design examples. Figs. A.3 to A.8 show a parametric comparison between actual and calculated values of the transfer efficiency for a wide range of transformer's electrical parameters, as a function of frequency. Calculated values for the variable parameters are identified by markers within each chart, and they are all very close to the correspondingly simulated values at low frequency. Default values for the fixed electrical parameters are $R_P = 2\,\Omega$, $R_S = 8\,\Omega$, $L_P = 6\,\text{nH}$, $L_S = 52\,\text{nH}$, $R_{RECT} = 100\,\Omega$, $C_{RECT} = 7.2\,\text{pF}$, and $k = 0.9$.

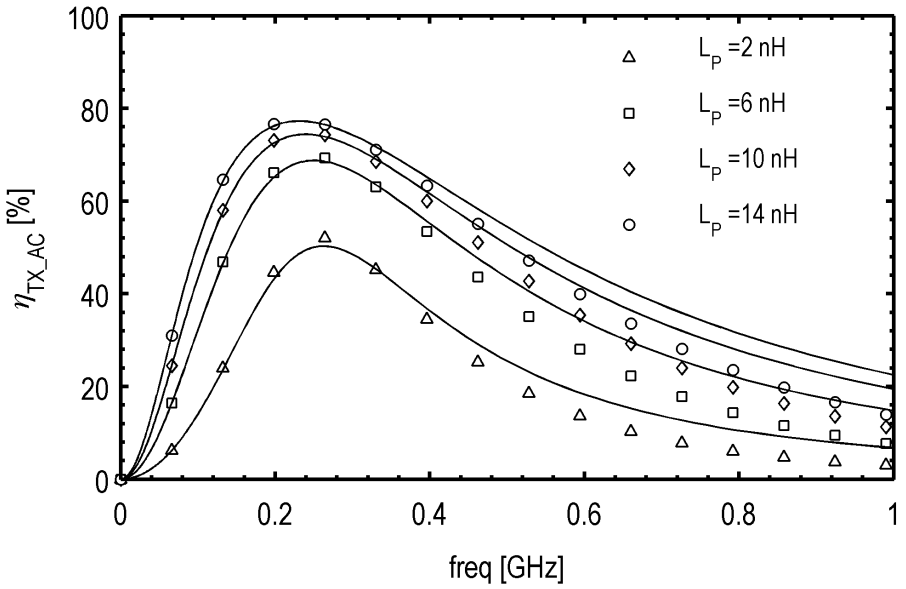


Figure A.3. Comparison between simulated transfer efficiency for the circuit in Fig. A.1(a) and calculated values from Eq. A.11 vs. L_P.

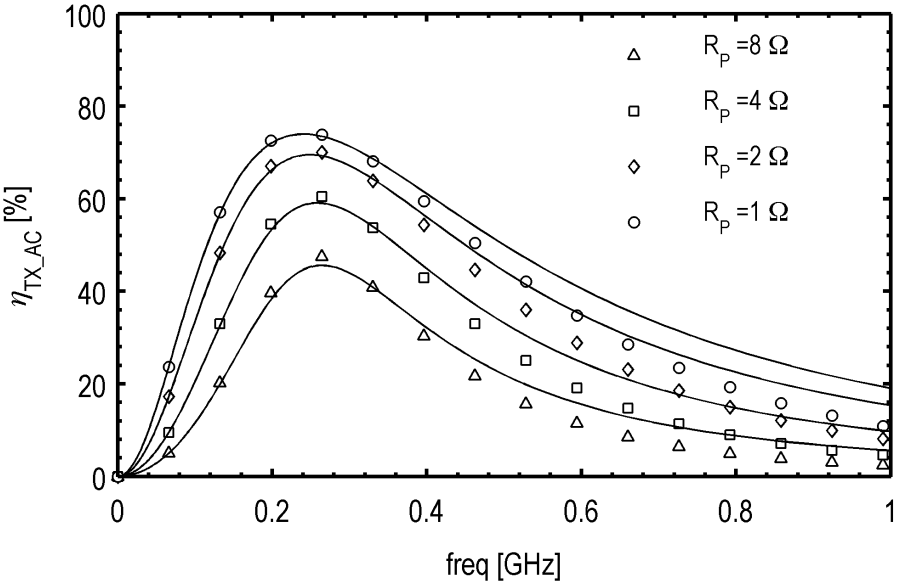


Figure A.4. Comparison between simulated transfer efficiency for the circuit in Fig. A.1(a) and calculated values from Eq. A.11 vs. R_P.

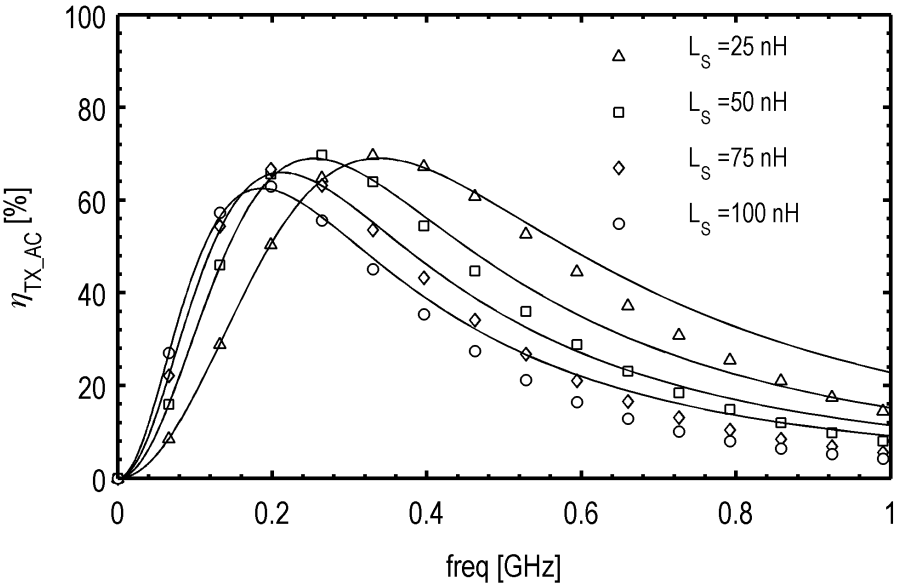


Figure A.5. Comparison between simulated transfer efficiency for the circuit in Fig. A.1(a) and calculated values from Eq. A.11 vs. L_S.

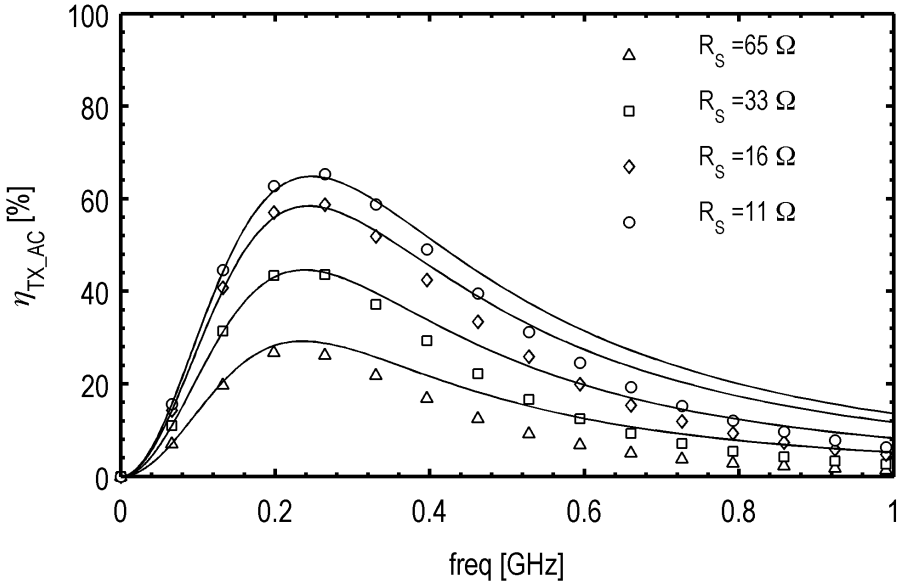


Figure A.6. Comparison between simulated transfer efficiency for the circuit in Fig. A.1(a) and calculated values from Eq. A.11 vs. R_S.

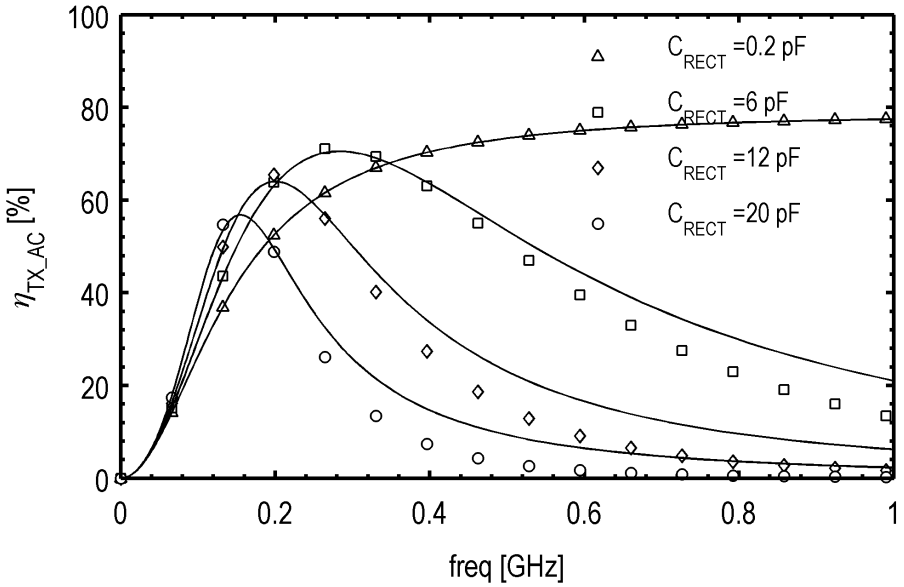


Figure A.7. Comparison between simulated transfer efficiency for the circuit in Fig. A.1(a) and calculated values from Eq. A.11 vs. C_{RECT}.

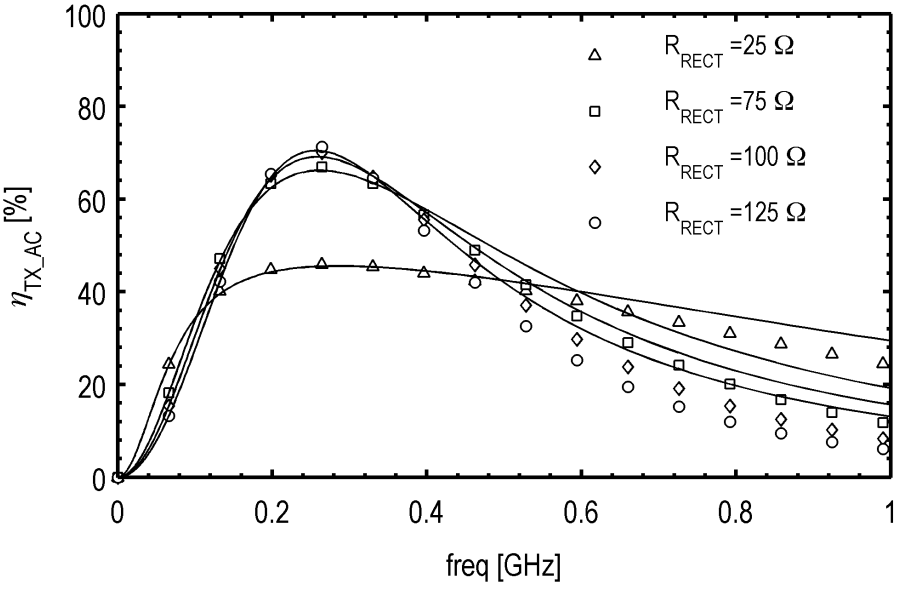


Figure A.8. Comparison between simulated transfer efficiency for the circuit in Fig. A.1(a) and calculated values from Eq. A.11 vs. R_{RECT}.

Appendix B

Circuit topologies and passive device modeling for CMOS-based systems

This appendix focuses on circuit solutions and passive devices modeling to efficiently implement power transfer systems with CMOS topologies.

The first section describes circuit techniques introduced in [67] and demonstrated on silicon in [5] and [19]. Both topologies rely on a three-windings integrated transformer to improve performance with respect to the state of the art and are briefly described.

Within this context, an innovative model for a three-windings transformer with mixed stacked-interleaved configuration was developed for design purposes. It has been successfully validated by means of EM simulations, and profitably used in the design of the converters reported in [5] and [17]. It is briefly discussed in the second section.

B.1 CMOS Topologies for power transfer systems

An important feature to achieve lowest fabrication costs is the compatibility with standard CMOS technologies. However, this constraint further increases the design

complexity of the power oscillator when compared with the simple cross-coupled LC topology described in Chap. 2. To better understand the main design issue of standard CMOS power oscillators, we recall its main features for the sake of clarity: the cross-coupled oscillator achieves high oscillation amplitudes, e.g. the drain voltage can reach two times the supply voltage V_{DD}. Taking into account the differential drain voltage, the oscillation amplitude at primary coils can be higher than $2 \times V_{DD}$, thus reducing the supply current for a given power level at the transformer primary coils. Since integrated implementations suffer from high resistive losses, dealing with low current is preferable if high efficiency is to be achieved. Its inherent simplicity is another distinctive characteristic that entails highest power density compared with other suitable topologies. However, this circuit requires either thick-oxide devices or lateral transistors with high voltage capability to sustain the gate-drain/drain-source voltage achieved, that is higher than the supply voltage. This is in contrast with typical gate-oxide breakdown voltage of standard CMOS devices, which is tailored to the supply voltage of CMOS logic circuitry, i.e. 3-5 V, and does not enable easy and effective operation above the supply voltage. Therefore this topology requires an high-efficiency buck converter to reduce V_{DD} if CMOS devices are to be used [71]. To avoid gate-oxide breakdown and an additional external buck converter, two standard CMOS devices should be stacked between the supply rails to implement the oscillator at least.

Current-Reuse Transformer-Coupled Oscillators

The complementary cross coupled topology in Fig. B.1(a) is a widespread oscillator topology when only standard-oxide CMOS devices are available, being its oscillation level inherently contained within the supply voltage. For small-signal operation it provides higher small-signal transconductance for the same biasing current, due to the double cross-coupled pair. However, for large-signal operation this advantage is

less important, since very high transistor's width are required to provide ac power with high efficiency and transconductance is not a problem. Although the active devices can easily reach the deep triode region to minimize power losses, for power transfer applications the efficiency of this topology is still lower than the standard cross-coupled one, due to lower oscillation level and higher losses in the active devices: indeed, the differential voltage across the primary coil can be around V_{DD} at most, which entails higher currents in the coil for a given power level, and during operation two devices are always stacked for each path between power supply and ground, apart from the primary coil, instead of only one. Therefore, novel transformer-loaded topologies are required to improve performance while avoiding breakdown and properly exploiting the characteristics of integrated transformers at the same time. This aspect is particularly important since passive devices are the bottleneck for both power efficiency and power density in standard technology, as demonstrated in Chap. 2 and well-known in literature [55].

A novel topology which was found to satisfy these requirements is shown in Fig. B.1(b). In this topology, three key techniques are exploited i.e. inductively coupled oscillators, current reuse, and output power combining [67]. The circuit is made up of two LC complementary oscillators, i.e. $M_{1/2}, L_{P1/2}, C_{P1}$, and $M_{3/4}, L_{P3/4}, C_{P2}$, respectively, which are stacked to share the same supply current, and whose tank inductors are magnetically coupled each other, according to the dot scheme depicted in the figure. Inductors $L_{P1/2}$ and $L_{P3/4}$ form the two primary windings of the isolation transformer, T_{ISO}, whereas inductors $L_{S1/2}$ are the secondary winding. If the magnetic coupling coefficient between the primary windings, k_P, is sufficiently high (typically greater than 0.6) frequency synchronization of the two oscillators is achieved [95, 96]. In this configuration the current reuse arrangement, which is easily implemented by means of the center tap of the primary windings, enables two high-efficiency LC cross-coupled oscillators to be stacked without the need of buck converters. The signal produced at each primary winding is then delivered to the

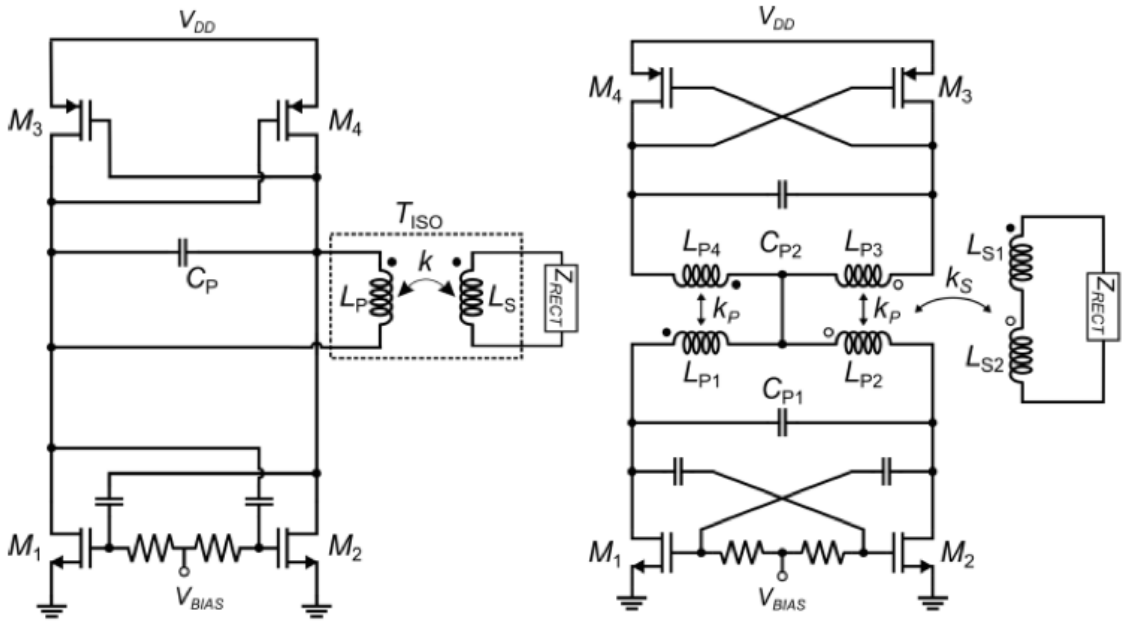


Figure B.1. Transformer-loaded CMOS oscillators with equivalent rectifier impedance load, Z_{RECT}: (a) Complementary cross-coupled oscillator, (b) Current-reuse transformer-coupled oscillator [5] ©2015 IEEE.

secondary winding of T_{ISO}, where power combining is performed.

In [5] the proposed topology was compared with the more traditional complementary cross-coupled oscillator shown in Fig. B.1(a). This comparison highlighted that the proposed topology can provide an increase in both output power and power efficiency higher than 10 % and 40 %, respectively. The comparison was carried out in the same CMOS process, at equal supply voltage and Z_{RECT}, and for the same oscillation frequency. Moreover, the total silicon area was kept constant for both the active core and transformer, which is a key constraint in this context: indeed, the results of the comparison entails that optimum design for this topology can lead to a more efficient use of integrated transformer's implementations.

Current-Reuse Hybrid-Coupled Oscillators

In spite of better performance when compared to the complementary cross-coupled oscillator, the current-reuse transformer-coupled topology, here shown in Fig. B.2(a) for the sake of clarity, still suffers from low power density when compared to the cross-coupled LC oscillator. A fair comparison can be carried out between the implementation in [5] and the one discussed in Chap. 2, which adopts the same BCD technology described in Chap. 1.2: the latter shows around four time higher power density.

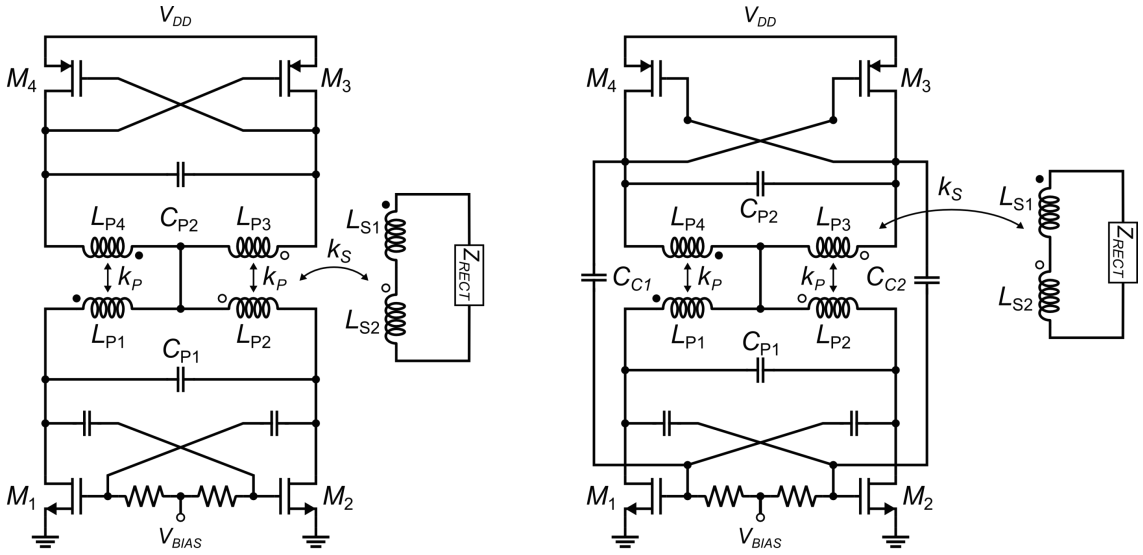


Figure B.2. Transformer-loaded CMOS oscillators with equivalent rectifier impedance load, Z_{RECT}: (a) Current-reuse transformer-coupled oscillator [5], (b) Current-reuse hybrid-coupled oscillator topologies [19] ©2015 IEEE.

To improve this aspect, it is worth noting that the aforementioned need for a good magnetic coupling factor between nMOS and pMOS, k_P in Fig. B.2(a), poses several constraints on the transformer implementation, which accounts for most of the area occupation of the dice. This issue led to the choice of an interleaved configuration for the primary windings (i.e. coils $L_{P1,4}$ and $L_{P2,3}$) in [5], which guarantees both high k_P due to reduced spacing between coils and reduced series

resistance due to the extensive use of metal 3 for the coils. However, interleaved configurations suffer from lower Q-factors and very high area occupation compared to other configurations.

Fig. B.2(b) shows a different circuit configuration which improves this aspect, that was called current-reuse hybrid-coupled oscillator [67, 19]. It exploits again both current-reuse and transformer-based power-combining techniques, however, compared to the transformer-coupled one, an additional coupling between nMOS and pMOS is introduced by capacitors $C_{C1,2}$ to simplify frequency synchronization. These capacitive links reduce the need for high k_P and hence provide more freedom in the choice of transformer configuration and optimization.

An example of implementation is reported in [19], where the primary windings adopt and area-saving tapped configuration. Tapped configuration guarantees better inductance density and Q-factors for the primary coils since minimum metal spacing is used between each inductor turn, however suffers from low coupling factor k_P and hence it could not be used with the transformer-coupled topology. A comparison between [19], [5] and the work in Chap. 2 is shown in Table B.1: thanks to the use of a tapped transformer enabled by the hybrid coupling topology, power density is almost doubled compared to the transformer-coupled topology, although still lower than the cross-coupled one, of course.

Table B.1. Comparison between dc-dc converters fabricated in the same BCD technology adopted in this work.

Oscillator topology	Rectifier topology	P_{OUT} [mW]	η [%]	V_{DD}/V_{OUT} [V]	f_{OSC} [MHz]	Isolation [kV]	Chip no.	Power density [mW/mm²]
LDMOS cross-coupled	Full bridge	710/780	26/28	5/20	165	5	2	76/83
Current-reuse transformer-coupled	Full bridge	200	27	5/8	240	5	2	19
Current-reuse hybrid-coupled	Full bridge	300	24	5/10	225	5	2	36

B.2 Modeling of a three-coils isolation transformer

As discussed in the previous section, the transformer-coupled topology adopted in [5] is based on an a three coils-transformer whose schematic is shown in Fig. B.3. Its physical implementation adopted in that work is shown in Fig. B.4 instead. For the sake of clarity, both planar and 3-D views of primary and secondary windings are depicted.

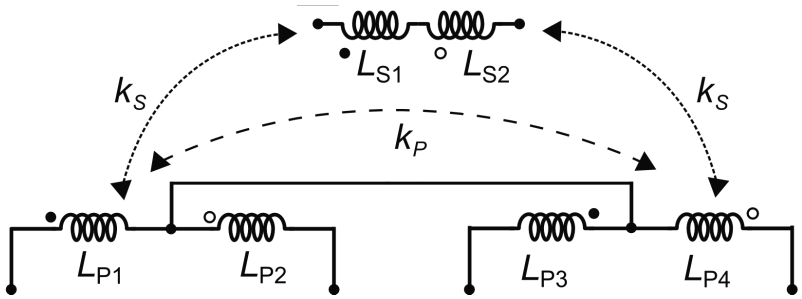


Figure B.3. Isolation transformer schematic ©2015 IEEE.

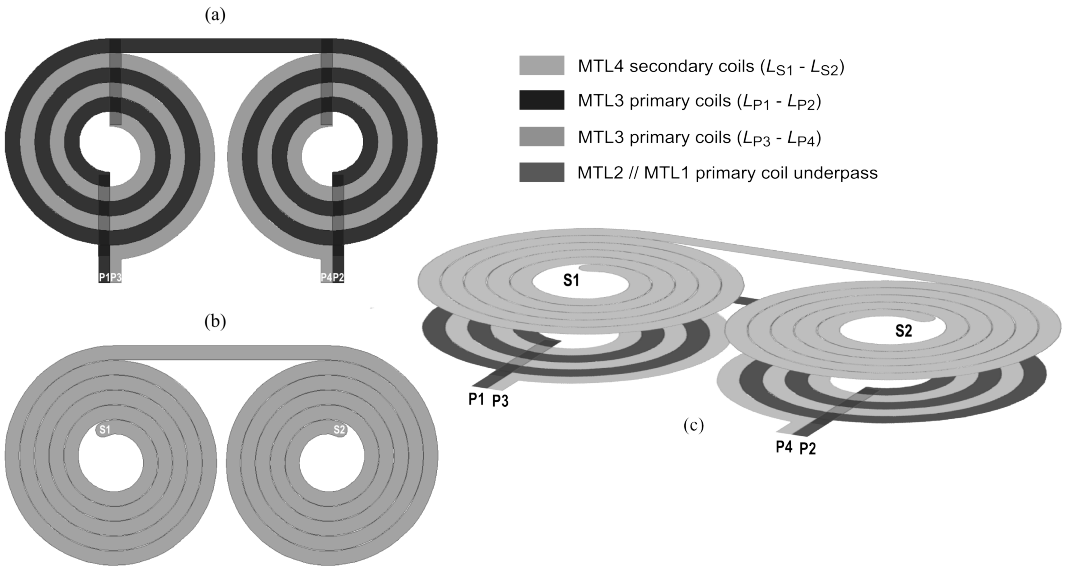


Figure B.4. Isolation transformer: (a) Primary windings, (b) Secondary winding, and (c) 3-D view [5] ©2015 IEEE.

Since adequate magnetic coupling factor is required by the circuit topology, the physical implementation adopts an interleaved configuration between primary windings, whereas the need for galvanic isolation mandates a stacked configuration towards the secondary coil. Specifically, the four inductors of the primary windings, L_{P1-P4}, were arranged as two symmetric interleaved configurations, $L_{P1/3}$ and $L_{P2/4}$, one for each secondary coupled coils (i.e., L_{S1} and L_{S2}), with a common terminal for the center-tap. By using the minimum spacing ($1\,\mu$m) available on the metal 3 for $L_{P1/3}$ and $L_{P2/4}$ magnetic coupling is further maximized. Another advantage of this configuration is its symmetry, which is exploited to simplify design and optimization of the transformer. Underpasses are built in the bottom metal layers and are only used to contact the inductor terminals and the center-tap. They adopt both metal 2 and metal 1 to reduce their series resistance. Finally, the secondary coils, L_{S1} and L_{S2}, are stacked on the primary ones using the top metallization and series connected to build the secondary winding.

The design of this transformer for the converters in [5] and [17] followed a co-design flow similar to the one adopted in Chap. 2. To maximize coupling factor k_S, between primary and secondary windings, which affects the overall system efficiency, it is of utmost importance to equalize the external diameters of the secondary coils L_{S1} (L_{S2}) and the interleaved primary spirals L_{P1}-L_{P3} (L_{P2}-L_{P4}), using geometrical constraints similar to Eq. 2.17. However, being such transformer topology completely different from the work in Chap. 2, and much more complex, a novel lumped, geometrically scalable model was developed for its three winding configuration to speed-up the design flow.

Lumped, geometrically scalable hybrid model.

The schematic of the lumped scalable model developed is shown in Fig. B.5. The displayed network models half structure (i.e., the single-ended configuration) of the

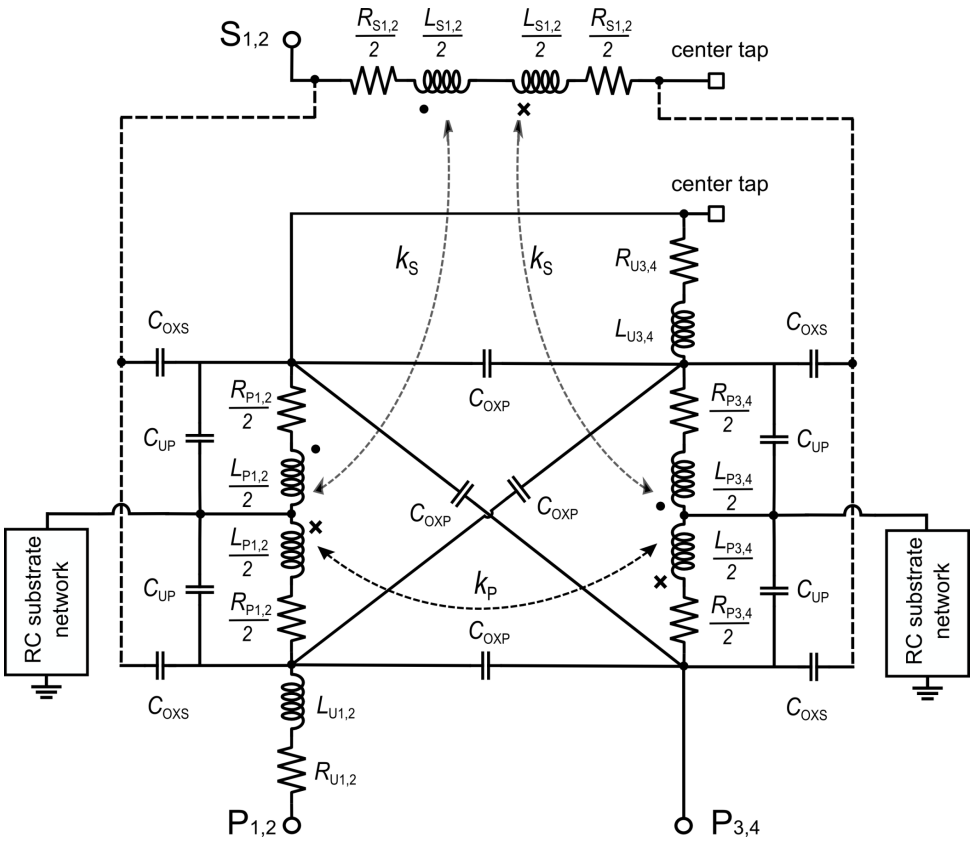


Figure B.5. Lumped scalable model of the isolation transformer (half-structure) [5] ©2015 IEEE.

transformer and consists of two T-like branches, one for each coil of the interleaved primary spirals, and a π-like branch for the stacked secondary coil, respectively. In particular, the primary interleaved spirals $P_{1,2}$ and $P_{3,4}$ are modeled by two T branches (i.e., $L_{P1,2}/2$ and $L_{P3,4}/2$), magnetically coupled through the magnetic factor k_P, while capacitors C_{OXP} take into account the fringing capacitive coupling. The model takes also into account inductive, resistive, and capacitive contributions due to the underpass connections, while, a traditional RC network is included to model the substrate effects [79]. For small transformers the self resonance frequency (SRF) is mainly due to capacitors C_{OXP} and C_{UP} since the oxide layer between primary and secondary windings is very thick. The primary windings $P_{1,3}$ and $P_{2,4}$

are also magnetically and capacitively coupled to the secondary spiral $S_{1,2}$ through the magnetic coupling factor k_S and capacitors C_{OXS}, respectively. Of course, at the increasing of D_{OUT}, primary to secondary winding capacitors C_{OXS} become more important and were included to model this effect.

The scalability of the model is crucial for its employment into the co-design procedure. Low-frequency inductance values (i.e., $L_{P1/2}$, $L_{P3/4}$, $L_{S1/2}$) are obtained by means of monomial equations [76], whose coefficients were determined by least square fitting to EM simulated data. Underpass inductance, L_{UP}, is instead calculated with the well known expression for a rectangular conductor [97]. Capacitor contributions arise from both area (i.e., C_{OXS} and C_{UP}) and perimeter (C_{OXP}) effects and are easily calculated using the expressions for a parallel plate capacitor [70, 79, 98]. The frequency dependent resistances, $R_{P1/2}$ and $R_{S1/2}$, which model the current crowding phenomena on the spirals, adopt the same novel expression reported in Eq. 2.15. Finally, magnetic coupling variations are modeled by means of two monomial expressions for both k_P and k_S, whose coefficients were determined by least square fitting to EM simulated data [70].

A distinctive feature of this model is the use of T-like branches, which was found to provide a better approximation of the frequency behavior of the interleaved transformer compared to traditional *pi*-like topologies.. Model accuracy was verified by using EM simulated data of geometrically scaled transformers drawn according to the configuration of Fig. B.4 (primary: n from 2.5 to 3.5, w from 70 to 130 μm, D_{IN} from 350 to 550 μm; secondary: n from 5 to 7, w from 70 to 130 μm, D_{IN} from 350 to 450 μm). Fig. B.6 depicts the error distributions on low-frequency inductance, maximum Q-factor, SRF and magnetic coupling factors, k_P and k_S, for 24 transformers, which are well below 10%. These results confirmed the soundness of the model that was hence profitably exploited to design the transformer adopted in [5]. The same model was also exploited for the power link in [17], by the way with different fitting parameters, properly customized to the small area target of

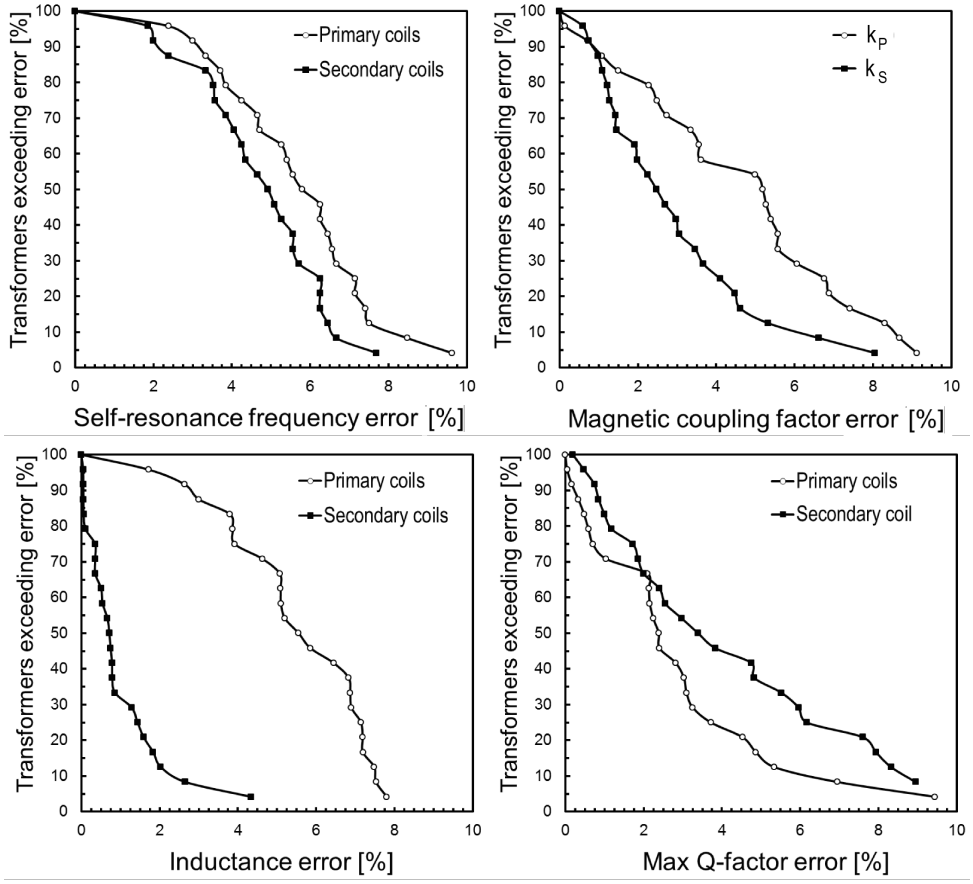


Figure B.6. Error distributions of the lumped scalable model of the isolation transformer calculated with respect to EM simulations [5] ©2015 IEEE.

that system.

Measurement results

A test-chip was integrated containing the transformer adopted in [5], to check the reliability of both EM sims and model results for the final design, whose geometrical parameters are shown in Table B.2. A micrograph of the transformer with highlighted ports for testing is shown in Fig. B.7. The S-parameters of this transformer were measured on-wafer for five different samples from the same lot by means of a Cascade Microtech probe station and an HP8155 network analyzer.

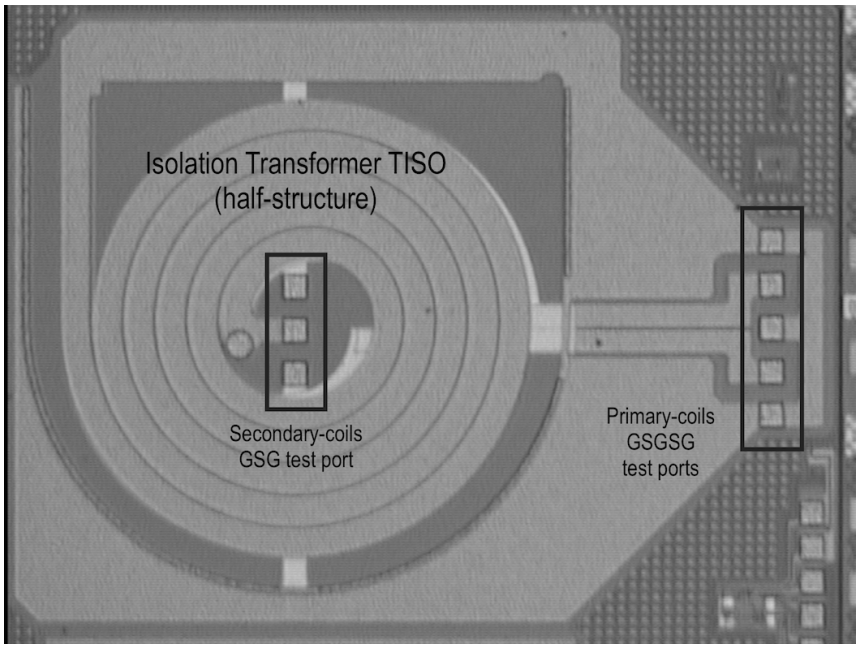


Figure B.7. Test-chip structure for the three-coils transformer adopted in [5].

Table B.2. Geometrical parameters of the transformer in Fig. B.2 [5] .

Parameters	Primary coils	Secondary coils
Number of turns (n)	2.5	5
Width (w) [μm]	110	106
Spacing (s) [μm]	112	5
Inner diameter (d_{IN}) [μm]	460	431
External diameter (d_{OUT}) [μm]	1680	1640

Fig. B.8 compares (single-ended) performance of the adopted isolation transformer estimated by the developed lumped model, simulated with a $2D$ EM tool, and measured on-wafer. Main discrepancies with measured performance are related to the SRF and are mainly due to inaccuracy in the parasitic de-embedding [99], which were not integrated in the test-chip due to area constraints. It is worth noting

the excellent agreement between the model and measured/simulated curves in the useful range of frequencies (i.e., below the SRF), which further validates its utility.

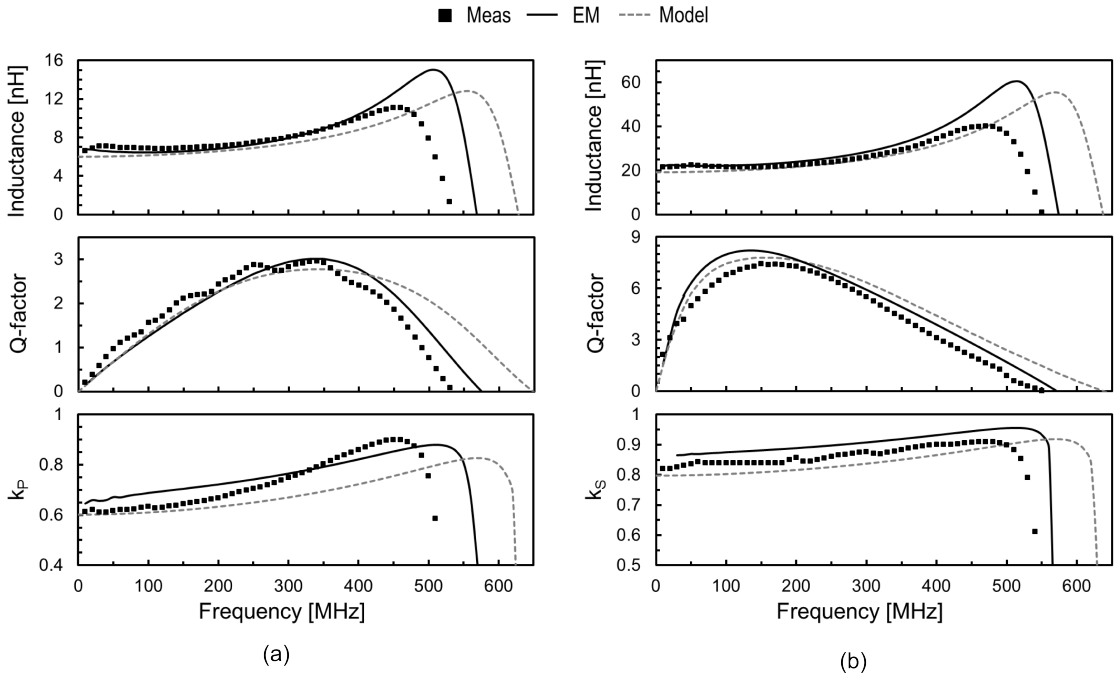


Figure B.8. Three windings transformer's main parameters - measurements vs. simulation and model: (a) Primary coil. (b) Secondary coil [5] ©2015 IEEE.

Appendix C

Publications

Patents

1. E. Ragonese, V. Fiore, N. Spina, and G. Palmisano, "Power oscillator apparatus with transformer-based power combining," Italian Patent App. MI2013A 000454, filed Mar. 2013.

2. E. Ragonese, V. Fiore, N. Spina, and G. Palmisano, "Power oscillator apparatus with transformer-based power combining," US Patent App. 14/216037, filed Mar. 2014.

3. E. Ragonese, V. Fiore, N. Spina, P. Lombardo, G. Palmisano, "Power oscillator apparatus with transformer-based power combining for galvanically-isolated bidirectional data communication and power transfer," US Patent App. 14/631397, filed Feb. 2015.

International Conferences

1. V. Fiore et al., "A 13.56MHz RFID Tag with Active Envelope Detection in an Organic Complementary TFT technology," in Solid-State Circuits Conference

Digest of Technical Papers (ISSCC), 2014 IEEE International , San Francisco, 2014, pp. 492-493.

2. P. Lombardo, V. Fiore, E. Ragonese, G. Palmisano, "A Fully-Integrated Half-Duplex Data/Power Transfer System with up to 40Mbps data rate, 23mW Output Power and On-Chip 5kV Galvanic Isolation," accepted in International Solid State Circuit Conference (ISSCC) 2015.

Peer-reviewed Journals

1. V. Fiore et al., "An Integrated 13.56-MHz RFID Tag in a Printed Organic Complementary TFT Technology on Flexible Substrate," in Transactions on Circuits and Systems I, vol. 62, pp. 1668-1677, June 2015.

2. N. Spina, V. Fiore, P. Lombardo, E. Ragonese, G. Palmisano, "Current-Reuse Transformer-Coupled Oscillators with Output Power Combining for Galvanically Isolated Power Transfer Systems," accepted in Transactions on Circuits and Systems I, to be published.

3. V. Fiore, E. Ragonese, G. Palmisano, "Low-Power ASK Detector for Low Modulation Indexes and Rail-to-Rail Input Range," accepted in Transactions on Circuits and Systems II, to be published.

4. V. Fiore, E. Ragonese, G. Palmisano, "A Fully-Integrated Watt-Level DC-DC Converter with On-Chip Galvanic Isolation," submitted to Transactions on Power Electronics.

5. N. Greco, V. Fiore, E. Ragonese, and G. Palmisano, "A Galvanically Isolated DC-DC Converter Based on Current-Reuse Hybrid-Coupled Oscillators," submitted to Transactions on Circuits and Systems II.

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