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Transport properties at 3*C*-SiC interfaces

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Introduction

For years it has been unclear what should be the definition of an interface in materials science. For a long time it was seen simply as the intermediate layer between two bulk materials. Interface properties were deduced by theory starting from known macroscopic material properties. To date, many materials science aspects concerning interfaces in electronic devices are unresolved, and the macroscopic performances cannot be precisely predicted from the known bulk properties of the individual constituents.

In this context, nanoscience will play a key role in accessing new groundbreaking knowledge and bringing forth emerging technologies. It seems that nanoscience is the future of science but even more the science for the future. In particular, the equipments and methodologies recently implemented allow us to change the way to approach materials science and provide new means for tuning device performances. Interface properties can now be studied at nanoscale, i.e. atomic thicknesses can be resolved.

One of the fascinating physical aspects that can be investigated at nanoscale is the properties of electronic device interfaces in cubic (3*C*) silicon carbide (SiC). For years this material has been believed to be a very promising wide bandgap semiconductor for power electronics, due to its predicted properties. Among the large number of SiC polytypes, 3*C*-SiC (or β-SiC) is the only cubic form. This polytype has several potential advantages over the more mature and better studied hexagonal α-SiC (4*H* and 6*H*), such as higher electron mobility and better stability under electrical stress. These properties make it a strong candidate material for high frequency and high power applications. However, in spite of prolonged efforts, the predicted performances have not been achieved at a macroscopic level, and thus exploiting the potential advantages of this material remains an elusive task. The aim of this thesis is to understand and overcome some of the challenges faced for device fabrication in this material, by studying the nanoscale transport properties at 3*C*-SiC interfaces. In this way, the non-ideal macroscopic behavior of fabricated devices can be better understood and ultimately improved.

3*C*-SiC epilayers are most commonly grown on silicon substrates, due to the availability of cheap production over large area wafers. However, the growth of 3*C*-

SiC on Si is complicated due to the huge lattice mismatch and thermal expansion coefficient mismatch. Recent developments in epitaxial growth have demonstrated the possibility of forming heterojunction structures by growing cubic SiC on top of hexagonal SiC substrates, enabling interesting possibilities for applications, such as devices based on a two-dimensional electron gas (2DEG) that can be formed at the heterointerface, or dual wavelength optoelectronic devices that are based only on the different stacking sequences of pure SiC. Moreover, 3*C*-SiC grown on hexagonal SiC substrates can have superior properties due to the next to non-existent lattice mismatch (less than 0.1 % in the growth plane). However, a special twin boundary defect called double positioning boundary (DPB) is usually observed for β-α SiC heteroepitaxy, coming from the two possible orientations of the cubic β-SiC axis on the hexagonal α-SiC basis. It has been shown that this type of defect can be suppressed by using a vapor-liquid-solid (VLS) mechanism to grow the heteroepitaxial 3*C*-SiC. This type of 3*C*-SiC can then be used as the seed for subsequent homoepitaxial growth, which is the basis for most samples discussed in this thesis.

The present thesis has been done in the framework of the MANSiC research and training network funded by the European Commission within the Sixth Framework Programme. The MANSiC project was a four-year partnership (2007-2010) between nine academic institutions and two companies spread across Europe. The scientific aim of this project was to implement a knowledge based approach to develop technology based on high quality 3*C*-SiC thin films or bulk material grown by members of the consortium. The knowledge based approach, trough the involvement of academic research and advanced education, was necessary to find new ideas and competences in order to break the static development in the field. The goal was then to determine many of the material properties of this polytype, for which the database is still incomplete. The project was divided into 3 interdependent scientific work-packages, devoted to material growth, characterization and realization of new devices and innovative demonstrators.

In spite of recent progresses accomplished in material growth, the cubic polytype is still fraught with large concentrations of various defects, which have so far hindered the achievement of the predicted electrical properties in this polytype. As an example, the surface morphology of 3*C*-SiC is usually characterized by large steps, while triangular pits and large concentrations of stacking faults are also present in the material. These defects have properties that are inherently nanoscale and that will have a strong influence on the electrical behavior of the material, particularly at interfaces commonly found in electronic devices, e.g. metal-semiconductor contacts (Ohmic and Schottky), *p*-type-*n*-type (*p*-*n* junctions) or dielectric-semiconductor interfaces, found e.g. in a metal-oxide-semiconductor field effect transistors (MOSFET). Understanding the behavior of non-idealities at such interfaces will be crucial in order to predict the macroscale behavior of potential devices. To this end, characterization approaches that are able to distinguish morphological, electrical and structural features at the nanoscale are essential.

In this thesis, various experimental approaches were employed and new methodologies were implemented to study structural imperfections and the nanoscale transport properties at 3*C*-SiC interfaces. The material was mainly provided by the project partners. The topics include the major concerns related to the electronic transport at metal/SiC interfaces and the non ideal behavior in metal/oxide/SiC systems. Characterization techniques ranging from optical, to structural, morphological and electrical were employed in this work. Most attention will be given to scanning probe microscopy (SPM) based methodologies, able to physically probe the sample and image tip-sample interactions of morphological and electrical nature at the nanoscale. Experimental approaches employing atomic force microscopy (AFM), conductive AFM (C-AFM), and scanning capacitance microscopy (SCM) modules have been employed to study various interfaces necessary to realize structures for electronic devices.

The results that have come out of this thesis can of course also be extended to a broader and more general area of interest. Indeed, in spite of the significant progress achieved in the last decade in hexagonal SiC material quality, there are still several scientific open issues related to the basic transport properties at SiC interfaces that can affect the device performance, keeping them from reaching their theoretical limits. The practical difficulties concerning SiC are largely related to limitations on the area of the devices, in turn imposed by the existence of structural defects that are formed during the growth process. Significant efforts in fundamental research at the nanoscale are essential to better understand the carrier transport phenomena, both at surfaces and interfaces. In that sense, the findings of this study can be of interest to the community of experimentalists working with SiC in the field of electronic devices.

The dissertation is divided into four main chapters.

In chapter 1, a general introduction to silicon carbide is presented, providing an overview of the properties of SiC as a wide bandgap semiconductor for power electronic devices. The crystal structure and the formation and properties of different polytypes are discussed, alongside crystal growth and the state of the art of SiC power devices. While 4*H*-SiC is the benchmark material for the wide bandgap scientific community, the focus is maintained on new explorations. Then the topic of investigation in this thesis is motivated, outlining the potential advantages of cubic SiC and the possibilities to fabricate novel devices in β-α SiC heterostructures. The problems faced in SiC technology development are mostly related to material defects, and this particular issue is more pressing for the cubic polytype, where the material maturity is lower. Therefore, the chapter concludes by comparing the prominent types of defects present in hexagonal and cubic SiC.

Chapter 2 discusses Ohmic contacts to 3*C*-SiC. Ohmic contacts play a very important role in the signal transfer between the semiconductor and the external circuitry. A contact resistance that is significant compared to that of the bulk of the device will lead to a voltage drop at the contact interface, in turn resulting in decreased efficiency due to added resistive losses.

Previous findings concerning Ohmic contacts to 3*C*-SiC have shown a great spread in the specific contact resistance values, pertaining to the difficulty to control the material quality. The behavior of an Ohmic contact can be directly correlated to the crystalline quality of the contacted material, and it is therefore of exceptional interest to study the properties of Ohmic contacts to the high quality, single crystalline 3*C*-SiC material achieved by heteroepitaxial growth onto α-SiC substrates. To this end, and in order to have the widest possible comparison to literature findings, the Ohmic behavior of the Ni/3*C*-SiC system was studied upon high temperature annealing. Indeed, comparatively low values of the specific contact resistance were measured on contacts to single-domain 3*C*-SiC films grown onto α-SiC substrates by the VLS technique, hinting towards very high crystal quality.

A gradual improvement in the structural uniformity of the contact interface with increasing annealing temperature up to 950°C was observed by X-ray diffraction (XRD). It was found that nickel silicide phase formation commences at annealing temperatures above 600°C, where Ni_5Si_2 and Ni_2Si coexist upon annealing at 750°C and 850°C. After annealing at 950°C, only Ni_2Si, which is the most thermodynamically stable phase in this temperature range, was detected. Also an increased presence of carbon was observed with increasing annealing temperature.

Indeed, the mechanism of Ohmic contact formation in Ni/SiC systems upon annealing is normally attributed to the formation of carbon clusters inside the silicide, leaving vacancies in the semiconductor which act as electron donors for SiC, thereby increasing the tunneling current. However, coupling conventional electrical techniques with C-AFM current spectroscopy and current mapping allowed the visualization of a new aspect concerning Ni-based Ohmic contacts to SiC. Specifically, an increased uniformity of the nanoscale current distribution on the contacts was observed with increasing annealing temperature, indicating that an increase of the effective contact area contributes to the improvement of the contact properties normally observed after high temperature annealing of Ni/SiC.

Chapter 3 addresses one of the biggest problems for device fabrication in 3*C*-SiC, i.e. the difficulty to achieve good rectifying contacts, with acceptable blocking behavior. This problem has been attributed to electrically active defects in the 3*C*-SiC epilayers and at the heterointerfaces. Therefore, the electrical activity of defects at 3*C*-SiC surfaces and how they affect metal/3*C*-SiC Schottky (rectifying) interfaces is the main topic of the chapter. The structure and morphology of various defects present at β-SiC/α-SiC interfaces and in the cubic epilayer were studied by AFM and transmission electron microscopy (TEM). The nanoscale electrical behavior of various defects at the contact interface and the behavior of fabricated Schottky diodes were studied by local current mapping and current-spectroscopy using C-AFM. This allowed visualization of the electrical activity of defects and their role in the electrical behavior of the material from the nanoscale to the device level.

Surface preparations and interface reactions were found to be key issues for the formation of good rectifying contacts to 3*C*-SiC. In particular, the electrical activity of the most pervasive extended defect in 3*C*-SiC, the stacking fault, can be suppressed at the (111) surface by an ultraviolet (UV) irradiation. It was demonstrated that the physical mechanism behind the passivation can be related to an oxidation/healing reaction occurring locally at these defects due to their local polarity inversion with respect to the non-polar (111) surface. The passivation led to an overall improvement in the electrical properties of fabricated diodes, showing strong reductions in the leakage currents and increased Schottky barrier heights. Indeed, combining the passivation of the stacking faults with characterization of very small diodes allowed demonstrating the possibility of fabricating almost ideal Au/3*C*-SiC Schottky diodes. The dependence of the Schottky barrier height on the diode area found for Au contacts could be theoretically modeled as leakage currents due to electrically active point-like defects. Further improvements were observed upon a thermal reaction between Pt and SiC that consumed a thin layer of SiC to create platinum silicide, thereby generating a “fresh” interface, away from the original SiC surface.

Due to its intrinsic material properties, 3*C*-SiC is a promising material for high-frequency MOSFETs. In this context, the possibility to easily grow SiO_2 by thermal annealing in an oxygen ambiance gives SiC a great advantage over competing compound semiconductors. However, MOSFETs fabricated in α-SiC suffer from low inversion channel mobilities, caused by a large density of interface traps that are energetically located near the conduction band edge in hexagonal SiC. Due to the lower bandgap, these traps occupy states well inside the conduction band in the cubic polytype, where they do not affect the channel mobility. Indeed, MOSFETs with excellent on-state characteristics have been demonstrated in 3*C*-SiC. The challenges for MOSFET fabrication in this material are instead related to poor off-state characteristics and premature oxide breakdown.

Chapter 4 presents an investigation of the SiO_2/3*C*-SiC interface, where the causes of the often observed premature breakdown in MOS structures were studied by electrically stressing the system using C-AFM to perform localized time-dependent dielectric breakdown measurements on ‘nano-MOS’ capacitors formed at each tip position. Such an experimental approach allows direct observation of dielectric failure as a function of stress time, which can then be related to the simultaneously acquired surface morphology, all determined with nanoscale lateral resolution. A strong correlation was found between the oxide reliability and the 3*C*-SiC surface roughness prior to oxidation. Premature breakdown was found to occur preferentially near step-bunching edges, which was attributed to a local electric field concentration on top of these defects due to the abrupt change in height. A combination of capacitance-voltage measurements and scanning capacitance spectroscopy (SCS) characterization showed that premature breakdown not caused by structural defects at the oxide-semiconductor interface can be attributed to electron injection into traps while the SiO_2/3*C*-SiC system is kept in accumulation.

At the end of the thesis, the scientific open points overcome in this work are summarized, reporting also which new issues that have been raised along the road. An outlook for β-α SiC heterostructures and interesting possible future investigations are also discussed.

Chapter 1

Introduction to silicon carbide

Silicon carbide (SiC) is a wide bandgap semiconductor with properties that are highly suitable for devices working at high-power, high-frequency, high-temperature, and in harsh environments, with superior performances compared to silicon-based devices. This well-tried opening is found in many papers on the topic of SiC. Still, it cannot be omitted, since it highlights the material's potential and the reason it has been a topic of intense study for several decades. SiC is a material with high breakdown electric field strength, high saturated drift velocity of electrons, and a high thermal conductivity. Moreover, SiC has a great advantage over competing compound semiconductors in the fact that, like silicon (Si), it has silicon dioxide (SiO_2) as its native oxide. This is a key element to any semiconductor technology, both concerning processing and device applications. For example, it opens up great possibilities for device applications utilizing a metal-oxide-semiconductor (MOS) structure. Therefore, these properties make SiC ideally suited for a vast number of applications. In this chapter, more details of the promising properties as well as the material's challenges will be discussed. Indeed, the unique properties that have attracted so much attention to SiC also make it a challenge to manufacture and process into working devices.

The main application for SiC crystals is in power electronics. Silicon is the material currently dominating the electronics industry. However, the demand for improved energy efficiency in power electronics, which can be satisfied by reducing the switching and conduction losses of devices, as well as devices capable of high temperature operation, is pushing for the power electronics technology development in wide bandgap semiconductors. In this context, SiC has been touted as a top candidate for decades. Recently, the development of modern epitaxial techniques has led to a rapid improvement in the material quality of SiC, thus leading to a constant increase in the performances of SiC based devices.

In this way, the material is slowly moving on from being perpetually "promising", to becoming a reality for the cutting edge power applications of today and in the future.

Compared with their silicon counterparts, electronic devices fabricated in SiC enable a significant reduction of the electrical losses, as well as of the sizes and weights of the electronics modules, with ensuing improvements in efficiency and cost.

The potential applications of SiC-based electronic devices nowadays include aerospace (high temperature engines, radiation hard devices), transportation (power supply, power switching and power module) as well as industry (power supply), communications (radio frequency (RF) switching) and renewable energies (e.g., power conversion in solar and photovoltaic plants).

The advantages of SiC over Si based power devices can be summarized as follows:

- SiC unipolar devices are thinner, and they have lower on-resistances, which results in lower conduction losses and higher overall efficiency.
- SiC based power devices have higher breakdown voltages because of their higher critical breakdown electric field.
- SiC has higher thermal conductivity (4.9 W/cm-K for SiC and 1.5 W/cm-K for Si), meaning that SiC power devices have a lower thermal resistance and the device heating rate is slower, also enabling size reduction in the cooling systems of power applications.
- SiC can operate at higher temperatures (up to 1000°C compared to 150°C for Si).
- SiC is extremely radiation hard and therefore suited for aerospace applications, by decreasing the additional weight from radiation shielding.
- Because of low switching losses, SiC based devices can operate at high frequencies (> 20 kHz) which is not possible with Si based devices in power levels above a few kilowatts.

1.1 Historical background

Silicon carbide (SiC) is a solid compound made of 50% carbon and 50% silicon. Naturally occurring SiC is also known as “moissanite”, after the French researcher Dr. Henri Moissan who first identified it in 1905 [1]. It is found only in minute quantities in exceptional geological places like kimberlitic volcanic openings and in certain types of meteorite. Virtually all of the silicon carbide sold in the world is synthetic. The first to synthesize SiC was Jöns Jacob Berzelius in 1824 [2]. Berzelius was born just outside of Linköping in Sweden, which is peculiar considering that the center of SiC research in Sweden is at the University of Linköping. However, at that time the properties of SiC were not understood. The interest in SiC did not rise until the invention of the electric smelting furnace by Eugene and Alfred Cowles [3], and Acheson's adoption of this furnace to produce carbonaceous compounds to substitute diamond as an abrasive and cutting material [4]. The crystalline products Acheson found after the process were characterized by a great hardness, refractabiliy and infusibility. He called the product "carborundum" and described it as a carbon silicide with the chemical formula SiC. Shortly afterwards the electronic properties of SiC started to be investigated. The first light emitting diode (LED) was made from SiC in 1907 [5]. In 1955, Lely presented a new concept of growing high quality crystals. The research in SiC became more intensified after this and the first SiC conference was held in Boston in 1958. However, the success and rapid increase of the Si technology caused the interest in SiC to drop, and the SiC research activities in the 1960's to the late 1970's were scarce. The next big break came in 1978, with the invention of the seeded sublimation growth by Tairov and Tsvetkov [6] that led to the birth of SiC wafer growth. By introducing a seed crystal and forcing material transport from the source to the seed by a thermal gradient, the growth rates could be increased and seeds of larger diameters and lengths could be made. The produced boules could be sliced and polished into wafers.

In 1987, another breakthrough came with the "step-controlled epitaxy" on off-axis substrates [7], which meant that high quality epitaxy could be conducted at low temperatures. In light of this milestone, Cree Research was founded in 1989 and became the first company sell SiC wafers, and Cree has remained the biggest player to this day when it comes to SiC substrates. This was the beginning of a wave of interest for SiC that is yet to subside.

In 2001, Infineon launched its Schottky diode product line made from SiC (currently in the 5th generation) and Cree also has Schottky diode as well as high-frequency MESFETs on the market. The SiC Schottky diode market was worth an estimated $29 million in 2009, with market revenues estimated to be 25% higher than the previous year. Moreover, limitations of the Si technology and the III/V technology have further increased the interest in SiC and at present the field is growing rapidly much owing to the recent commercial availability of substrates. In August 2010, CREE announced 6" 4*H*-SiC wafers. Improved epitaxy, continuously growing wafer diameters and improved material quality, coupled with milestones in devices, ensures that the currently large interest will remain.

1.2 Crystal structure

1.2.1 Basic building block

Silicon carbide is a binary compound, tetrahedrally bonded and made up by Si and C atoms (both group IV element materials) in a 1:1 ratio [8,9]. Each Si atom shares electrons with four C atoms, so that each atom is 88% covalently and 12% ionically bonded to four nearest neighbors. The approximate distances between Si-C and Si-Si or C-C atoms are 1.89 Å and 3.08 Å, respectively. The basic building block of a silicon carbide crystal is the tetrahedron of four silicon atoms with a carbon atom in the center. The SiC tetrahedron is schematically illustrated in Fig. 1.

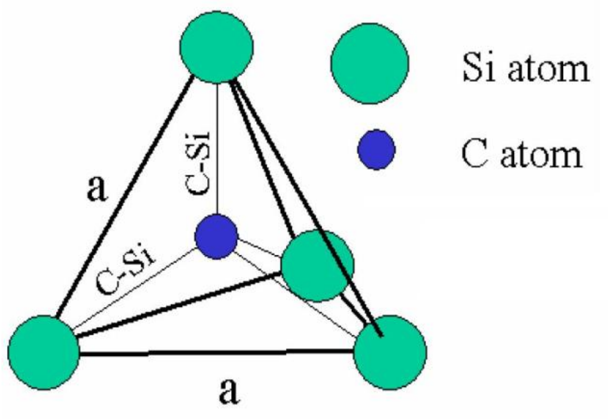


Figure 1. Tetragonal bonding of a central carbon atom with the four nearest silicon neighbors. Two types of tetrahedrons can nucleate, where one is rotated 180° around the *c*-axis with respect to the other.

1.2.2 Polytypism

In general, the phenomenon of the same material crystallizing in different modifications is called polymorphism. The existence of different crystalline modifications of SiC was discovered in 1912 [10]. However, since SiC exhibits a particular two-dimensional polymorphism, the different SiC modifications were later named *polytypes* [11]. The various polytypes, which can exist in cubic (C), hexagonal (H), and rhombohedral (R) crystal structures, share the same chemical composition but exhibit different electrical properties.

All the known polytypes of silicon carbide crystallize according to the laws of close spherical packing, resulting in binary structures constituted by identical layers. All polytypes have a hexagonal frame of SiC bilayers. Viewed as layers of spheres of the same radius, the hexagonal frame takes on the shape in Fig. 2. The SiC bilayers are the same for all lattice planes. However, the relative positions of the adjacent planes are slightly shifted to fill the ‘voids’ in the adjacent layer in a close-packed arrangement. Then, as seen in Fig. 2, there are three possible inequivalent positions for the spheres. Referring to the possible positions as A, B, and C, the different polytypes can be built by organizing the repetitive stacking sequence. Thus, e.g. the only cubic polytype in SiC, called 3*C*-SiC, has the stacking sequence ABCAB. The simplest hexagonal structure, called 2H-SiC, has the sequence ABA. The two important hexagonal polytypes, 6*H*-SiC and 4*H*-SiC, take on the sequences ABCACBABCACB, and ABCBABCB, respectively. The number in the notation refers to the number of layers before the sequence repeats itself [12].

These structures differ both in the order in which cubic (C) and hexagonal (H) layers are arranged and in the number of these layers in a unit cell. What determines the polytype is the sequencing order of the Si-C tetrahedron during the stacking of the Si-C bilayers (see Fig. 1 and Fig. 2).

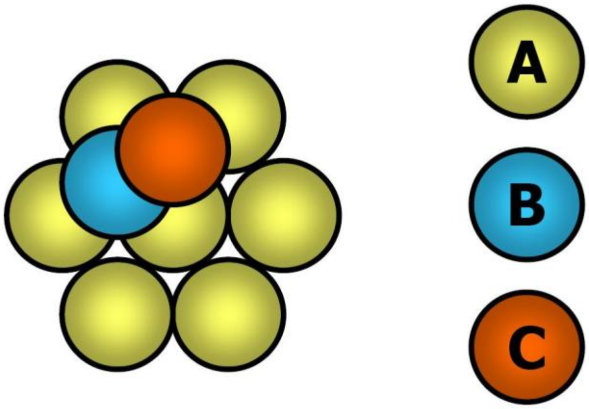
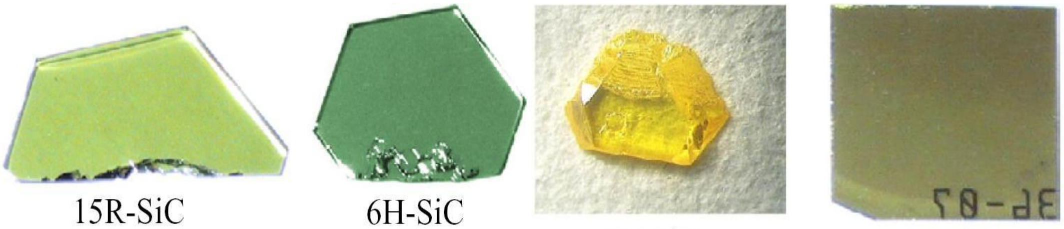


Figure 2. Schematic positions of atom centers for a close spherical packing. Only three possible positions exist for the SiC tetrahedron centers—A, B and C.

Fig. 2 shows schematically the positions of the SiC tetrahedron centers for a close spherical packing. If in the first layer the centers of all the spheres lie at points A, in the second layer positions of centers at points B or C are possible. If in the layer centers of all the spheres lie at points B, in the next layer positions of centers at points A or C are possible. If in the layer centers of all the spheres lie at points C, in the next layer positions of centers at points A or B are possible. In such a way the positions, which are occupied by atoms in the second and subsequent layers, determine the structure of a polytype. In other words, for each polytype the structure will simply correspond to the letters' sequence AB, ABC, ABCB, etc. Polytypes are also frequently characterized by Ramsdell designations [13], constituted by a natural number, equal to the number of layers in the period in the direction perpendicular to the basal plane, and a letter symbol characterizing the crystal system of the Bravais lattice: C, cubic; H, hexagonal; R, rhombohedral. The most frequently occurring are 6*H*, 4*H*, 15R and 3*C* polytypes (see optical images in Fig. 3).



15R-SiC 6H-SiC 3C-SiC 4H-SiC

Figure 3. Optical images of the four most common SiC polytypes.

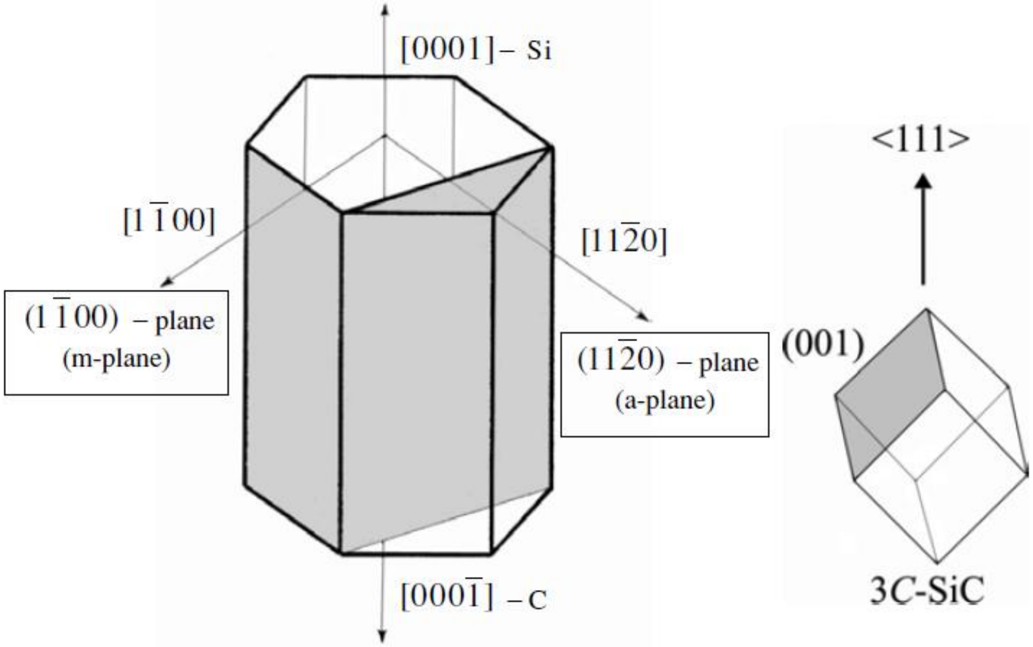

[0001]– Si
[1$\bar{1}$00]
(1$\bar{1}$00) – plane
(m-plane)
[11$\bar{2}$0]
(11$\bar{2}$0) – plane
(a-plane)
[000$\bar{1}$] – C
<111>
(001)
3C-SiC

Figure 4. Schematic images of the hexagonal and cubic crystal lattices of SiC [13].

The hexagonal and cubic crystal lattices are schematically shown in Fig. 4. Only in two SiC polytypes, the positions of all atoms are equivalent and correspond to either cubic (3*C*-SiC) or hexagonal (2H-SiC) sites of the crystal lattice (4*H*-SiC has one cubic and one hexagonal and 6*H*-SiC has two cubic and one hexagonal) [14]. In all other polytypes, atoms may occupy sites of both types and polytypes differ in the number of atoms in hexagonal (N_H) and cubic (N_C) positions (see e.g. [15]).

Therefore, it is convenient to characterize polytypes of silicon carbide by the parameter 'hexagonality' γ [16], which is defined as the ratio between the number of atoms in hexagonal positions and the total number of atoms in the unit cell:

$$\gamma = \frac{N_H}{N_H + N_C} \tag{1}$$

The hexagonality of a polytype may vary from unity (2H-SiC) to zero (3*C*-SiC). It is noteworthy that the ability to crystallize in different crystal lattices is inherent not only in SiC, but also in quite a number of other compounds: GaN, ZnSe, ZnO, diamond, etc. However, these other compound semiconductors normally crystallize only in the 3*C* and 2H polytypes, without the intermediate polytypes. By contrast, the extreme polytypes are more difficult to obtain for SiC, whereas this compound crystallizes in a plentitude of intermediate forms. 3*C*-SiC films of a rather large area have been obtained (see e.g. [17] or [18]), whereas 2H crystals exist at present only in the form of needles [19]. The absence of crystals with sizes suitable for device applications means that most of the electrical parameters of 2H-SiC have not been determined.

At present, there is no theory that would be satisfactory in every respect in explaining why SiC crystallizes in a wide variety of polytypes. It is not completely clear, either, what factors favor formation of one or another polytype.

A remarkable and beautiful feature of polytypism is the behavior of impurity atoms. In Fig. 5, it can be seen that the sites are not equivalent in the hexagonal polytypes 6*H*-SiC and 4*H*-SiC. The difference is in the second-nearest neighbors. A nitrogen atom substituting a carbon atom in the lattice can either occupy a "k" site or an "h" site in 4*H*-SiC. The k site is a lattice site that displays cubic symmetry, whereas the h site has hexagonal symmetry. The immediate vicinity of a nitrogen atom on either site is the same, but the second-nearest neighbors to the sites are different, which creates a slightly different core binding energy. Thus, 4*H*-SiC has two binding energies for the nitrogen donor, which has consequences when designing devices. 6*H*-SiC has three energy levels for nitrogen and 3*C*-SiC has only one. More complex polytypes such as rhombohedral (15R-SiC) have no less than five binding energies, although only four have been identified [12].

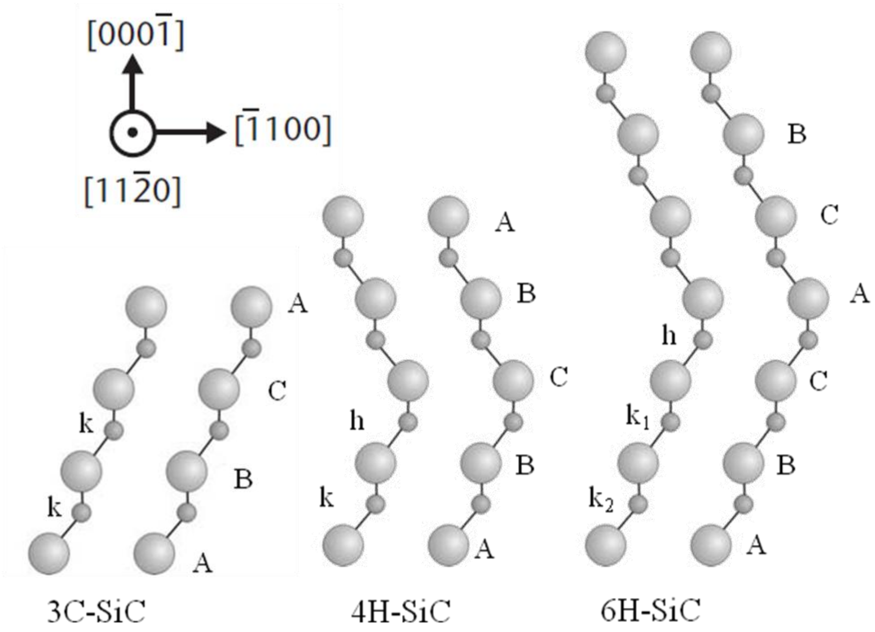


Figure 5. The three most common polytypes in SiC viewed in the [1120] plane. From left to right, 3*C*-SiC, 4*H*-SiC, and 6*H*-SiC; *k* and *h* denote cubic and hexagonal crystal symmetry points, respectively.

1.3 Material properties

1.3.1 Mechanical and chemical properties

SiC is a very hard material with a Young's modulus of 424 GPa [20]. It is chemically inert and reacts poorly (if at all) with any known material at room temperature. The only known efficient etch at moderate temperatures is molten KOH at 400 - 600°C. It also has no liquid phase and instead sublimes at temperatures above 1,800°C. The vapor constituents during sublimation are mainly Si, Si_2C, and SiC_2 in specific ratios, depending on the temperature.

1.3.2 Electronic properties

While the possibility to crystallize in different polytypes, being chemically inert, hard, and temperature resistant are all important properties, the aspect of SiC that has attracted so much attention concerns the unique electronic properties.

Due to the unstable nature on most polytypes, only three of them are commonly produced. They are called 6*H*-SiC, 4*H*-SiC and 3*C*-SiC. Most of the physical properties of these polytypes are identical, except the electronic ones. The main parameters of 6*H*, 4*H* and 3*C* SiC polytypes are listed in table 1. For electronic devices, each polytype has its specific advantages. For example, 4*H* is better suited for high power (e.g. high voltage electricity distribution) and high temperature (e.g. car or plane engines), while 3*C* should be better for high frequency applications (e.g. radar).

Table 1. Selected physical and electronic properties of the most common SiC polytypes [21].

Parameter	4*H*-SiC	6*H*-SiC	3*C*-SiC
Stacking order	ABCB	ABCACD	ABC
Jagodzinskii notation	hc	hcc	c
Percentage 'hexagonality', γ (%)	50	33	0
Lattice constant (Å)	a = 3.073 c = 10.053	a = 3.08 c = 15.117	4.34
Dielectric constant, ε	9.66	9.66	9.72
Bandgap (eV)	3.26	3.0	2.39
Thermal conductivity (W cm^{-1} °C^{-1})	3-4	3-4	3-4
Critical breakdown field strength, E_c (MV cm^{-1})	3	3	2
Electron mobility, μ_n (cm^2 V^{-1} s^{-1}) (300 K)	≤ 850	≤ 450	≤ 1000
Saturation rate, v_s (× 10^7 cm s^{-1})	2	2	2.7
Hole mobility, μ_p (cm^2 V^{-1} s^{-1}) (300 K)	≤ 120	≤ 100	≤ 40

1.3.2.1 Bandgap

The wide bandgap is what enables the use of SiC for very high temperature operation. Thermal ionization of electrons from the valence band to the conduction band, which is the primary limitation of Si-based devices during high temperature operation, is not a problem for SiC-based devices because of this wide bandgap.

The band structure is indirect, and the width of the bandgap strongly depends on the polytype; specifically, it depends on the percentage of hexagonality (γ from Eq. 1), and varies from 2.39 eV for 3*C*-SiC to 3.33 eV for 2H-SiC [21]. Thus, the difference in the bandgaps ($\Delta E_{g[H-C]}$) between the cubic (3*C*) and the purely hexagonal (2H) polytypes of SiC is 0.9 eV. The bandgap is plotted as a function of γ in Fig. 6. For other semiconductors exhibiting different polytypes (GaN, ZnS, ZnSe, etc), $\Delta E_{g[H-C]}$ is generally $\leq$ 0.2 eV [22].

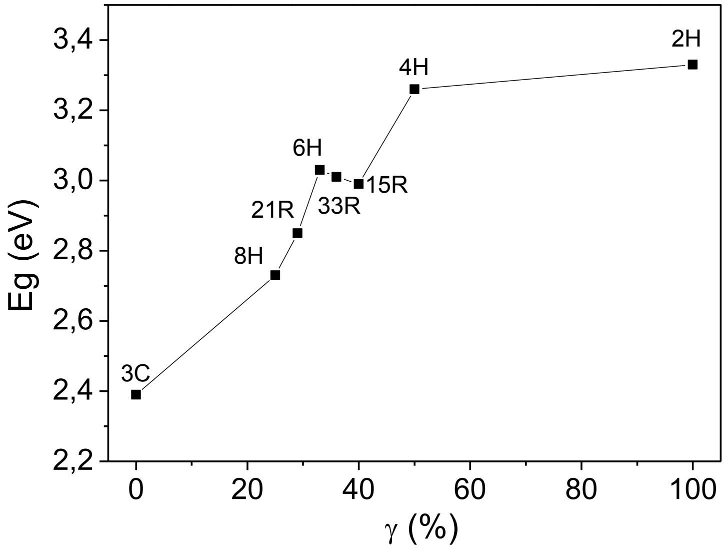


Figure 6. Energies of the indirect bandgap of several SiC polytypes as a function of the 'hexagonality' percentage [23].

1.3.2.2 Critical electric breakdown field

One of the most important properties for power-device applications is the critical electric breakdown field, E_C. This property determines maximum electric field that the material can support before suffering physical breakdown. Normally, wide bandgap materials have a high breakdown electric field because the wide bandgap leads to high impact ionization energy. Silicon carbide can withstand an electric field about ten times greater than GaAs or Si without undergoing avalanche breakdown [24]. This high breakdown electric field enables the fabrication of very high-voltage, high-power devices such as diodes, power transistors or high power microwave devices [25]. In addition, it allows close distances between adjacent devices, allowing high device packing density for integrated circuits. The breakdown voltage at a *p-n* junction is given by:

$$V_B = \frac{E_C W_d}{2} \tag{2}$$

where V_B is the breakdown voltage, and W_d the drift region width. Considering the same breakdown voltage, a significantly thinner drift region can be realized in SiC compared to Si. In Fig. 7, V_B is shown as a function of the drift region width for different materials.

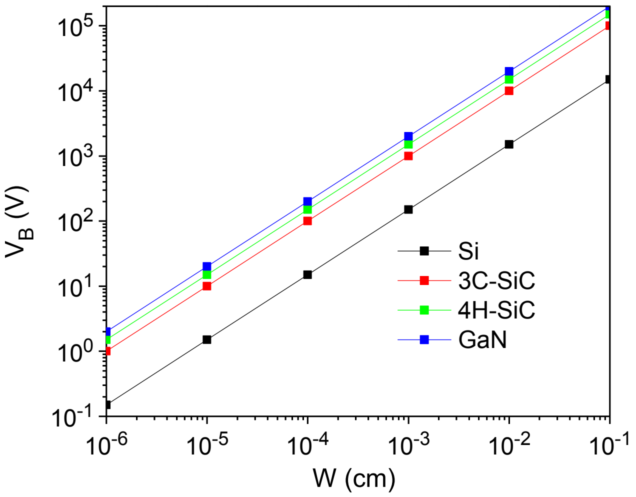


Figure 7. Breakdown voltage as a function of drift region width for Si, 3*C*-SiC, 4*H*-SiC and GaN.

The relative strength of E_C for SiC compared to Si of ten times refers to devices designed for the same blocking voltage. For a doping of approximately 10^{16} cm^{-3}, E_C for 4*H*-SiC is 2.49 MV/cm [26]. For Si, the value of E_C is about 0.401 MV/cm for the same doping [27]. In this comparison, the difference between SiC and Si is only about a factor of six and not the often advertized factor of ten. However, if one compares the critical strengths of devices made for the same blocking voltage, then a Si device constructed for a blocking voltage of 1 kV would have a critical field strength of about 0.2 MV/cm, which, when compared with the 2.49 MV/cm of SiC, amounts to the factor of ten.

1.3.2.3 Thermal conductivity

The second most important parameter for high power and high-frequency device applications is the material's thermal conductivity. An increase in temperature generally leads to a change in the physical properties of the device, which normally affects the device in a negative way. Most important is the carrier mobility, which decreases with increasing temperature. Heat generated through various resistive losses during operation must thus be conducted away from the device and into the package.

At room temperature, SiC has a higher thermal conductivity than any metal. The thermal conductivity of copper is 4.0 W/(cm-K) [28]. That of silver is 4.18 W/(cm-K) [28]. There is a dependence on the purity of the crystal as well as on the crystal direction [29]. High-purity semi-insulating SiC material has the highest reported thermal conductivity with a value of 4.9 W/(cm-K). Lower values are measured for the doped materials but the values remain above 4 W/(cm-K) at room temperature [30]. This property enables SiC devices to operate at extremely high power levels [31,32] and dissipate large amounts of excess generated heat, which causes a temperature increase that degrades the device performance [33,34]. Due to this, together with the low power losses and the high temperature capability [35,36], SiC devices can operate without thermal cooling system contrary to other semiconductor devices, such as Si. It is a great advantage in relation to cost, size and weight of power electronic systems.

1.3.2.4 Saturated drift velocity and carrier mobility

For high-frequency devices, a very important parameter is the saturated drift velocity v_s. It is one of the key material and device properties that determine the ultimate limit of speed of response and frequency of a device, such as a transistor. In a semiconductor, carrier velocity cannot indefinitely increase with the applied electric field. Carriers speed up in response to a stronger field until the saturation drift velocity is reached. At this point, higher fields do not result in any increase.

In SiC, the saturation drift velocity is 2-2.7 × 10^7 cm/sec [37], which is at least twice that of Si. A high-saturated drift velocity is advantageous in order to obtain as high channel currents and high frequencies as possible, and clearly SiC is an ideal material for high-gain, and high-speed solid-state devices.

Electrons and holes are accelerated by electric fields, but they lose momentum as a result of various scattering processes, such as lattice vibrations (phonons), impurity ions, crystal defects, surface or other material imperfections [38]. The drift velocity v_d of a carrier is proportional to the electric field E, provided that v_s has not been reached. The mobility μ is defined as the proportionality factor between v_d and E as

$$v_d = \mu E \tag{3}$$

The effects of all several microscopic phenomena are lumped into the macroscopic mobility introduced in the transport equations. The mobility is dependent on the local electric field, lattice temperature, doping concentration, polytype, crystal quality, local scattering at defects, etc. If the doping concentration increases, the mobility decreases due to scattering. For low doping concentration, the mobility decreases with temperature due to decreased vibrational energy of the lattice phonons [39,40].

1.3.3 Figures of merit for high power and high frequency devices

Owing to its wide bandgap, high heat conductivity and pronounced thermal, chemical and radiation stability, SiC has been regarded primarily for applications in the field of power electronics. The device potential of a semiconductor material is often estimated in terms of figures of merit. Johnson's figure of merit (JFOM) addresses the potential of a material for high frequency, voltage and power discrete amplifiers, according to [41]

$$JFOM = \frac{\left(E_B^2 v_s^2\right)}{4\pi^2} \tag{4}$$

where E_B is the breakdown electric field and v_s is the electron saturation velocity. The JFOM of 4*H*-SiC is up to 400 times better than Si and is only inferior to diamond.

Key's figure of merit (KFOM) instead considers the potentiality of a material for high frequency applications (like MOSFETs) [42]:

$$KFOM = \kappa\sqrt{\frac{cv_s}{4\pi\varepsilon}} \tag{5}$$

where κ, *c*, and ε are the thermal conductivity, the speed of light in vacuum, and the dielectric constant, respectively. Neither of these merits accurately describes the potential for power devices. Baliga's figure of merit (BFOM) [43] defines parameters to minimize the conduction loss in low-frequency applications:

$$BFOM = \varepsilon\mu E_B^3 \tag{6}$$

where μ is the carrier low-field mobility. In Table 2, the figures of merit are presented for n-type 3*C*-SiC, 4*H*-SiC, diamond [44], GaN [45], GaAs [45] and Si [45]. All values are normalized to Si. It seems that 3*C*-SiC is the best SiC option for high frequency switching, inferior only to diamond among these materials. By studying Table 2 it is clear that, from a purely theoretical point of view, diamond would be the ultimate semiconductor for power electronics. However, it should be mentioned that the figures of merit do not tell the whole story. In diamond, the energy levels of the dopants are much deeper than those in SiC, leading to poor operation at room temperature. There are also other problems related to the use of diamond that appear to be even larger than the problems faced by the SiC technology community [46].

Table 2. Relative figures of merit of different semiconductors.

	JFOM	KFOM	BFOM
Si	1	1	1
3*C*-SiC	324	4.83	163
4*H*-SiC	400	4.17	464
GaAs	1.78	0.32	14.6
GaN	1600	3.04	1507
Diamond	8,100	32.2	23,000

1.4 Growth

While it is beyond the scope of this chapter and this thesis to explain the details of SiC growth, the main principles of commercial bulk and epitaxial growth of hexagonal SiC will be summarized here. The specific growth of heteroepitaxial 3*C*-SiC on α-SiC substrates will also be discussed, since it is more essential to the topic of this thesis.

1.4.1 Hexagonal SiC bulk growth

Silicon carbide substrates are the key elements in the development of SiC epitaxial layers for electronic devices. Because of the phase equilibriums in the Si and C materials system (the material sublimes before it melts), the most popular bulk growth techniques are based on physical vapor transport. As previously mentioned in Section 1.1, Tairov and Tsvetkov [6] invented seeded sublimation growth in 1978. The techniques used today to manufacture SiC wafers are almost exclusively based on this concept. In this technique, a seed crystal of SiC is introduced into the reactor chamber and heated above the sublimation temperature. A thermal gradient is applied so that the seed is slightly colder than the source. Vapor transport of carbon and silicon bearing species from the source (or carbon species from the graphite walls) will thus occur to the seed where it condenses and the growth proceeds (usually along the *c*-axis). The principal vapor constituents during sublimation are Si, Si_2C, and SiC_2, and the ratio between them depends on the temperature. For a typical 4*H*-SiC bulk sublimation growth process, the SiC source temperature is 2100-2400°C [47].

1.4.2 Hexagonal SiC epitaxial growth

In order to improve the quality compared to the bulk material and to produce complex device structures, epitaxial techniques are necessary. Epitaxial layers are needed in all electronic SiC applications and their characteristics are mainly dependent on the intended final device. For example, power devices (from few hundred volts to some kilovolts) typically require low-doped (10^{14}-10^{16} cm^{-3}) and thick (5-100 μm) layers, whereas high-frequency devices require thin layers (less than 0.2 μm to several μm) with moderate (10^{16} cm^{-3}) to heavy (10^{19} cm^{-3}) doping.

Chemical vapor deposition (CVD) is presently the most widely used epitaxial technique for growth of SiC epitaxial layers for device structures. The basic steps occurring during CVD can be listed as follows (Fig. 8): reactant gases are transported by carrier gas to the reactor, reactant species diffuse through the boundary layer above the growth surface, reaction (adsorption or chemisorption) takes place on the surface, gaseous byproducts are transported away from the surface, they diffuse away through the boundary layer and are eliminated with the carrier gas [48-50].

There are several types of CVD reactors, e.g. vertical or horizontal, cold wall or hot wall, made of metal or quartz, working at atmospheric or low pressure, with or without plasma, with different heating types. The wafer is positioned on a resistively or inductively heated substrate holder and fed by a mixture of reactants, for SiC typically $SiH_4 + C_3H_8$ diluted in H_2.

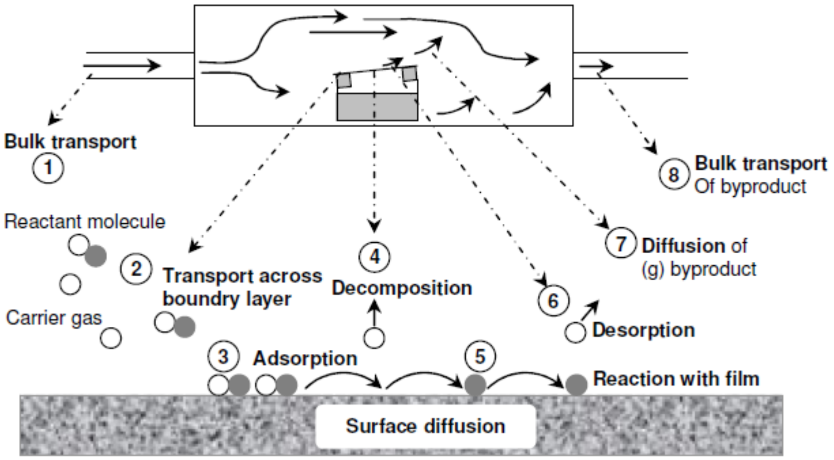

Bulk transport
1
Reactant molecule
Carrier gas
2
Transport across boundry layer
4
Decomposition
3
Adsorption
5
Surface diffusion
Reaction with film
6
Desorption
7
Diffusion of (g) byproduct
8
Bulk transport Of byproduct

Figure 8. Schematic of the fundamental steps involved during chemical vapor deposition [50].

Thanks to the massive progress achieved in SiC epitaxial growth in the last 25 years, it is now possible to grow high-quality epilayers on the bulk substrates. This progress has enabled the fabrication of virtually all types of semiconductor devices using SiC technology, as will be discussed in 1.5.

1.4.3 3*C*-SiC heteroepitaxy

All of the material used in this thesis started with a 3*C*-SiC layer that was heteroepitaxially grown onto some underlying substrate. Indeed, for 3*C*-SiC no real bulk growth exists, and the material is grown by heteroepitaxy onto Si or α-SiC substrates. This leads to the classical heteroepitaxial problems such as mismatch induced defects, interfacial reactivity and wafer bending [51].

Many attempts have been performed in order to grow high quality crystalline 3*C*-SiC films on Si substrates, but the huge lattice mismatch (20%) between Si (5.43 Å) and 3*C*-SiC (4.53 Å) and the large difference in thermal expansion coefficients (8%) lead to large stresses in the grown film [52]. This results in a poor crystalline quality of 3*C*-SiC and, consequently, in poor device characteristics.

1.4.3.1 β-α SiC heteroepitaxy

Growing 3*C*-SiC heteroepitaxially onto 6*H*-SiC or 4*H*-SiC could lead to an improvement of the crystalline quality of the cubic polytype, due to an almost negligible lattice mismatch (0.1%) between 3*C*-SiC and α-SiC [21]. The 0.1% lattice mismatch may seem strange if one considers the lattice parameters specified in table 1. However, in order to conceive how the cubic lattice is incorporated into the hexagonal one, it is necessary to look from above at a cube standing on one of its vertices. The projection of such a cube onto a horizontal plane will be a hexagon, as seen in Fig. 9. In this case, a growing 3*C*-SiC film will have another crystallographic orientation than that of the substrate. If the initial hexagonal substrate has a (0001) orientation, the grown 3*C*-SiC layer will have a (111) orientation. This means that the lattice constants of the cubic and hexagonal polytypes virtually coincide in the growth plane (lattice mismatch < 0.1%).

During the initial stacking of 3*C*-SiC on the (0001) hexagonal plane, two equally probable nucleation orientations (differing by a 60° rotation) are possible, as can be seen in Fig. 9. When 3*C*-SiC islands of different orientation nucleate and subsequently expand and meet during growth, the individual domains are separated by extended defects known as *double-positioning boundaries* (DPBs) [53]. We will see in chapter 3 that this type of defect provides a local path for leakage currents to pass through the 3*C*-SiC layer, and they have a particularly deleterious influence on the rectifying properties of metal-3*C*-SiC contacts.

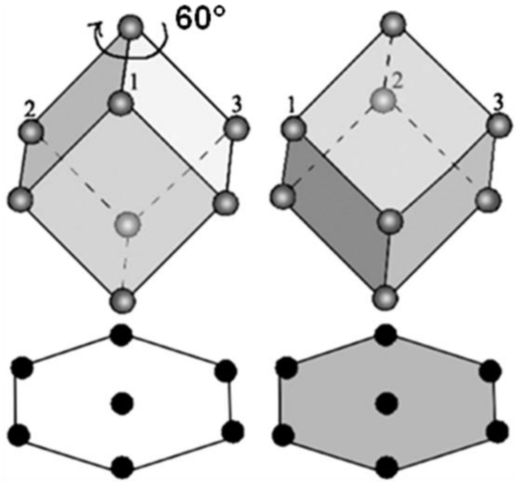


Figure 9. Incorporation of the cubic lattice onto the hexagonal SiC substrate.

1.4.3.2 β-α SiC heteroepitaxy by vapor liquid solid mechanism

In addition to CVD grown SiC heterostructures, 3*C*-SiC grown on α-SiC by a so called Vapor-Liquid-Solid (VLS) technique have been used for this thesis. A home-made deposition apparatus at the Université Claude Bernard, in Lyon, France, specially designed for VLS growth, was used. A schematic of the reactor is presented in Fig. 10. Briefly, the α-SiC (0001) on-axis or 2° off-axis seeds are placed at the bottom of a graphite crucible. Si and Ge pieces are then stacked on top of the seed and heated under purified Ar up to 1200-1450°C in order to form alloy melts containing various atomic % of Si. Propane is added at high temperature to start the VLS growth. The optimized use of this technique has been found capable of suppressing the DPB defects normally observed for β-α SiC epitaxy [53].

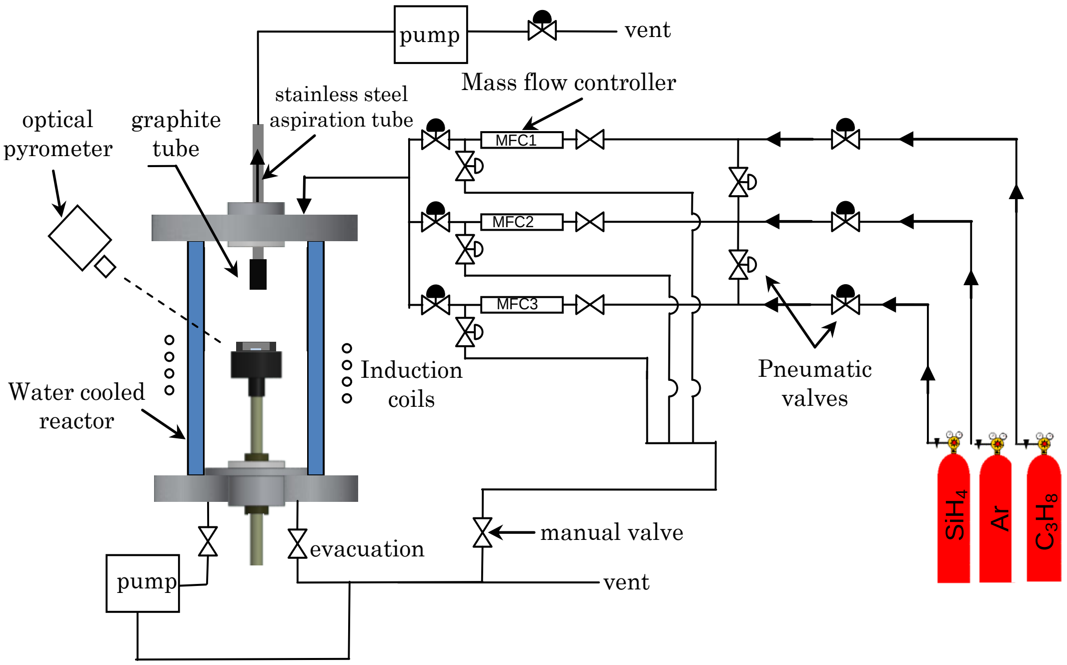

pump
vent
Mass flow controller
stainless steel aspiration tube
optical pyrometer
graphite tube
MFC1
MFC2
MFC3
Induction coils
Pneumatic valves
Water cooled reactor
evacuation
manual valve
pump
vent
SiH_4
Ar
C_3H_8

Figure 10. Schematic of the VLS equipment.

1.5 SiC devices and applications

The mainstream electronics of today has evolved over the last five decades through continuous developments of the silicon technology. Even if other semiconductors, like SiC, are emerging and displaying superior bulk properties compared to silicon, their role remains limited to niche markets. However, the dramatic and rapid development of silicon technology would not have happened if it had been locked in a race against the pre-existing technologies at that time, competing for the same applications (like vacuum tubes for signal amplifiers). Similarly, no remarkable development of SiC electronics should be expected if the efforts are limited to a competition with silicon for existing applications. So, how can SiC technology become attractive and competitive in the electronics market? A long chain of new applications cannot be created at the same level of sophistication or system complexity as in silicon technology, at least not in a foreseeable time. However, the extraordinarily high levels of complexity of integrated electronic systems, the nanosized structures, and the highly sophisticated functions are pushing Si technology ever closer towards its physical limitations. As such, the electronics community is pushed toward the development of new technologies in other materials.

The demand for low switching and conduction losses, as well as devices capable of high temperature operation is a major driving force behind power electronics technology development in wide bandgap semiconductors. The development of modern epitaxial techniques has lead to a rapid improvement in the material quality of silicon carbide, with the consequence that SiC devices have now become an interesting reality.

SiC technology surely opens up the possibility of a new generation of electronic equipment offering more effective, smaller and cheaper solutions. Actually, the conditions to make SiC the foremost semiconductor material for high temperature, high voltage, high frequency and high power applications exist [54,55]. It can be used in a large number of industrial and military areas and, in particular, in the harshest environments, such as nuclear reactors and space.

Because SiC has a critical electric breakdown field strength that is about ten times larger than that of Si, SiC power electronic devices can be made much thinner than the corresponding devices based on Si. Coupling this with the capability to handle larger current densities, SiC devices can be made smaller and more efficient. Also, because the thermal conductivity of SiC is approximately three times higher than that of Si, the size of power electronic devices can be further reduced in the cooling systems. Thus, the future of SiC technology looks very promising thanks to its smaller size, lower power losses, higher efficiency, and better heat-dissipation.

Comparing the properties of silicon carbide to some other semiconductors, one notes that SiC is superior in many regards. For example, the existing semiconductor technologies of Si and GaAs cannot tolerate high temperatures and chemically hostile environments, while the large Si-C bonding energy makes SiC resistant to high temperature, chemical attack and radiation. Most traditional integrated circuit technologies using silicon devices are not able to operate at temperatures above 150°C, especially when high operating temperatures are combined with high-power, high-frequency and harsh environment. High-temperature circuit operation from 350°C to 500°C is desired for use in aerospace applications (turbine engines), nuclear power instrumentation, satellites, and space exploration. These are environments and applications where SiC may really come to shine.

It is now clear that a change in technology from silicon to silicon carbide will revolutionize the power electronics. For instance, it will be economically feasible to use power electronics to a much larger extent than today. High power silicon carbide devices which operate at high temperatures will be used for a variety of power applications, e.g. in space-based, light-weight and radiation hard power systems, electric airplanes, military electric vehicles, engine control in new hybrid cars, and turbine engine actuators. Many of these applications require diodes and switches capable of blocking large voltages and conducting large currents, while operating at elevated temperatures and being subjected to harsh environments.

So far, a wide array of SiC devices has been experimentally demonstrated, including bipolar junction transistor (BJT). [56], insulated gate bipolar transistor (IGBT) [57], metal-semiconductor-field effect transistor (MESFET) [58], junction field effect transistor (JFET) [59] and metal-oxide-semiconductor field effect transistor (MOSFET) operating at temperatures up to 923 K [60], *p-n* junction diodes and Schottky diodes [61]. Additionally, heterojunction devices such as GaN/SiC heterojunction bipolar transistor (HBT) have been produced [62].

Looking at the power electronics market, today there are high-frequency JFETs offered commercially, as well as an emerging market for Schottky diodes made from SiC available from Cree, Infineon and ST microelectronics. Schottky diodes fabricated in 4*H*-SiC have been shown to have superior performance compared to Si-based devices. Due to SiC´s outstanding material properties, unipolar SiC based electronic devices show lower switching losses, combined with higher switching speeds and they also show better thermal stability. With the commercialization of silicon carbide diodes starting almost one decade ago (Infineon released its first generation of SiC Schottky diodes in 2001), today the SiC diode product line boasts a voltage range from 300 V up to 1700 V [59].

Considering the market for SiC, that of Schottky diodes is currently the largest, and it is continuously growing. Presently, the largest portion of these devices is used for power supply applications. However, many industry experts believe that the largest market for SiC Schottky diodes within the next years will be photovoltaic inverters for solar cells and photovoltaic plants, where the possibility to increase the efficiency of the inverter modules can lead to considerable savings in cost.

While SiC JFETs are becoming available on the commercial market they have not yet succeeded to the same extent. Furthermore, within this year some semiconductor companies announced the release of the first SiC MOSFETs and BJTs in late 2010.

Clearly, the future of this material seems to be bright. We are still at an early stage of the SiC revolution, however, and the material's full potential has yet to be realized.

Aside from the power device market, SiC has also found its way into the fields of radiation detectors and chemical sensors. SiC has proved to be efficient at absorbing short wavelength light, which has enabled the realization of SiC UV-sensitive photodiodes, including commercial UV flame detectors made by General Electric [63]. By monitoring and controlling the combustion gas-fired turbines used in electrical power generation systems, these UV flame sensors are reducing pollution emissions. Also high quality prototypes of other devices have been demonstrated, such as large-area SiC X-ray detectors based on Schottky diodes, which function at 100°C [64].

The high-temperature capabilities of SiC allow the production of catalytic metal-SiC and metal-insulator-SiC (MIS) structures used as gas sensors. The wide bandgap of silicon carbide permits an operation temperature of up to 1,000°C [65], with time constants for the gas response of a few milliseconds [66]. The high possible operating temperature of these devices, not possible with silicon, favors their use in combustion engines, where they could assist in active combustion control, reducing pollution emission from automobile and aircraft engines.

1.6 The interest in cubic silicon carbide (3*C*-SiC)

First of all, 3*C*-SiC is the only polytype with isotropic properties due to its cubic crystal symmetry. In addition, it is not subjected to micropipe defects formation. 3*C*-SiC has a larger saturated drift velocity than both 4*H*- and 6*H*-SiC polytypes, and more than twice that of Si, which is advantageous for obtaining higher channel currents in microwave devices [12].

Furthermore, among the three most stable SiC polytypes, 3*C*-SiC has the highest bulk electron mobility. The carrier mobility influences the frequency response or time response behavior of a device in two ways. First, the mobility is proportional to the carrier velocity for low electric field. Therefore, a higher mobility material is likely to have a higher frequency response, because carriers can move more readily through the device. Second, the device current depends on the mobility; i.e. higher mobility results in larger currents. At larger currents, the capacitance charges faster, leading to a higher frequency response [67].

An interesting future device application for 3*C*-SiC is as a metal-oxide-semiconductor field effect transistor (MOSFET) for high current and high voltage switching applications. Such application requires small donor ionization energy and low density of traps at the interface semiconductor/oxide interface. SiC in general has a great advantage over competing compound semiconductors in the possibility to easily grow silicon dioxide (SiO_2) by thermal annealing in an oxygen ambiance. However, in hexagonal polytypes the interface state density is high at the SiO_2/SiC interface, which leads to low inversion channel mobility in MOSFET devices [68]. On the other hand, using the 3*C* polytype, these interface states are located inside the conduction band due to its lower bandgap [69]. It should lead to superior inversion channel mobility in MOSFETs.

In recent years, the world's interest in the fabrication and study of heteropolytype structures based on SiC has considerably increased. Palyakov *et al.* [70] has demonstrated theoretically the possibility of high electron mobility transistor (HEMTs) in a hetero polytype junction β/α (3*C*/4*H* or 3*C*/6*H*). This study predicted the formation of a two-dimensional electron gas (2DEG) at such interface with superior potential for high electron mobility transistors (HEMTs) compared to the better studied AlGaN/GaN hetero system [70,71].

The properties that make especially the hexagonal to cubic SiC interface interesting can be summarized as follows:

1. The large difference in the bandgap between cubic and hexagonal polytypes lies almost entirely in the conduction band, yielding large conduction band offsets ($\Delta E_{c3C/6H} = 0.7$ eV and $\Delta E_{c3C/4H} = 1.0$ eV).

2. The abrupt change in spontaneous polarization between the polar 4*H*/6*H* polytypes and the non-polar 3*C* polytype leaves fixed positive charge on the C-face of the hexagonal structure, introducing an electric field at the interface which causes an accumulation of free electrons to form a 2DEG in the zincblende 3*C*, confined by the large band offset, as illustrated in Fig. 11.

3. The next to perfect lattice matching ($\Delta a/a < 0.1\%$ in the growth plane) should enable the growth of structurally perfect interfaces with no stress relaxation induced dislocation defects. These factors combine to open up the possibility for novel quantum-well heterostructures and two-dimensional electron gas (2DEG) high electron mobility transistor (HEMT) devices, based only on the different stacking sequences of chemically identical, but structurally different layers of SiC.

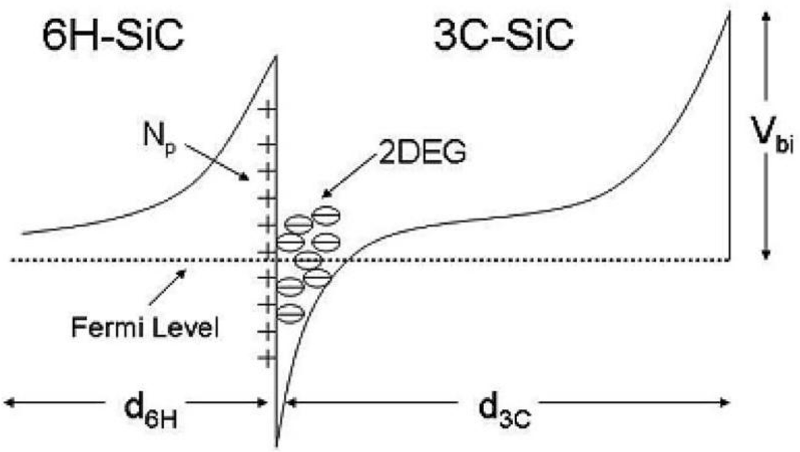


Figure 11. Energy band diagram at the 6*H*-SiC/3*C*-SiC heterointerface in the case of *n*-type material [72].

Some attempts have been made to investigate the formation of such a 2DEG [72-74], and it was first experimentally demonstrated in 2007 by Chandrashekhar *et al*. [73].

The benefits of 3*C*-SiC spreads across a vast number of domains, from power electronics to chemical sensors, medical applications and biotechnology. As growth processes continue to improve, so too will the many applications for which they are used since this is the key limiting factor for 3*C*-SiC technology insertions.

1.7 Defects

For power device applications, it is very important to get defect-free, high-purity SiC epilayers. Actually, a perfect crystal, where each atom of the same type is located in the correct position, cannot exist. All crystals have some defects. However, even if defects constitute a severe obstacle to the production of high quality SiC devices, they can also contribute to the conduction properties of the material. Thus, crystal defects are not always bad. Intrinsic defects are important for different applications of SiC [75], e.g., they govern the carrier life-time of high-voltage power devices and are also responsible for the color of the material [76].

Crystalline defects can be divided into point, line, planar, and volume defects, which are all characterized by a local disorder in the regular arrangement of the atoms. This sub-chapter will review point defects and linear defects in a general crystal. Planar and volume defect, hereafter commonly referred to as structural defects, will be discussed specifically for hexagonal and cubic SiC.

1.7.1 Point defects

Point defects can be either referring to vacancies, which are unoccupied sites in the crystal lattice that are usually occupied, or interstitials, which are atoms that occupy a site in the crystal structure where there ought to be no atom. A nearby pair of a vacancy and an interstitial, caused when an atom moves into an interstitial site and creates a vacancy, is called a Frenkel pair [77]. The occupation of a lattice site of an impurity atom that is not supposed to be in the lattice is known as a substitutional defect. These variations of point defects are illustrated in Fig. 12.

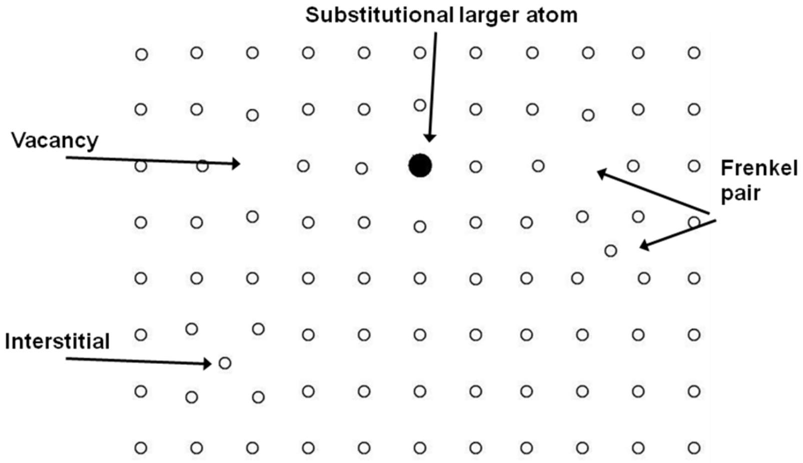


Figure 12. Different types of point defects in a crystal lattice.

1.7.2 Linear defects

There are two basic types of linear defects, the edge dislocation and the screw dislocation. They can be described as a lattice imperfection that is propagated only in a single line direction. Edge dislocations are caused by the termination of a plane of atoms in the middle of a crystal. In such a case, the adjacent planes bend around the edge of the terminating plane so that the crystal structure is perfectly ordered on either side (Fig. 13a). A screw dislocation occurs by atomic planes sliding over each other due to stress in the crystal (Fig. 13b). The direction and magnitude of the distortion in the crystal is expressed in terms of a Burgers vector. In an edge dislocation the Burgers vector is perpendicular to the line direction, and for a screw dislocation it is parallel to the line direction. In real materials, dislocations are mixed, having the characteristics of both. Dislocations can move if the atoms from one of the surrounding planes break their bonds and recombine with the atoms at the terminating edge [78].

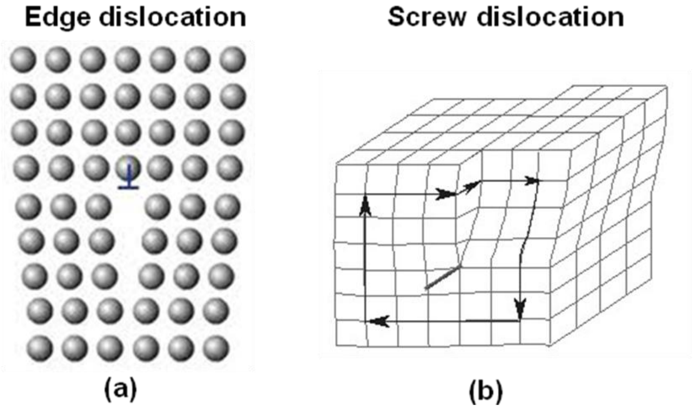


Figure 13. Atomic planes bending around a terminating crystal plane to form an edge dislocation (a), and planes sliding over each other to form a screw dislocation (b). The arrows indicate the Burgers vectors.

1.7.3 Structural defects in 4*H*-SiC

The most severe obstacle to the production of high quality 4*H*-SiC devices is a defect called *micropipe*, a sort of small wormhole with a diameter of the order of micrometers in the crystal structure. Micropipes are defects unique to the growth of SiC and they are physical holes which can penetrate large distances in the crystal [79].

It has been shown that micropipes are "killer" defects if they intersect the active regions of a device [80], i.e. placing any device directly on top of the micropipe is bound to cause failure. These defects are particularly disturbing for large-area devices such as high-power devices because the probability of placing a device on a micropipe naturally increases with the device area. To obtain decent yields, e.g. above 80%, for a 10-A Schottky device, micropipe densities must be in the order of 8 mp/cm^2. For a 50-A Schottky micropipe density below 2 mp/cm^2 is required. Usually, the density of micropipes ranges from a few to some hundreds per cm^2 [80]. While the micropipe formation is not fully understood, it is thought that they may be caused by several screw dislocations bunching together to form a giant screw dislocation, making it energetically favorable to open up a hollow core in the center [81]. A different way of forming micropipes may be simply by system contamination, where particles are trapped in the growing crystal, thus forming a micropipe [82].

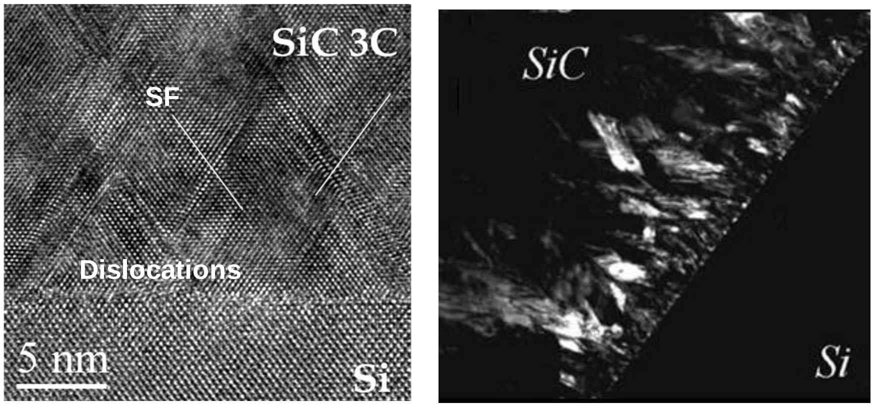
Even if the mechanism of their formation is not fully understood, in the last years great improvements have been achieved and “zero micropipe” 4*H*-SiC wafers are now available on the market [83]. This should result in reasonable yields of power devices.

The second defect that needs to be discussed is the *stacking fault*, which creates degradation of bipolar devices. A stacking fault can simply be described as a local region in the crystal where the regular stacking sequence of the Si-C bilayers (see 1.2.2) has been interrupted. Such an interruption can propagate along the growth direction for long distances, even all the way through an epilayer. PiN diodes operating under normal conditions begin to degrade [84,85], attributed to the expansion of stacking faults upon electrical stress [86]. While the diode is operating, stacking faults evolve with an accompanying reduction in carrier lifetime. The defects thus act as recombination centers for the carriers. Furthermore, the stacking order has been identified as that of the 3*C*-SiC polytype and, according to the study by Stahlbush, an explanation to the recombinative behavior of the stacking fault is that the 3*C*-SiC, having a lower bandgap than 4*H*-SiC, acts as a quantum well, thereby enhancing the recombination [87]. It is a very serious materials issue that must be solved prior to the realization of commercial bipolar devices.

1.7.4 Structural defects in 3*C*-SiC

The topic of investigation in this thesis is the properties of 3*C*-SiC interfaces. For this polytype, the level of material maturity is still at the stage where fundamental research is necessary. In the case of cubic silicon carbide, large concentrations of stacking faults, as well as twins, dislocations, anti-phase boundaries (APBs) and DPBs occurring in heteroepitaxial films have so far hindered the achievement of the predicted electrical properties, both within the semiconductor substrate and at metal/SiC interfaces [88].

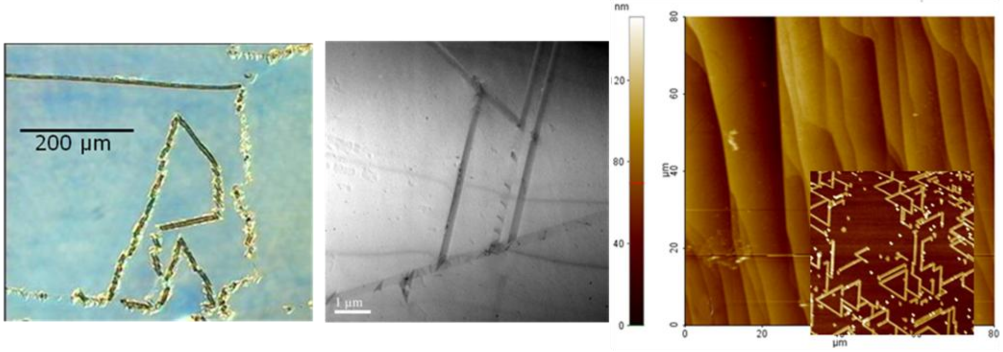
In 3*C*-SiC, micropipes cannot exist [89]. On the other hand, the probability of stacking fault formation is very high due to the low (even negative) SF formation energy for this polytype [89]. However, stacking faults are less crucial for device stability in this polytype since they do not cause bipolar degradation in 3*C*-SiC devices [90]. Aside from SFs, the type of defects present in the material depends on the substrate onto which the heteroepitaxial 3*C*-SiC is grown. Defect-generation occurs at the hetero-interface and in the 3*C*-SiC film itself. Common defects in 3*C*-SiC grown onto Si substrates include misfit dislocations (a type of edge dislocation caused by lattice strain due to the lattice mismatch), stacking faults, twins and APBs [52]. Fig. 14a shows a high resolution transmission electron microscopy (HRTEM) image of a 3*C*-SiC/Si interface, where misfit dislocations are visible at the interface, and SFs can be seen in the 3*C*-SiC layer. Twin generation may be considered as a result of the inverted stacking of bilayers. The most common defects in 3*C*-SiC are related to stacking errors on such planes (e.g. stacking faults and microtwins) [91]. In a layer with anti-phase boundaries, the crystallographic direction remains the same, but each side of the boundary has an opposite phase, related to the two possible twinning rotations of the SiC tetrahedron (see 1.2.1 and Fig. 1). In Fig. 14b, APBs forming at the interface can be seen for a 3*C*-SiC layer grown on (110) Si selecting the (111) diffraction spot to form a dark field image.



(a) **(b)**

Figure 14. HRTEM image showing misfit dislocations at the SiC/Si interface and stacking faults in the SiC layer (a), and dark field image of APBs forming at the interface (b) [91].

Unique to 3*C*-SiC grown onto hexagonal SiC substrates is the double positioning boundary (DPB) defect. This defect is similar to anti-phase boundaries, but comes from the way the cubic lattice is incorporated onto the hexagonal one. Their formation was discussed in 1.4.3.1 and is illustrated in Fig. 9. These defect regions are much larger than the anti-phase boundaries and can be seen even with an optical microscope, as can be seen in the Nomarski image presented in Fig. 15a, which was taken on 3*C*-SiC/4*H*-SiC structure grown by CVD at IFM at the Linköping University in Sweden. Additional results obtained from this sample, as well as the electrical behavior of DPBs, will be discussed in chapter 3. Upon closer inspection by transmission electron microscopy, large concentrations of stacking faults can be seen in the plan-view image in Fig. 15b. The morphology of a VLS-grown 3*C*-SiC/6*H*-SiC structure, grown at the Université Claude Bernard in Lyon, further reveals a surface characterized by large steps, alongside triangular pits (Fig. 15c).



(a) (b) (c)

Figure 15. Nomarski optical microscopy image of a DPB formed on a 3*C*-SiC layer that was grown onto 4*H*-SiC by CVD (a). Stacking faults arriving to the 3*C*-SiC surface of the same sample can be seen in the 8 × 8 μm^2 plan-view TEM image in (b). The AFM surface morphologies in (c) were determined on a 3*C*-SiC layer grown onto 6*H*-SiC by VLS, and show jagged steps visible on an 80 × 80 μm^2 area and triangular pits visible on a 10 × 10 μm^2 area in the inset.

Most of these defects have properties that are inherently nanoscale and that will strongly influence the electrical behavior of the material, particularly at interfaces commonly found in electronic devices, e.g. metal-semiconductor contacts (Ohmic and Schottky), *p*-type-*n*-type (*p*-*n* junctions) or dielectric-semiconductor interfaces (found e.g. in a MOSFET). Understanding the behavior of non-idealities at such interfaces will be crucial in order to predict the macroscale behavior of potential devices. Hence, significant efforts in fundamental research at the nanoscale have become mandatory to better understand the carrier transport phenomena, both at surfaces and interfaces.

The influence of the crystalline quality and the electrical homogeneity on the Ohmic properties of metal/3*C*-SiC interfaces is discussed in chapter 2. Chapter 3 discusses nanoscale transport at metal/3*C*-SiC rectifying (Schottky) interfaces, where structural defects can present preferential through-layer paths for detrimental leakage currents, causing lateral inhomogeneities in the Schottky barrier height and non-ideal carrier transport across the interface. The role of defects in the premature breakdown usually observed for MOS devices based on the SiO_2/3*C*-SiC interface is discussed in chapter 4. Indeed, structural defects can lead to interface roughness, in turn causing localized thinning of the dielectric and localized enhancement of the electric field. Moreover, defects at the SiO_2/3*C*-SiC interface can lead to localized increases in the oxide trap and/or charge densities, also contributing to the premature dielectric breakdown.

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Chapter 2

Ohmic contacts to 3*C*-SiC

A crucial issue for electronic devices is the capability to form reproducible and reliable Ohmic contacts, with a low specific contact resistance ρ_c. Good Ohmic contacts are important for the signal transfer between the semiconductor and the external circuitry. A contact resistance that is significant compared to the on-resistance of the device leads to a voltage drop at the metal-semiconductor interface, in turn resulting in decreased efficiency due to added resistive losses [1].

To form a good metal-semiconductor Ohmic contact, the contact metal should be chosen to minimize the rectifying energy barrier that forms when it is brought into contact with the semiconductor. However, the forbidden energy bandgap of 3*C*-SiC is more than twice as wide as that of Si. Hence, one should expect that all metals form sizable Schottky barrier heights with 3*C*-SiC, while the formation of Ohmic contacts with low specific contact resistances is more challenging than in the case of Si.

This chapter will first present a succinct review of the basic Schottky model of metal-semiconductor barriers, along with the physics of Ohmic contacts and a description of the technique most commonly used to determine the specific contact resistance. Thereafter, Ohmic contacts to 3*C*-SiC will be discussed, and the specific case of Ni-based Ohmic contacts to single crystal 3*C*-SiC grown by the vapor-liquid-solid (VLS) mechanism at the university of Lyon is investigated. The nanoscale and the macroscale electrical properties of the contacts were studied as a function of annealing temperature. It was found that increasing the annealing temperature gradually reduces the specific contact resistance, while the structural and nanoscale electrical homogeneities in the contact gradually increase.

2.1 Formation of metal-semiconductor contacts

Depending on the characteristics of the carrier transport across the interface, metal-semiconductor contacts are designated either as Ohmic or as rectifying (or Schottky). Ohmic contacts are characterized by linear and symmetric current-voltage (*I*-*V*) characteristics, with a voltage drop that is insignificant compared to the one caused by the on-resistance of the device [1]. Rectifying contacts, instead, display strongly non linear *I-V* behavior, where the current flows only under positive bias voltage conditions and conduction is blocked under reverse bias. Actually, the basis of one of the oldest semiconductor devices was formed in 1874, when Braun first reported on the rectifying properties of metal-semiconductor interfaces [2]. His article, which deals with an interface controlled device, marked the beginning of semiconductor science. In 1938, Schottky explained this rectifying behavior by the formation of depletion layers in the semiconductor side of such an interface [3]. In his honor metal-semiconductor devices with rectifying properties are often called *Schottky barrier devices*.

Fig. 1 shows the energy band diagram of a metal and an *n*-type semiconductor according to the *Schottky model.* A schematic of the system and the energy bands are shown before (a) and after (b) the metal-semiconductor system is brought into contact. The work function of a solid is the energy required to move an electron from the Fermi level of the material to the vacuum level. The metal work function Φ_m and the semiconductor work function Φ_s are indicated in the band diagrams in Fig. 1a. The semiconductor electron affinity, χ_s, is the potential difference between the bottom of the conduction band E_C and the vacuum level.

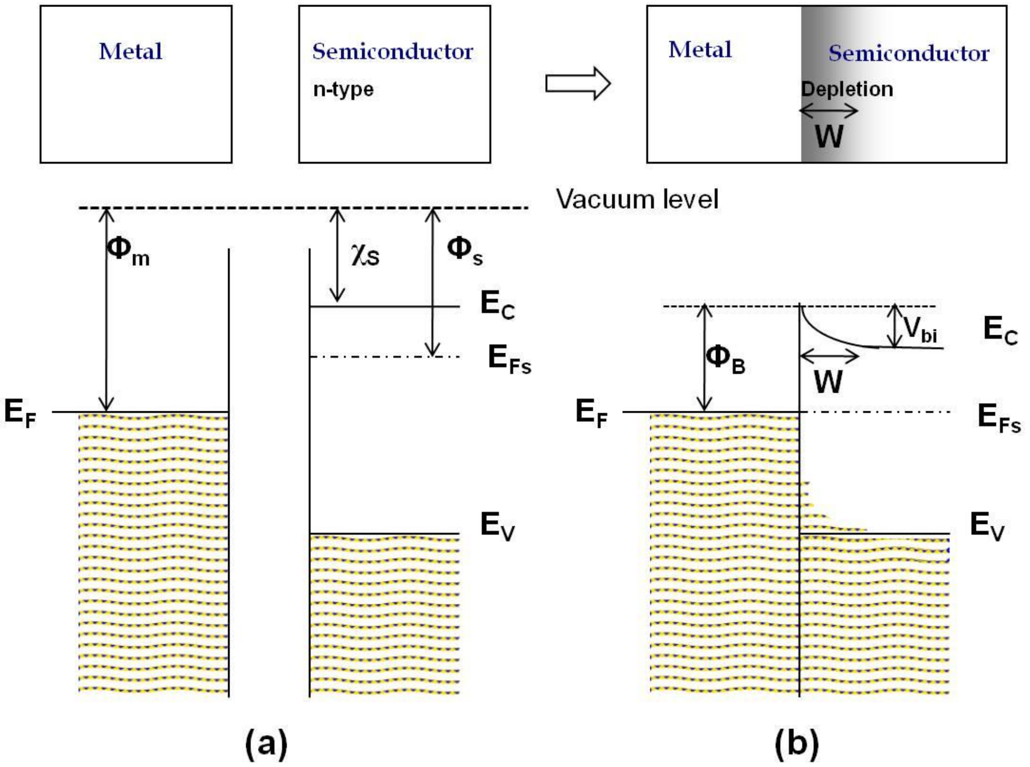


Figure 1. Schematic (top) and energy band diagram (below) for a metal and an *n*-type semiconductor contact according to the simple Schottky model. Fig. (a) and Fig. (b) show the system before and after contact, respectively. In this case, the situation $\Phi_m > \Phi_s$ results in the formation of a rectifying contact with a Schottky barrier height Φ_B [4].

When the materials are brought into contact (Fig. 1b), the Fermi levels in the two materials align in order to reach thermal equilibrium. For $\Phi_s < \Phi_m$, this means that electrons flow from the *n*-type semiconductor into the metal, thus depleting the majority carriers near the interface and creating a space-charge region with positively charged donors over the depletion width W in the semiconductor. The bottom of the conduction band level in the semiconductor is raised near the contact by the junction built-in potential, V_{bi}, according to

$$V_{bi} = \Phi_m - \Phi_s \tag{1}$$

The configuration in Fig. 1b generally results in the formation of a rectifying contact. The ideal Schottky barrier height, Φ_B, is the energy necessary for electrons in the metal to cross into the semiconductor after they have been brought into contact. The Schottky barrier height is extremely important in determining the properties of a metal-semiconductor contact since it determines the electrical behavior of both Ohmic and Schottky contacts. It is defined as the difference between the metal work function and the semiconductor electron affinity:

$$\Phi_B = \Phi_m - \chi_s \tag{2}$$

For $\Phi_m < \Phi_s$, an Ohmic contact is formed due to band alignment. In this case, electron transfer from the metal to the semiconductor lowers the energy levels at the interface, so that electrons can flow in either direction without having to overcome any barrier. However, most metals have work functions in the range 5-6 eV, while the electron affinities for most semiconductors are around 4 eV. Consequently, obtaining Ohmic contacts by work function engineering is infeasible.

To remedy this problem, the most widely adapted approach for the formation of Ohmic contacts to wide bandgap semiconductors involves the use of heavily doped material, whereby the ruling conduction mechanism can be controlled. While Φ_B is almost independent of the semiconductor doping concentration (it depends weakly on the doping through image force lowering [5]), the barrier width W depends on the doping level according to

$$W = \sqrt{\frac{2\varepsilon\varepsilon_0}{qN_D}\left(V_R + V_{bi}\right)} \tag{3}$$

where V_R is the applied reverse bias, q is the elementary charge, N_D is the density of ionized doping centres in the semiconductor, $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the permittivity of vacuum, and ε is the dielectric constant of the material (9.7 for SiC). Eq. 3 indicates that W increases roughly as $V^{1/2}$ and its value depends on the doping approximately according to $W \propto N_D^{-1/2}$. This dependence means that the main conduction mechanism depends on the doping level. For lightly doped semiconductors ($N_D < 1 \times 10^{17}$ cm^{-3}) the main conduction mechanism is *thermionic emission* [5], which is when conduction occurs through carriers crossing the Schottky barrier due to their sufficient thermal energy. In this case, the current density, J, across the junction is given by

$$J = A^{*}T^{2}e^{-\frac{q\phi_B}{kT}}\left(e^{\frac{qV}{nkT}}-1\right) \tag{4}$$

where A^* is the effective Richardson's constant for the semiconductor, T is the absolute temperature, q is the elementary charge, k is the Boltzmann constant, and n is the diode ideality factor.

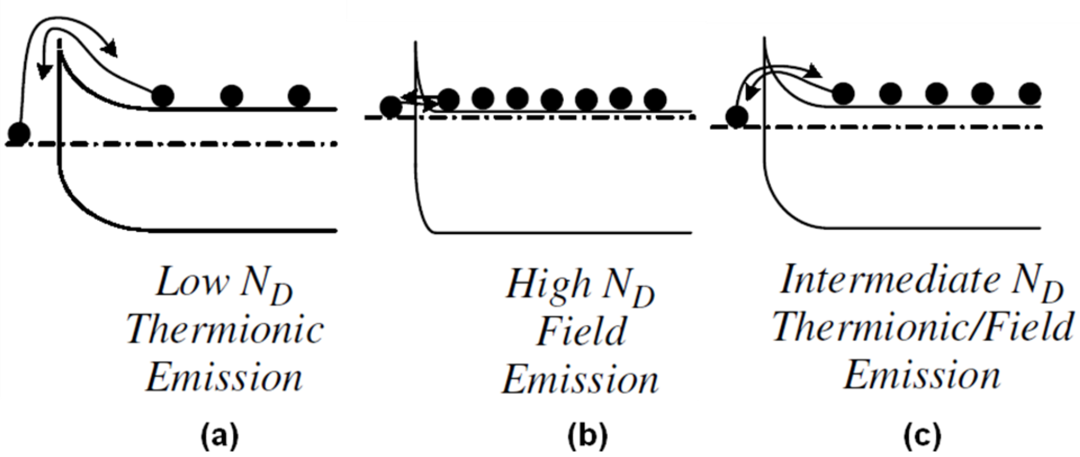
Heavily doped ($N_D > 1 \times 10^{19}$ cm^{-3}) material can be realized locally at the interface e.g. by ion-implantation and electrical activation through high temperature annealing. For a metal deposited onto a heavily doped semiconductor, the height of the Schottky barrier is the same as for lightly doped material but the barrier width is lower. The thin barrier favors carrier tunneling, leading to the formation of a tunnel Ohmic contact. In this case, the carrier transport is governed by the *field emission* mechanism.

For intermediate semiconductor doping levels, *thermionic field emission* is the dominating conduction mechanism. This mechanism is a combination of thermionic and field emission, meaning that the current transport through the barrier involves carriers that are thermally excited to an energy above the Fermi level, where the barrier is sufficiently thin for tunneling to take place.

The individual contributions of the three regimes to the total conduction is given by the characteristic energy, E_{00}, defined by

$$E_{00} = \frac{qh}{4\pi}\sqrt{\left(\frac{N_D}{\varepsilon\varepsilon_0 m}\right)} \tag{5}$$

where h is the Plank’s constant, and m is the tunneling effective electron mass. A comparison between E_{00} and the thermal energy kT shows that for $N_D < 1 \times 10^{17}$ cm^{-3}, $kT >> E_{00}$ and the thermionic emission mechanism (Fig. 2a) dominates. For $N_D > 1 \times 10^{19}$ cm^{-3}, $kT << E_{00}$ and field emission (Fig. 2b) dominates. For intermediate doping levels, $kT \approx E_{00}$ and the thermionic field emission (Fig. 2c) reigns. The band structure and the barrier width for the three different conduction regimes are illustrated in Fig. 2.



Low N_D
Thermionic Emission
(a)
High N_D
Field Emission
(b)
Intermediate N_D
Thermionic/Field Emission
(c)

Figure 2. Dominating electron conduction mechanism across a metal contact to *n*-type semiconductors for low (a), high (b) and intermediate (c) doping concentrations [6].

2.2 Specific contact resistance

The resistance measured between the two metal pads formed on a semiconductor sheet schematically shown in Fig. 3 consists of three components: the resistance of the metallic conductor R_m, the contact resistances R_c, and the semiconductor resistance R_s. The total resistance, R_T, is given by

$$R_T = 2R_m + 2R_c + R_s \tag{6}$$

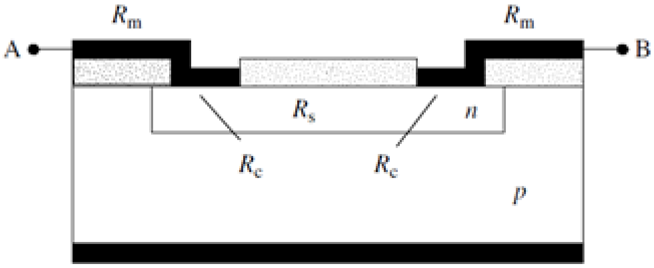


Figure 3. A schematic showing the various resistance contributions between two lateral contacts on a semiconductor [6].

The transport properties at a metal-semiconductor interface depends on several factors, like the barrier height of the metal, the carrier concentration in the semiconductor, the surface preparation method, the interface roughness, etc. While these factors are in principle independent of the contact geometry, they strongly influence the value of the contact resistance R_c. Therefore, a more important parameter, and the parameter that is determined from contact resistance measurements, is the *specific contact resistance* ρ_c (Ωcm^2). It is a very useful term for Ohmic contacts because it is independent of the contact area and therefore lends convenience to the comparison of differently sized contacts. In theory, it should be possible to define the specific contact resistance as the product of the total contact resistance R_c and the contact area (analogously with the resistance and the resistivity of a resistor). However, it is usually not the case that the entire lateral extent of the contact interface takes part in the conduction. The distance from the contact edge where the current density drops to $1/e$ of its highest value is called the transfer length, L_T. Moreover, ρ_c includes not only the contact interface but also the regions immediately above and below the interface. Therefore, the general definition of the ρ_c is instead expressed as a function of current density, according to [6,7]:

$$\rho_c = \left(\frac{\partial V}{\partial J}\right)_{V=0} \tag{7}$$

Since the current density depends on the applied voltage, the barrier height, and the doping density in a manner that varies for the three conduction mechanisms, the resulting expression can take on different forms. The expression in the thermionic emission regime is determined by combining Eq. 4 and Eq. 7, leading to

$$\rho_c = \frac{k}{qA^*T} e^{\frac{q\phi_B}{kT}} \tag{8}$$

As can be seen, in this regime ρ_c depends on Φ_B but is independent of N_D. In the field emission regime, on contrast, ρ_c depends strongly both on Φ_B and N_D, according to [8,9]:

$$\rho_c \propto e^{\frac{\phi_B}{\sqrt{N}}} \tag{9}$$

2.2.1 Determination of the specific contact resistance ρ_c

Due to non-idealities at the contact interface, such as current density and Schottky barrier inhomogeneities, ρ_c cannot be directly measured. Instead, it has to be determined through indirect approaches. While various techniques exist, the ones most commonly used comprise some adaptation of the transmission line model (TLM) [6].

The linear TLM technique consist of measuring the *I*-*V* behavior of an array of identical rectangular metallic pads of length *L* and width *Z*, separated by different pad distances *d*. A schematic of the specific measurement setup used in this work is illustrated in Fig. 4a, and *I*-*V* curves measured at the different pad distances are presented in Fig. 4b.

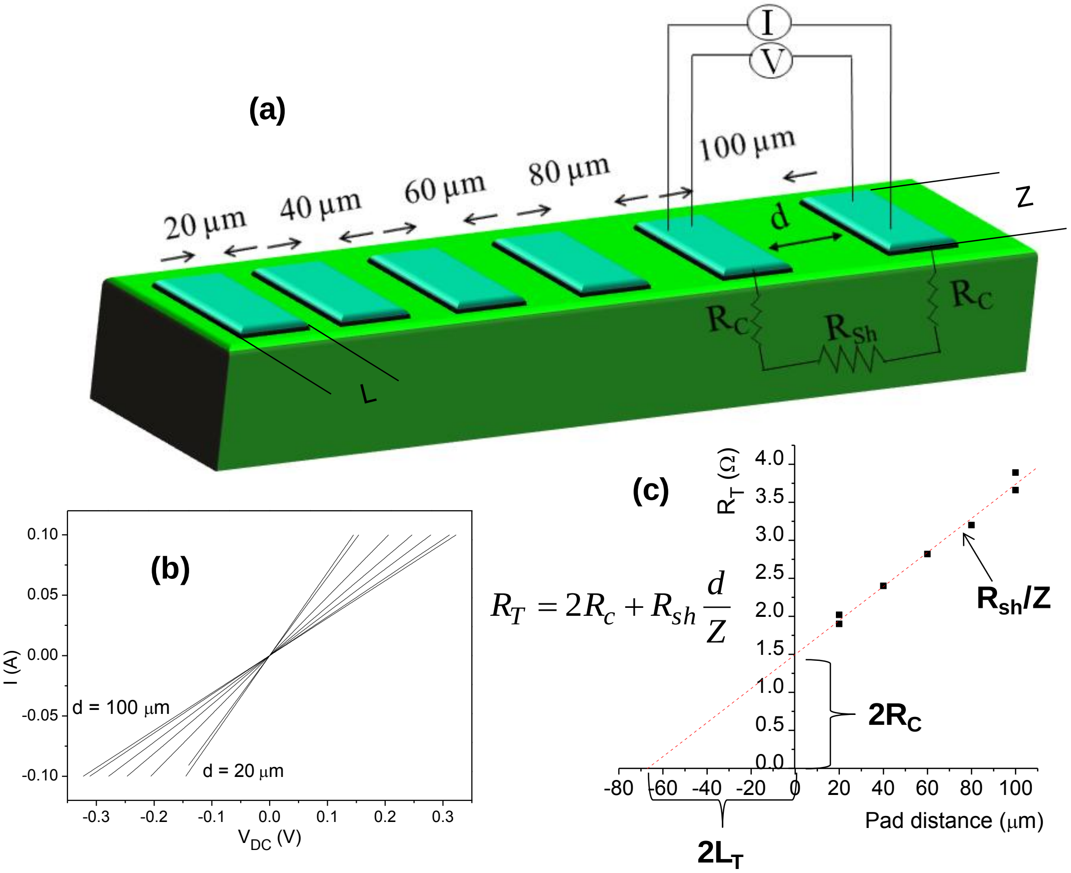

(a)
I
V
20 µm
40 µm
60 µm
80 µm
100 µm
d
Z
L
R_C
R_{Sh}
R_C
(b)
0.10
0.05
0.00
-0.05
-0.10
I (A)
d = 100 µm
d = 20 µm
-0.3
-0.2
-0.1
0.0
0.1
0.2
0.3
V_{DC} (V)
(c)
$R_T = 2R_c + R_{sh}\frac{d}{Z}$
R_T (Ω)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
R_{sh}/Z
$2R_C$
-80
-60
-40
-20
0
20
40
60
80
100
Pad distance (µm)
$2L_T$

Figure 4. Schematic of the TLM contact patterns (a). The total resistance R_T between two adjacent pads is determined from *I-V* measurements at different pad distances (b), shown here for as-deposited Ni contacts to VLS-grown 3*C*-SiC. From a plot of R_T as a function of the distance *d* between the pads (c), the contact resistance R_C, the sheet resistance R_{sh} and the transfer length L_T can be determined.

The total resistance R_T between two adjacent pads depends on the contact resistance R_C and on the semiconductor sheet resistance R_{sh} according to

$$R_T = 2R_c + R_{sh}\frac{d}{Z} \tag{10}$$

From the linear plot of R_T as a function of d (Fig. 4c), R_c can be determined from the intercept with the y-axis and L_T can be determined from the intercept with the x-axis. The semiconductor sheet resistance R_{sh} can be extracted from the slope.

The specific contact resistance can then finally be obtained from

$$\rho_c = R_c L_T Z tgh\left(\frac{L}{L_T}\right) \tag{11}$$

Two cases lead to simplifications of Eq. 11. For $L \leq 0.5\, L_T$, $tgh(L/L_T\,) \approx L/L_T$ and

$$\rho_c = R_c L Z \tag{12}$$

In the case when $L > 1.5\, L_T$, $tgh(L/L_T) \approx 1$ and

$$\rho_c = R_c L_T Z \tag{13}$$

For the contacts in this work, described in the next section, the relation $L \geq 3L_T$ was found, and consequently the approximation in Eq. 13 was used to extract the specific contact resistance values.

2.3 Ni based Ohmic interfaces to single crystal 3*C*-SiC

According to the discussion in 2.1, metal/SiC contacts are generally non-Ohmic after metal deposition, due to the high Schottky barriers at the interface. In order to overcome this problem, aside from using heavily doped material for creating tunnel Ohmic contacts, Ohmic contact to SiC are commonly formed by the deposition of a metal layer followed by an annealing process to generate an interface reaction (forming e.g. silicides, carbides, or ternary phases), with a subsequent reduction of the barrier height and/or barrier width.

Several different materials and surface preparation techniques have been studied in literature for the formation of Ohmic contacts to 3*C*-SiC [10-14], and the range of ρ_c is very large, going from 10^{-1} Ωcm^2 [10] to the high 10^{-6} Ωcm^2 [11]. Most studies report that nickel is the best material for contacts to *n*-type SiC, and that the contact properties improve with annealing temperature up to 950°C [11], whereas at higher temperatures there is a degradation of the contact properties [11,13]. Jae Il Noh *et al.* [10] showed that surface preparation and morphology play important roles, reporting a reduction of the specific contact resistance by almost two orders of magnitude after a chemical mechanical polishing (CMP) step that reduced the surface roughness from 21 to 6 nm. However, due to the difficulties to grow high quality 3*C*-SiC, until recently there have been no reports on Ohmic contact properties on single-domain crystals. This latter is a fundamental issue since the electrical quality of the contact can be directly correlated to the crystalline quality of the material. In this sense, a correlation between the macroscopic and the nanoscale electrical properties of the contact was not reported before, and it could enable a deeper understanding of the carrier transport mechanisms through metal/3*C*-SiC systems.

2.3.1 Experimental Details

About 0.7 µm thick, single-domain 3*C*-SiC (111) films were grown onto a 6*H*-SiC (0001) substrates by a vapor-liquid-solid mechanism, using a $Si_{25}Ge_{75}$ melt. This Si-Ge molten alloy was fed by propane at 1400°C for 30 min to grow the 3*C*-SiC films [15]. Growing under these conditions leads to a single-domain 3*C*-SiC layer, *n*-type N doped (nominally $N_D \approx 10^{18}$ cm^{-3}) [16]. On top of the 3*C*-SiC films, 100 nm thick Ni layers were deposited by e-beam evaporation. TLM patterns were fabricated in order to study the electrical properties of the contacts, using optical photolithography and wet etching of the metal.

The samples were subsequently subjected to rapid thermal annealing (RTA) steps in a Jipelec JetFirst oven, in inert ambient (Ar) for 60 seconds at temperatures between 600°C and 950°C. After each annealing step, several TLM patterns were measured and the specific contact resistance was then extracted by employing a linear regression method [6].

A PSIA XE-150 scanning probe microscope (SPM) was used to study the surface morphology of the layers by tapping mode atomic force microscopy (AFM) measurements. Besides the conventional macroscopic current voltage (*I*-*V*) characteristics, after each annealing step, a nanoscale electrical characterization of the contacts was carried out by local current measurements using a Veeco DI Dimension 3100 equipped with the Nanoscope V electronics and the C-AFM module. Conductive Si tips, covered with boron-doped polycrystalline diamond, were used due to their excellent stability [17]. Local current mapping was performed by scanning the C-AFM tip in contact mode over 10 µm × 10 µm areas on the contacts. A constant bias of 10 mV was applied to the C-AFM tip during the scans. Local vertical *I-V* curves between the back and the front of the sample were obtained by moving the tip in 1 µm steps over an area of 5 µm × 5 µm, sweeping the bias from -1 to 1 V at each tip position. A schematic of the experimental setup for the AFM and C-AFM measurements, along with the sample structure, is presented in Fig. 5.

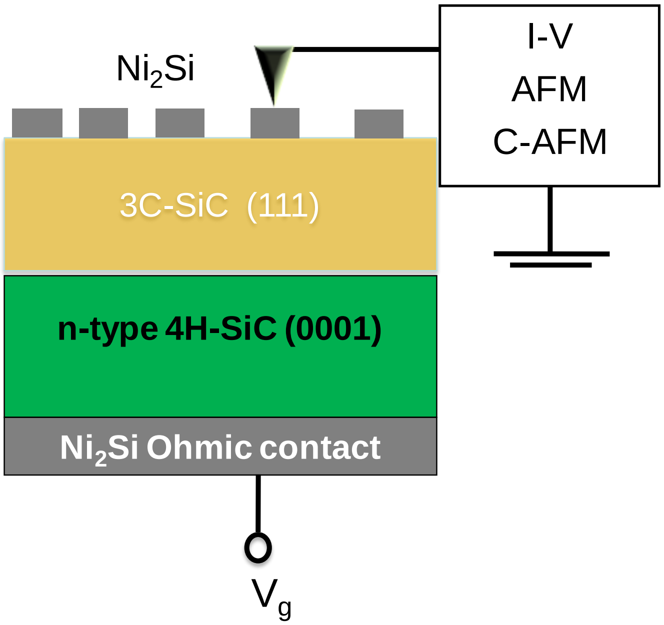


Figure 5. Schematic of the sample structure and the experimental setup during the AFM and C-AFM measurements. The SPM tip in scanned across the surface in a constant-force, tapping mode to register the surface morphology, whereas the current maps are obtained while scanning the C-AFM tip in contact mode across the contact. Localized *I-V* curves are obtained by sweeping the bias voltage while the tip remains firm and in contact with the metal surface.

Polytype identification of the 3*C* layers was performed by micro-Raman spectroscopy. Raman spectra were taken by using a continuous multi-line Ar ion laser beam operating at 514.5 nm. A confocal microscope (DILOR) focuses the laser beam onto the particle in a 1 µm diameter spot using a 100x Olympus objective with a power on the sample mostly maintained at 0.3 mW (and always lower than 0.5 mW). The spatial resolution and depth focus used in this work were better than 2 µm. The spectral resolution was 8 cm^{-1} with a peak accuracy of 1 cm^{-1}. Even though a confocal configuration was used to narrow the depth focus to just the 3*C* layer, contribution from the substrate could not be eliminated due to the small thickness of the layers. In cases where the frequencies of the longitudinal optical (LO) phonons are comparable with those of plasma oscillations of the free charge carriers, the interaction of these longitudinal oscillations lead to mixed plasmon–phonon modes [18,19]. An analysis of the frequencies and shapes of such modes allows evaluation of the carrier concentration [20]. In this work, the carrier concentration was extracted from the position of the LO phonon-plasmon coupled peak in the Raman spectra based on the reference data presented in [19].

X-ray diffraction analyses were recorded on a Bruker-AXS D5005 θ-θ diffractometer, using Cu K_α radiation operating at 40 kV and 30 mA to monitor the structural evolution of the contacts (phase formation) after each annealing step.

2.3.2. Characterization of the 3*C*-SiC layers

First, the presence of a 3*C*-SiC layer was investigated by micro-Raman spectroscopy. The transverse optical (TO) phonon peaks of the 6*H* substrate and the 3*C* layer are very close in the spectra. The 6*H*-SiC (0001) crystals present three TO active modes at 768, 789 and 796 cm^{-1}, where the last one is the weaker. On the other hand, the 3*C*-SiC (111) crystals produce only a strong 798 cm^{-1} TO mode [21]. However, the individual peaks can still be resolved and the peak visible at 798 cm^{-1} is the fingerprint of the 3*C*-SiC polytype, as can be seen in Fig. 6.

Micro-Raman spectroscopy was also used to estimate the doping level of the 3*C*-SiC layer. In fact, the position and shape of the LO peak is known to be *n*-type doping dependent, allowing approximation of the carrier concentration [19]. The 3*C*-SiC LO peak in the spectrum was found at 973.0 ± 0.5 cm^{-1} (see inset in Fig. 6). With this value, the *n*-type doping was estimated to be 3-6 × 10^{17} cm^{-3}, based on the reference data presented in [19].

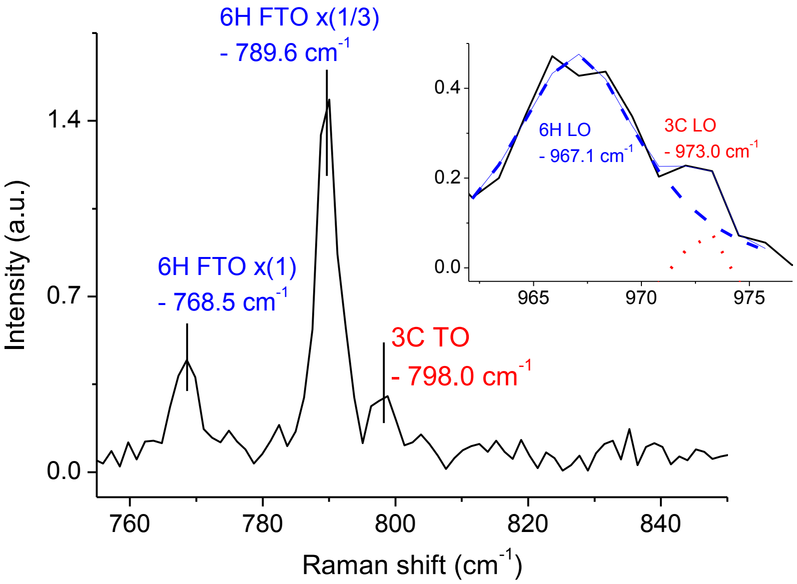


Figure 6. Micro-Raman spectrum measured on the as-grown VLS layer. The laser spot was focused to a 1 µm diameter spot on the surface. The inset shows curve fitting performed in order to determine the position of the 3*C* LO peak.

Since the quality of the semiconductor surface is of major concern for device processing, AFM was used to monitor the surface morphology of the 3*C* epilayers and a micrograph of the sample surface is presented in Fig. 7. The surface roughness (RMS) values of the layers were determined over a scanning area of 80 µm × 80 µm. A relatively high RMS value of 16.3 nm was determined. The high roughness can be related to the VLS growth mechanism of 3*C*-SiC onto 6*H*-SiC on-axis substrates, which leaves a surface characterized by jagged steps [16]. However, it is possible to improve the surface morphology by a homoepitaxial regrowth of 3*C*-SiC layers by chemical vapor deposition and a subsequent chemical mechanical polishing process [10].

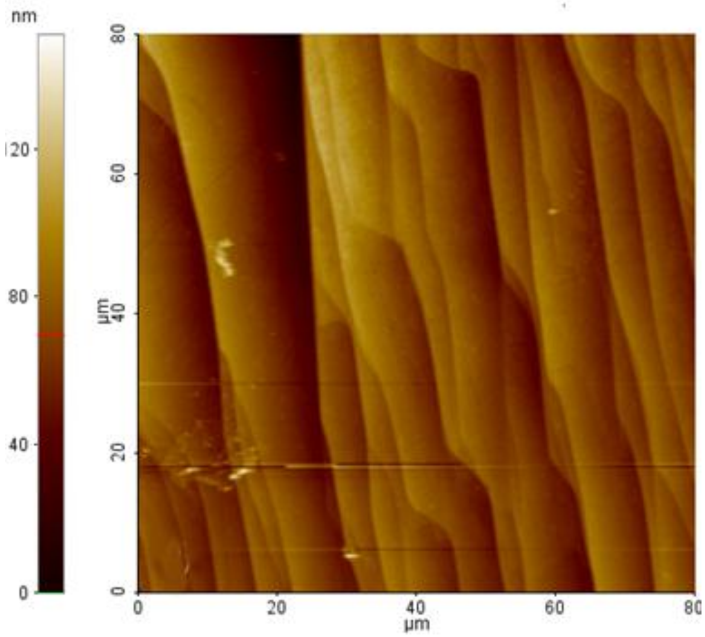


Figure 7. AFM micrograph determined over a scanning area of 80 µm × 80 µm on the 3*C*-SiC surface, yielding an RMS roughness value of 16.3 nm.

2.3.3. Structural evolution of the Ni/3*C*-SiC system upon annealing

The XRD patterns shown in Fig. 8 reveal the formation of different nickel-silicide phases in the contacts upon annealing. Up to an annealing temperature of 600°C (not shown in Fig. 8), no phase formation occurred, as only the peaks of the unreacted Ni were observed. Other studies report different temperatures required for thermal reactions to occur in the Ni/3*C*-SiC interface, depending on the orientation of the 3*C*-SiC crystal. Some authors report that reactions start at around 500°C [11,22-24] while others [25,26] agree with the findings in this work, reporting that annealing temperatures above 600°C are necessary for any reaction to take place. These results can be related to the different surface energies in the different 3*C*-SiC orientations. The (111) direction of the films in this study is the most stable 3*C*-SiC direction, therefore having the highest surface energy and the lowest concentration of dangling bonds [27]. This means that higher activation energy (i.e. higher annealing temperature) is involved in the formation of nickel silicide.

Thermal reactions started at higher temperatures, and a coexistence of the Ni_5Si_2 (also designated $Ni_{31}Si_{12}$ in the literature) and the Ni_2Si phase was observed upon annealing between 750°C and 850°C. The Ni has been totally consumed during the silicidation process, since no peaks related to the unreacted Ni were detected. Finally, after annealing at 950°C, only the most thermodynamically stable phase (in this temperature range), Ni_2Si, was detected [28]. Since only binary Ni-Si phases were observed between 750°C and 950°C, the carbon atoms in the consumed SiC layer have either been dissolved in the silicide film by the formation of precipitates in the reaction layer [29] or they have migrated toward the surface to form a thin graphite layer on top of the surface, as previously reported by Gasser *et al*. [30]. In our case, the overall degree of graphitization is higher at 950°C than at 850°C, as demonstrated by the intense graphite (101) XRD peak visible at 44.60° after annealing at 950°C.

The results observed in our 3*C*-SiC samples are similar to the evolution of Ni contacts on 4*H*-SiC with respect to annealing temperature. In fact, after annealing at 950°C, only the most stable Ni_2Si phase is present in both systems (Ni/3*C*-SiC and Ni/4*H*-SiC). Furthermore, also in the case of 4*H*-SiC, thermal reactions are reported to start in the temperature range 400-600°C (depending on surface and annealing conditions), where the coexistence of Ni_3Si_2 and Ni_2Si after annealing at 600°C is observed [4].

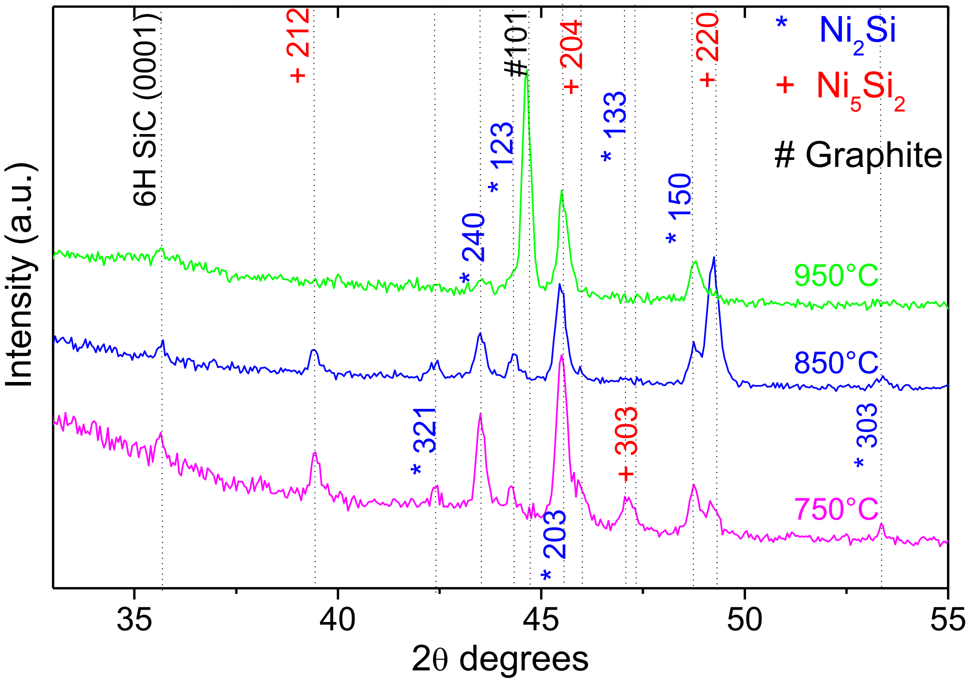


Figure 8. XRD patterns of a Ni/3*C*-SiC (111) sample after annealing at 750°C, 850°C, and 950°C.

2.3.4 Electrical properties of the annealed Ni/3*C*-SiC system

The specific contact resistance, $\rho_{c,}$ was determined by use of TLM measurements performed after annealing at different temperatures, and the resulting values are reported as a function of annealing temperature in Fig. 9. As can be seen, the specific contact resistance decreases with increasing annealing temperature. Specifically, ρ_c underwent a reduction from 5.0×10^{-5} Ωcm^2 after RTA at 600°C to 1.5×10^{-5} Ωcm^2 after RTA at 950°C (solid curve in Fig. 9).

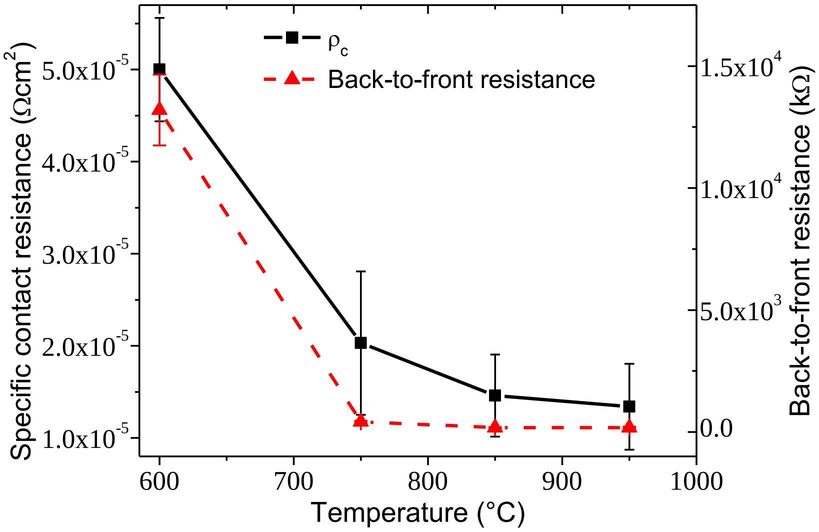


Figure 9. Annealing temperature dependence of the specific contact resistance (solid curve), measured by TLM, as well as the nanometric vertical resistance (dashed curve), measured by C-AFM.

The nanoscale electrical properties were determined by local current measurements with conductive atomic force microscopy, performed using diamond-coated Si tips. The C-AFM setup allowed the simultaneous acquisition of surface topography and current maps by scanning a biased, conductive, tip in contact mode on the metal surface. A constant bias was applied between the C-AFM tip and the sample back-contact during the scan. The C-AFM map reports, for each position of the scanning probe tip, the current which is injected into the metal through the nanometric tip contact, flows across the metal/3*C*-SiC interface and is collected at the semiconductor back-contact. Hence, the value of the local front-to-back current is affected by several resistive contributions, e.g. the resistance of the scanning probe tip, R_{tip}, the series and the spreading resistance of the metal layer, $R_{\mathrm{s,m}}$ and $R_{\mathrm{spr,m}}$, respectively, the contact resistance, the series and the spreading resistance of the semiconductor, $R_{\mathrm{s,s}}$ and $R_{\mathrm{spr,s}}$, respectively, and the back contact resistance, R_{b} [17]. The resulting total resistance, R, can then be described by

$$R = R_C + R_{s,m} + R_{spr,m} + R_{tip} + R_{s,s} + R_{spr,s} + R_b \tag{14}$$

However, when comparing the current maps after annealing in the considered temperature range (600 - 950°C), the changes in the 2D current distribution can only be ascribed to structural changes in the metal or to modifications of the metal/3*C*-SiC interface. No changes in the 3*C*-SiC heteroepitaxial layer are expected to occur after annealing at these temperatures. Hence, the 2D current maps determined by C-AFM constitute a means to directly monitor the evolution of the electrical homogeneity of the contact upon annealing. A similar approach was recently demonstrated to locally correlate the structural and electrical properties of Ohmic contacts on AlGaN epilayers [31].

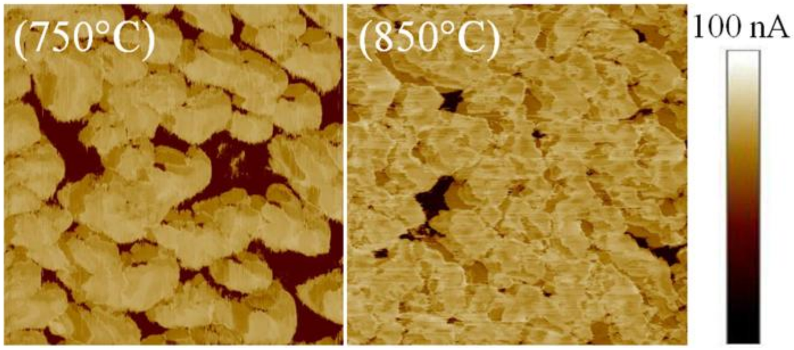


Figure 10. Local current distribution obtained by C-AFM over areas of 10 × 10 μm^2, after RTA at 750°C and 850°C, showing a decidedly increased electrical uniformity after annealing at 850°C.

The local current distribution on the contacts, monitored over scanning areas of 10 μm × 10 μm after annealing at 750°C and 850°C, is shown in Fig. 10. Alongside the increased structural uniformity (as observed by XRD), it is clear that also the uniformity of the current distribution improves with increasing annealing temperature. Moreover, in order to correlate the macroscopic electrical evolution of the contacts (from TLM) with the nanoscale current transport (from C-AFM), the local nanometric back-to-front resistance was determined from local *I-V* curves obtained by moving the C-AFM tip in 1 μm steps over an area of 5 μm × 5 μm, sweeping the bias from -1 to 1 V at each tip position. The reported values of the nanometric resistance are the average values extracted from 25 *I-V* curves. The values of this resistance as a function of annealing temperature are reported in Fig. 9 (dashed curve), in order to have a direct comparison with the trend of ρ_c (solid curve). The changes in the vertical resistance can be seen as changes in the contact resistance by considering that only the first three terms in Eq. 14 are expected to change upon annealing. Moreover, the low resistance values of Ni and its silicides means that the dominating out of the three contributions that change upon annealing is the contact resistance. Clearly, the nano- and macroscale resistances follow similar trends. This correlation can be attributed to the gradual improvement of both the structural homogeneity and the current uniformity with increasing annealing temperature, as observed by XRD and C-AFM, respectively.

2.3.5 Comparison with contacts to 3*C*-SiC grown by other techniques

In addition to the material quality, two important factors for Ohmic contacts are surface roughness and carrier concentration. As an example, a higher carrier concentration results in a narrower energy barrier and increased tunneling. The existence of a relation between the surface morphology of the semiconductor and the Ohmic contact properties has been previously established [10]; the lower the surface roughness, the better the contact. It was shown in [10] that a significant reduction of the specific contact resistance (specifically, the value was reduced from ≈ 10^{-1} to ≈ 10^{-3} $\Omega\mathrm{cm}^2$ in that study) is possible using CMP treatment of the sample surface prior to metallization.

Fig. 11 shows a comparison between the specific contact resistance values found for the VLS grown 3*C*-SiC in this work and the ones found in literature concerning Ni-Si contacts to 3*C*-SiC that has been grown by other techniques. The red dots correspond to the lower horizontal axis and are related to the semiconductor surface roughness, whereas the black squares correspond to the upper axis and are related to the doping concentration. The higher the doping and the lower the roughness, the better the specific contact resistance should be. Consequently, any value placing in the lower left of this graph is an indication of good crystalline quality. Indeed, the values obtained on the contacts to our single-crystal VLS layer are down and to the left. In order to find such low specific contact resistances for 3*C*-SiC grown by other techniques it is necessary to go either much lower in roughness, or much higher in doping. Considering the carrier concentration and the high roughness of the VLS grown epilayer, the measured specific contact resistance is remarkably low, which hints towards superior crystal quality.

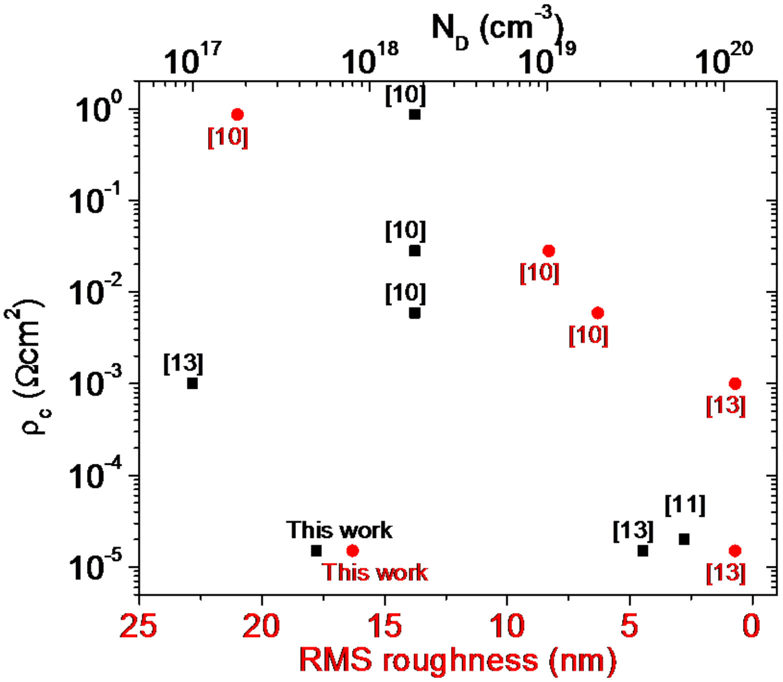


Figure 11. ρ_c **as a function of RMS surface roughness and epilayer doping concentration for the contacts in this study compared to values found in the literature. The red dots correspond to the lower horizontal axis and the semiconductor surface roughness, whereas the black squares correspond to the upper axis the doping concentration.**

2.3.6 Nanoscale homogeneity of the contacts related to macroscopic electrical properties

From the literature data regarding Ni-based contacts to 4*H* and 6*H* SiC, it is known that a good Ohmic contact is formed in the range of 900-1000°C, which is where a formation of carbon clusters inside the silicide is normally observed [4,32]. Indeed, the intense graphite (101) peak visible at 44.60° in the XRD pattern after annealing at 950°C (Fig. 8) demonstrates that such a process has taken place also in the contacts formed on our 3*C*-SiC layer. The role of carbon is believed to be crucial for the contact properties. In particular, the mechanism of Ohmic contact formation in a Ni/SiC system upon annealing is typically ascribed to the formation of carbon clusters inside the silicide, leaving vacancies which act as electron donors for SiC

[33]. The presence of these carbon vacancies near the interface increases the net carrier concentration under the contact, leading to increased tunneling current and a reduced contact resistance.

Measurements presented in this thesis, however, allow the visualization of an additional aspect: from the current maps in Fig. 10 it is evident that the uniformity of the current distribution increases with increasing annealing temperature. Each C-AFM micrograph comprises a 512 × 512 data points matrix, each point holding the value of the current at a specific position in the 2D map. The statistical distribution of these data points (see as an example the inset in Fig. 12) results in two distinct peaks, one near zero current and another around the maximum current value in the micrograph. From these distributions, the effective conductive area of the contact was estimated from the percentage of data points belonging to the high current distribution peak. Clearly, the effective area of the contact is directly related to the local resistance. In fact, as can be seen in Fig. 12, the inverse of the effective contact area percentage versus annealing temperature follows a similar evolution to that of the specific contact resistance up to 850°C. The decrease of the effective contact area upon annealing at 950°C can likely be attributed to a strongly increased presence of carbon clusters after annealing at this temperature (as indicated by the appearance the intense graphite (101) peak in the XRD spectrum in Fig. 8), leading to decreased lateral homogeneity at the contact interface. The results suggest that the improvement of the contact properties with increasing annealing temperature should be attributed not only to the structural evolution of the Ni silicide and the formation of carbon vacancies near the semiconductor/contact interface, but also to an increase of the effective contact area. This interpretation is in agreement with the findings in [34], where the homogeneity of Ni/4*H*-SiC Schottky barriers was investigated as a function of annealing temperature. In that case a degradation of the Schottky contact was observed after annealing at 950°C, which was attributed to the formation of small low-barrier patches that add a strong contribution to the total current density at low biases [35]. Together, these results may serve as an explanation to the Schottky to Ohmic transition normally observed after high temperature annealing of Ni-silicide/SiC systems in the high doping range [33].

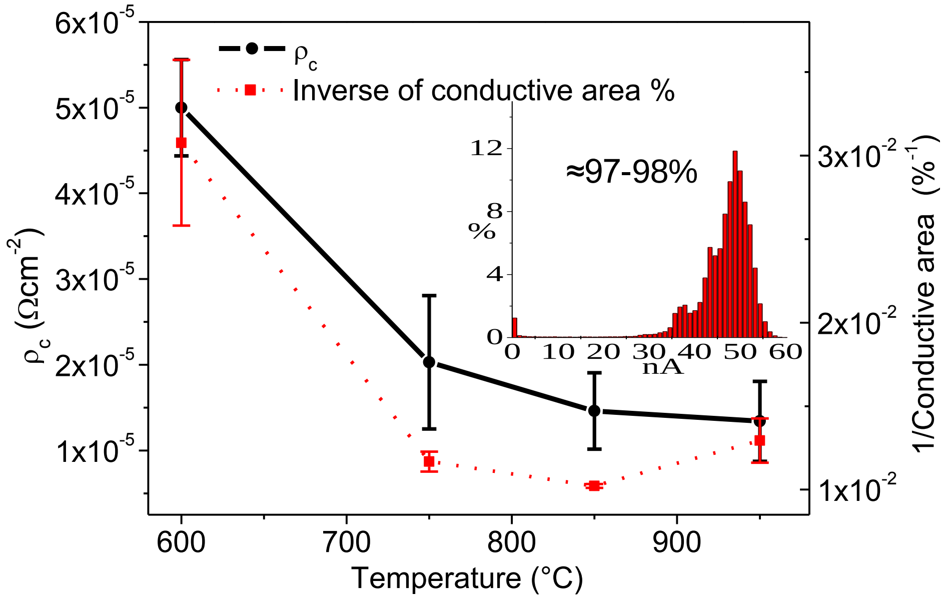


Figure 12. Trends of the inverse of the effective contact area (dotted curve) and specific contact resistance (solid curve) as a function of annealing temperature. The inset shows the statistical distribution of current in a current map obtained after RTA at 850°C, from which the effective area percentage was calculated.

2.4 Closing remarks

In conclusion, the structural and electrical evolution of a Ni/3*C*-SiC system with respect to annealing temperature studied in this thesis has allowed the visualization of a new aspect concerning Ni-based Ohmic contacts to SiC. Specifically, an increased uniformity of the local current distribution was observed with increasing annealing temperature, indicating that an increase of the effective contact area contributes to the improvement of the contact properties. A correlation between the annealing process and the electrical characteristics has been found in both the macroscale TLM measurements and the nanoscale C-AFM measurements. By increasing the annealing temperature from 600°C to 950°C, a gradual improvement was observed in the uniformity of the nanoscale current distribution, accompanying the gradual improvement of the structural homogeneity of the contacts observed by XRD. After this evolution, the specific contact resistance was reduced to 1.5×10^{-5} Ωcm^2. In light of the high roughness and the relatively low doping of the grown layer, the low experimental value of the specific contact resistance hints towards very high crystal quality of the single-domain 3*C*-SiC film grown by the VLS mechanism.

Even though the technological applications of 3*C*-SiC are beyond the scope of this thesis, these results are promising from a technological point of view. It has been demonstrated that high-frequency and high-power SiC electronics devices, particularly those in which a high current density flows horizontally, need to have Ohmic contacts with ρ_c values in the range 10^{-5}-10^{-6} Ωcm^2 [35,36]. Here, ρ_c values within this range were measured already on an as-prepared and rather rough 3*C*-SiC surface. Further improvement of the contact properties should be obtained upon a surface smoothing by CMP. Moreover, the doping concentration in the VLS grown layer was determined to be in the range $N_D = 3\text{-}6 \times 10^{17}$ cm^{-3}, whereas good Ohmic contacts should ideally be formed to semiconductor areas with doping concentrations $> 10^{19}$ cm^{-3}, in order to be in the field emission regime and ensure the formation of a tunneling Ohmic contact. Increasing the doping concentration by ion-implantation would surely reduce the width of the energy barrier and increase the tunneling current, leading to a reduced specific contact resistance. This leads to the conclusion that the formation of good Ohmic contacts to 3*C*-SiC films grown by the VLS mechanism is most achievable, and that this is not something that will hamper technology development in 3*C*-SiC films grown by this technique.

2.5 References

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Chapter 3

Nanoscale transport properties at 3*C*-SiC Schottky interfaces

Throughout the history of SiC electronic devices, due both to the limited material quality and processing issues, Schottky contacts to hexagonal SiC have exhibited non-ideal current–voltage characteristics (*I–V)*, often with large differences between individual devices. Even if the material quality has significantly improved in recent years, the control and reproducibility of the electrical properties of Schottky barriers is still considered as a key issue. More critical is the situation in cubic 3C-SiC, which is still characterized by a high density of defects, order of magnitudes higher than in hexagonal SiC. Indeed, one of the main obstacles that stand in the way of device fabrication in 3*C*-SiC is the formation of reliable rectifying contacts, with ideal characteristics and low leakage current values. Therefore, it is very important to understand the nature of the non-ideal behavior and to determine how the material quality and/or different surface preparations influence carrier transport through the metal-semiconductor interface.

This chapter will start with a description of the measurement techniques normally used to characterize Schottky diodes and the methods used to extract the diode parameters. Then, common causes of the non-ideal behavior will be presented, reviewing which role nanoscale non-idealities at the contact interface play on the macroscale diode behavior. Recent advances in the nanoscale characterization and control of Schottky interfaces in SiC will also be discussed. The bulk of this chapter will deal with how different types of defects affect the nanoscale electrical properties of 3*C*-SiC epitaxial layers, as well as the Schottky barrier formed between Au, Pt, and Pt_2Si and the semiconductor surface. The electrical activity of various defects and their role in the behavior of fabricated Schottky diodes were studied by local current mapping and current-spectroscopy using C-AFM and the scanning spreading resistance microscopy (SSRM) module. This allowed visualization of the behavior of defects from the nanoscale to the device level.

3.1 Schottky barrier diodes

Schottky barrier diodes are unipolar rectifying metal-semiconductor junctions, i.e., they do not inject minority carriers into a neutral region, as do *p*-*n* diodes. Consequently, Schottky barrier diodes do not store minority carriers when they are forward biased, and the reverse current transient is negligible. What little reverse recovery time they may exhibit is primarily dictated by their capacitance rather than minority carrier recombination as in conventional *p*-*n* junction rectifiers. This allows high frequency and low switching loss. Schottky rectifiers have been used for over 25 years in the power supply industry. The primary advantages are very low forward voltage drop and switching speeds that approach zero time making them ideal for output stages of switching power supplies.

3.1.1 Determination of diode parameters

As described in chapter 2, the Schottky barrier height Φ_B is the most important parameter for a metal-semiconductor contact. Another parameter that is very important for Schottky barrier diodes is ideality factor n [1]. The ideality factor incorporates all those unknown effects that make the device stray from the ideal behavior. For example, a Schottky diode is unlikely to be uniform over its entire area; localized low barrier height patches lead the *I*-*V* characteristics to deviate from the thermionic mechanism [2]. There are a few methods to determine the barrier height of metal-semiconductor contacts [3]. Current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) methods are among the most common electrical techniques for barrier height determination. One tacit assumption in using these measurement techniques is that the Schottky interface under investigation is homogeneous. Of course, in a real contact this is not the case, e.g. a large surface roughness or structural defects reaching the semiconductor surface can lead to localized barrier lowering and increased leakage currents [2,4-6].

3.1.1.1 Current-voltage (*I*-*V*) measurements

In an *I*-*V* experiment, the junction current is measured as a function of applied bias voltage. From a plot of the natural logarithm of the forward-bias current (Fig. 1), the Schottky barrier height Φ_B and the ideality factor n can be determined.

According to chapter 2 (section 2.1), in the case of moderately or low doped semiconductors, the current transport through the Schottky junctions is dominated by thermionic emission of majority carriers over the potential barrier from the semiconductor into the metal contact. For an intimate metal-semiconductor interface the current across the Schottky barrier can, in the ideal case, be described by thermionic emission theory [7] according to

$$I \ = AA^{*}T^{2}e^{-\frac{q\phi_B}{kT}}\left(e^{\frac{qV}{nkT}}-1\right) \tag{1}$$

where A^* is the Richardson's constant for the semiconductor, A is the diode contact area, q is the elementary charge, T is the absolute temperature, k is the Boltzmann constant, n is the ideality factor and Φ_B is the barrier height. Actually, in real Schottky diodes the thermionic emission theory only describes the forward *I-V* characteristic for a limited range of current densities. At higher diode currents, deviations from the ideal characteristics are observed due to the series resistance contribution from the drift region, the substrate and the back contact resistances, and the spreading resistance of the Schottky metal, resulting in a roll-over of the forward *I-V* characteristic (Fig. 1a) [8-10].

It is often convenient to write Eq. 1 in the form

$$I = I_S\left(e^{\frac{qV}{nkT}}-1\right) \tag{2}$$

where I_S is the saturation current, which can be extrapolated from a semi logarithmic plot of I versus V, as illustrated in Fig. 1a. The diode saturation current is related to Φ_B by

$$I_S = A^{*}T^{2}e^{-\frac{\phi_B}{kT}} \tag{3}$$

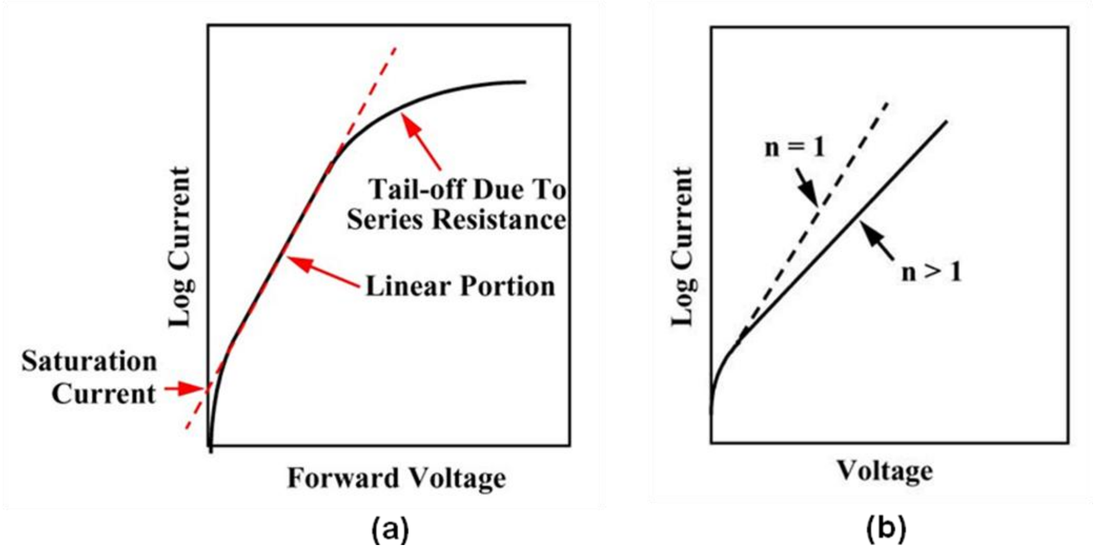

Figure 1. ***I-V*** **curves of a typical Schottky diode showing the extrapolation of the saturation current and the roll-over due to the series resistance (a), and the influence of the ideality factor on the forward current (b). Figure taken from [11].**

The barrier height is then evaluated by extrapolating the value of I_s from the linear region in the ln(*I*) versus *V* plot, and is given by

$$\phi_B = \frac{kT}{q}\ln\left(\frac{I_s}{A^*T^2}\right) \tag{4}$$

In this study, the value of the Richardson's constant A^* for of 3*C*-SiC is assumed as 194.1A/cm^2/K^2. [12].

The ideality factor *n*, instead, is determined from the slope of the linear region (the slope gives q/nkT).

3.1.1.2 Capacitance-voltage (*C-V*) measurements

The barrier height can also be extracted from capacitance-voltage (*C-V*) measurements. In this case no current is passed through the diode. The high frequency (> 500 kHz) capacitance of uniformly-doped Schottky diodes is measured as a function of the applied bias voltage. These measurements are usually done in the reverse bias to reduce the influence of the in-phase current on the measurement. The capacitance per unit area is given by

$$C = \sqrt{\frac{q\varepsilon\varepsilon_0 N_D}{2(V + V_{bi})}} \tag{5}$$

where N_D is the density of ionized doping centres in the material, $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the permittivity of vacuum, ε is the dielectric constant of the material, and V_{bi} is the so called *built-in potential,* which occurs due to the band bending in the semiconductor near the interface [13]. Eq. 5 represents the basis for *C*-*V* measurements. Fig. 2 shows the ideal $1/C^2$ curve as a function of the applied reverse bias for an *n*-type semiconductor. A completely linear curve corresponds to uniform depth distribution of free carriers. The donor concentration can be determined from the slope of the curve, while the extrapolation of the condition $1/C^2 = 0$, which is the intercept with the *x* axis gives V_{bi}, which is related to the value of the barrier height through Eq. 6:

$$\phi_B = V_{bi} + \xi + \frac{kT}{q} + \Delta\phi \tag{6}$$

where ξ is the difference between the Fermi level and the conduction band minimum for a neutral semiconductor, and $\Delta\Phi$ the image force lowering of the barrier height at the interface.

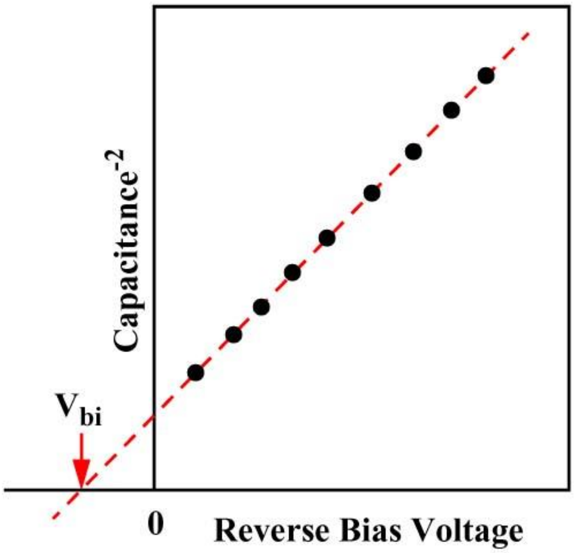

Figure 2. Typical $1/C^2$–V curve. The built-in potential is given for the condition $1/C^2 = 0$. Figure taken from [11].

3.1.2 Non-ideal Schottky diode behavior in SiC

There are several possible reasons that the behavior of the diodes stay from the ideal. The electrical behavior of the Schottky contact has been observed to be strongly dependent on the quality of the metal-semiconductor interface [14]. Inhomogeneities, structural defects, surface states and/or residual processing-induced contaminations in the interfacial region are commonly the reason for deviations from the ideal behavior in the electrical characteristics of Schottky contacts to SiC.

As discussed in 2.1, the Schottky-Mott theory proposes that Φ_B depends sensitively on the work function of the metal, Φ_m, according to

$$\Phi_B = \Phi_m - \chi_s \tag{7}$$

where χ_s is the semiconductor electron affinity. However, this prediction has received little support from experiment. The barrier heights measured in actual experiments often showed some dependence on the preparation of the metal-semiconductor interface, which indicates that Φ_B depends on more than just the work function of the metal. The dependence of Φ_B on Φ_m for 3*C*-SiC, 4*H*-SiC and 6*H*-SiC, extracted based on the *I*-*V* technique, was reported in [15]. The reported Φ_B values are systematically lower for cubic SiC than for the hexagonal polytypes, which is related to the different values of electron affinity, 4.0 eV in 3*C*-SiC, 3.5 eV in 6*H*-SiC and 3.1 eV in 4*H*-SiC [15,16]. Moreover, despite some scatters in the experimental data, by and large, metals with larger work functions have been found to have systematically higher barriers than those with lower work functions. The observed dependence, though, is much weaker than that predicted by the Schottky-Mott theory.

In order to explain the deviation from the ideal behavior observed in metal/SiC contacts, some other model than the Schottky-Mott one is needed. One explanation could be that carrier transport takes place through field emission or thermionic field emission mechanisms. However, as discussed in 2.1, the governing transport mechanism is determined by the doping level, which is normally below 5×10^{16} cm^{-3} for Schottky diodes in *n*-type SiC. This means that forward bias tunneling through the barrier is very improbable. On the other hand, barrier inhomogeneities due to interface damage and interfacial layers all tend to raise *n* above unity.

3.1.2.1 Fermi level pinning

The term *Fermi level pinning* has often been used to describe the insensitivity of the experimentally measured barrier heights towards the metal work function. From the very beginning of Schottky barrier studies, the Φ_B values for a wide range of metals on a particular semiconductor were found to fall within a narrow range. This range was so narrow that an empirical "one-third" rule was established; stating that Φ_B always appeared at roughly 1/3 of the bandgap for *p*-type material, and at roughly 2/3 of the bandgap for *n*-type material. Thus, the Fermi level appeared to be fixed, or "pinned", at $E_g/3$, from the valence band maximum. However, subsequent experiments showed that the one-third rule was not obeyed by the majority of metal-semiconductor systems. So, this rule was only part of a larger picture. Surface states in that part of the bandgap were speculated to be the source of the pinning effect. Pinning due to defects in the semiconductor is another possibility [17]. Some structural defects in semiconductors are known to have electric activities deep in the bandgap. If a high density of electrically active defects is present anywhere in the semiconductor, the local Fermi level can be pinned at a level close to the energetic position of the defects.

The slope of the Φ_B versus Φ_m is called the *interface index S*. This parameter gives an indication on the ideality of Schottky contacts. $S = 1$ corresponds to pure Schottky–

Mott behavior, whereas $S = 0$ corresponds to complete Fermi level pinning. In this latter case, the carrier transport properties are determined by interface states or defects, independently of the metal [18]. This condition is known as the Bardeen limit [19], and the barrier height is given by $\Phi_B = E_g - \Phi_0$, where Φ_0 is the energy level of the interface states or defects responsible for the pinning. As reported in [15], the S values for 3*C*-SiC, 4*H*-SiC and 6*H*-SiC have been found as 0.32, 0.41 and 0.40, respectively.

3.1.2.2 Nanoscale inhomogeneity of Schottky barriers on SiC

An accurate approach to describe the non-ideal behavior of a metal-semiconductor contact is the Tung's model [2]. This model considers the presence of a distribution of nanometer-size "patches" with a lower barrier height embedded in a uniform high barrier background. The presence of these low barrier patches may translate into an anomalous *I-V* behavior, which is often characterized by an excess of forward current at low-voltage levels. For circular patches of low Φ_B embedded in a region of higher Φ_{B_0}, the ideality factor n and the effective barrier height Φ_{eff} can be modeled according to [20]:

$$n = 1 + \frac{\gamma}{3\eta^{\frac{1}{3}} V^{\frac{2}{3}}{}_{bb}} \tag{8}$$

$$\phi_{eff} = \phi_{B_0} - \gamma \left(\frac{V_{bi}}{\eta} \right)^{\frac{1}{3}} \tag{9}$$

where $\eta = \varepsilon_r / qN_D$ and ε_r is the permittivity of the semiconductor, while γ is a parameter that describes the lateral size and the barrier height of a single patch [20]. Eqs. 8 and 9 show that a nanoscale lateral distribution of low Schottky barrier patches leads to non-ideal behavior ($n > 1$) and a lowering of the barrier height (Φ_{eff}) compared to the theoretical one (Φ_{B0}).

Using Tung's formalism has helped to explain several irregularities in the electrical behavior of Schottky contacts to SiC. For example, a consequence of the existence of these low barrier patches is that the effective area involved in the current transport may be significantly smaller than the geometric area of the contact. This, in turn, can serve as an explanation for the underestimation of the Richardson's constant in SiC commonly found among the values reported in literature [21]. This formalism has also been used to explain the temperature dependence of Φ_B and n, by showing that current flow through the high barrier regions becomes dominant at high temperatures, leading to a high Φ_B value and an ideality factor close to unity [21]. Conversely, at lower temperatures, electrons only have enough energy to overcome the lower barrier patches, leading to an increase in n and a lowering of the barrier.

Another important nanoscale issue for the properties of the Schottky barrier is surface preparation and post-deposition annealing [22-28]. The presence of surface roughness, interfacial contaminants, and residual thin oxide layers influence the uniformity of the Schottky barrier by causing low barrier patches. Moreover, electrically active structural and/or point defects near the interface or in the bulk can provide localized barrier height reduction and preferential paths for leakage currents [29]. The influence of such defects can be abated by e.g. a sacrificial oxidation to obtain a clean surface, or a passivation that heals surface defect states, as will be discussed in sections 3.2.4 and 3.2.6.

Recent advances have been accomplished in this field owing to the development of novel techniques, enabling the local transport properties to be determined with nanoscale spatial resolution [30]. For example, the influence of a thin residual oxide layer on the barrier uniformity at Au/6*H*-SiC interfaces was recently studied by local barrier height mapping performed using C-AFM. This approach allowed determination of Φ_B with a spatial resolution determined by the SPM tip diameter (≈ 40 nm), which in turn allowed demonstration of better lateral homogeneity at the interface without the residual oxide [31]. This result demonstrates that nanoscale control of SiC surfaces is an essential tool on the ways towards ideal behavior.

3.2 Rectifying contacts to 3*C*-SiC

One of the main obstacles that stand in the way of device fabrication in 3*C*-SiC is the formation of reliable rectifying contacts (*p*-*n* or Schottky junctions), with ideal characteristics and low leakage current values.

Many studies have used gold (Au), which is nonreactive with C and Si, as Schottky contact material to *n*-type 3*C*-SiC [32]. Because of its high metal work function (5.47 eV), Au is expected to form a Schottky barrier height (Φ_B) of about 1.47 eV on *n*-type 3*C*-SiC, assuming Schottky-Mott behavior and an electron affinity of 3*C*-SiC of 4.0 eV [33,34]. However, surface states related to material defects lead to low experimentally measured values [12,35-39]. Table I summarizes experimentally observed Schottky barrier height values reported in the literature for various metal contacts to 3*C*-SiC epilayers grown on different substrates, extracted using different techniques. As seen, high barrier heights have been extracted only from capacitance-voltage (*C*-*V*) measurements where no current passes across the barrier. However, the use of this method can effectively mask any detrimental effects of leakage currents due to conductive extended defects present in the semiconductor material and/or barrier inhomogeneities. On contrast, for current-voltage (*I*-*V*) measurements the extracted barrier height values can be affected by preferential leakage current conduction through extended defects like e.g. stacking faults or dislocations [40,41].

Table 1. Literature summary of Schottky barrier height values for metal/3*C*-SiC interfaces.

Metal	3*C*-SiC surface	Substrate	Φ_B (eV)	Method	Ref.
Au	(100)	Si	1.15-1.2	C-V	35
Pt	(111), (100)	Si	1.3-1.8	C-V	36
Au			1.0-1.6		
Pt + (800°C)	(100)	Si	0.95 (1.35)	C-V	37
Pd	(100)	Si	0.95, 0.92	C-V, XPS	38
Au			0.78, 0.87		
Co			0.69, 0.73		
Ti			0.53		
Ag			0.4		
Tb			0.35		
Al			0.16		
Au	(100)	Si	1.11, 1.15	C-V, photoresponse	39
Ti	(100)	3*C*-SiC	N/A, 0.4	C-V, I-V	12
Au			0.65, 0.67		
Ni			0.54, 0.56		

Large concentrations of stacking faults, associated with the low stacking fault formation energy for this polytype [42], as well as twins and screw dislocations occurring in heteroepitaxial films have so far hindered the achievement of the predicted electrical properties in 3*C*-SiC, both within the semiconductor substrate and at the metal/SiC interface [32]. Das *et al.* [43] used temperature dependent *I-V* characterization of 3*C*-SiC grown on different substrates to reveal information related to the deep states present in the material, demonstrating the degrading effects of defects on electrical properties in 3*C*-SiC substrates. Further, Tan *et al.* [44] used *I-V* analysis to obtain information pertaining to the electrically active defects in 3*C*-SiC films, and the active defects were attributed to stacking faults and point defects and contribute to traps at ~ 0.656 eV below the conduction band edge. While the possibility of fabricating 3*C*-SiC MOSFETs with excellent on-state characteristics has been demonstrated [45,46], the same studies also indicated that a significant reduction of the stacking fault density is required in order to achieve acceptable blocking voltage values and off-state leakage currents. Consequently, it is imperative to better understand the role of specific material defects and how their detrimental influence on devices can be abated.

Recently, Song *et al*. demonstrated the intense electrical activity of unindividuated extended defects in 3*C*–SiC, proving that they behave as through layer connections for leakage currents [47].

In this chapter, the focus is on how different types of defects affect the nanoscale electrical properties of 3*C*-SiC epitaxial layers, as well as the Schottky barrier formed between Au, Pt, and Pt_2Si and the semiconductor surface. A better understanding of the deviation from ideal Schottky behavior was sought by studying the correlation between the transport properties of 3*C*-SiC Schottky barrier diodes and the specific crystal defects in 3*C*-SiC epilayers grown using different techniques and on different substrates ([001] 3*C*-SiC and [0001] α-SiC). Defects were studied and quantified by transmission electron microscopy (TEM) and conductive atomic force microscopy (C-AFM), and a method based on C-AFM [40] was used to study how the defects influence the conduction across the barrier. The effects of an ultraviolet (UV) irradiation treatment on the nanoscale electrical behavior of the defects and the overall performance of the devices were also studied. Also the effect of contact formation through interface reaction was studied for the Pt/3*C*-SiC system, which reacts to form Pt silicides upon high temperature annealing. Depending on defect density, surface treatment and contact area, Schottky barrier height values between 0.3 and 1.4 eV were found. The results can help elucidate which are the device-limiting defects in 3*C*-SiC and to which extent they need to be reduced to reach device maturity.

3.2.1 Experimental

3*C*-SiC (111) heteroepitaxial layers were grown onto (0001) 4*H*- and 6*H*-SiC substrates using a chlorine based chemical vapor deposition (CVD) process [48] (sample A) and a vapor-liquid-solid (VLS) mechanism [49] (sample B), respectively. Homoepitaxial layers were grown in the (100) direction onto 3*C*-SiC substrates using continuous feed physical vapor transport (CF-PVT) [50] (sample C) and in the (001) direction by CVD (samples D and E) [51].

Before metallization all samples were cleaned by etching for 5 min in $H_2SO_4 : H_2O_2$ = 3 : 1 solution followed by 5 min of etching in HF : H_2O = 1 : 10 solution. Then, Ohmic back contacts were formed by evaporation of a 100 nm thick layer of Ni and a subsequent rapid annealing step at 950°C for 60 seconds to form nickel silicide [52,53]. The samples were then subjected to an ultraviolet (UV)-irradiation treatment at 200°C, in order to electrically passivate carbon related defect states at the surface [54,55]. Front contacts to samples A, B, C and D were then formed by sputter deposition of a 100 nm thick Au film, and circular contacts with radii in the range 5-150 µm were defined by optical lithography and wet etching. Sample E was additionally cut into four pieces, and front contacts were formed by sputter deposition of an 80 nm thick Pt film, and circular contacts with radii from 10 to 150 µm were defined by a lift-off process. The fabricated Pt diodes were then annealed for 5 minutes at 500°C, 700°C and 950°C in argon ambient and the structural evolution of the contacts was monitored by X-ray diffraction (XRD) as described in chapter 2 (section 2.3). A schematic of the fabricated Schottky diodes and the measurement setup is presented in Fig. 3.

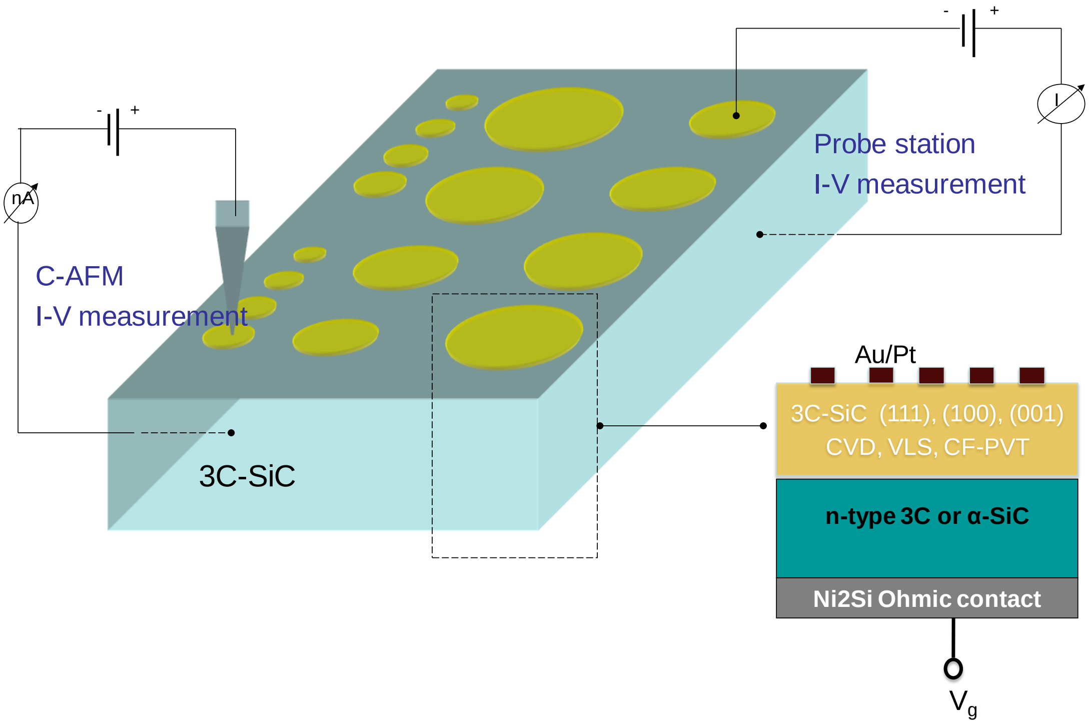
- +
nA
C-AFM
I-V measurement
3C-SiC
- +
I
Probe station
I-V measurement
Au/Pt
3C-SiC (111), (100), (001)
CVD, VLS, CF-PVT
n-type 3C or α-SiC
Ni2Si Ohmic contact
V_g

Figure 3. Illustration of the fabricated Schottky diode structures and the measurement approach.

The fabricated diodes were electrically characterized by current voltage (*I-V*) measurements in a Karl Süss electrical probe station, as well as by conductive atomic force microscopy (C-AFM) [56,57], performed using a Veeco DI dimension 3100, equipped with the nanoscope V electronics and the scanning spreading resistance (SSRM) module [58], which is essentially C-AFM with a logarithmic current amplifier that allows studying a wider range of current variations than what is possible using the normal C-AFM module. The use of C-AFM *I-V* probing was necessary since measurements using conventional probes were not possible on the smaller contacts (radius of less than 20 µm).

The physical parameters describing the Au/3*C*-SiC contacts were extracted from *I-V* measurements using thermionic emission theory [7]. The nanometric dimension of the scanning probe tip (the tip radius is ≈ 20 nm) could cause a lateral localization of the current across the metal-semiconductor interface, which would limit the diode area and make it difficult to determine the effective contact area, which would, in turn, render the extracted parameters unreliable. As demonstrated by Giannazzo *et al*. [56], the nanometric localization of the current can occur due to two physical reasons, the electric field localization at the apex of the biased conductive tip, and the high lateral resistivity of very thin metal films. The latter can be avoided by using a relatively thick metal layer, whereas the influence of the electric field localization has to be investigated by comparing *I*-*V* curves measured on the same diodes by C-AFM and in a normal electrical probe station.

Fig. 4 shows a comparison of *I*-*V* characteristics measured in an electrical probe station and by C-AFM probing. The curves were measured on the same Au/3*C*-SiC/4*H*-SiC/Ni_2Si vertical structures on diodes with a contact radius of 50 µm. As seen, the small dimension of the C-AFM tip increases the series resistance (affecting the forward saturation current) but does not affect the linear part of the ln(*I*) versus *V* curve. Since the linear region is the same for both sets of curves, this means that it is accurate to extract the Schottky barrier height from either type of measurement, since only the saturation current is interesting for the determination of the diode properties.

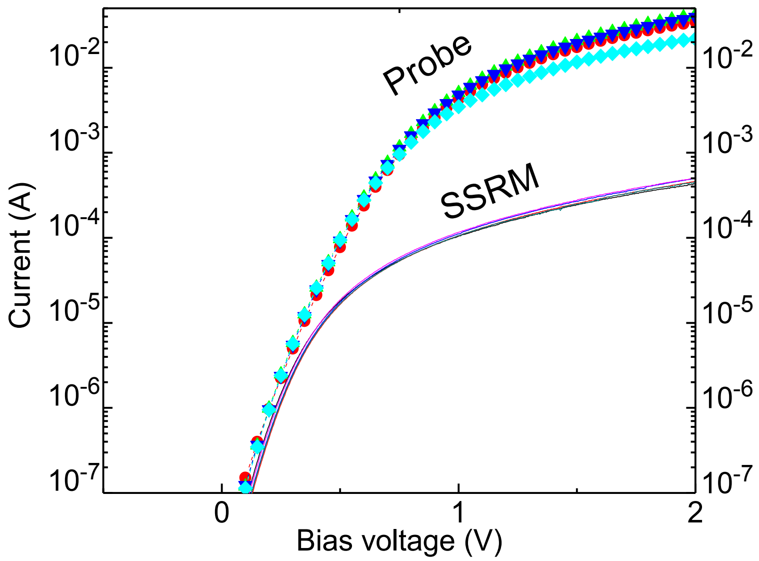

Figure 4. ln(*I*)-*V* characteristics of diodes with a contact radius of 50 µm, obtained from measurements in an electrical probe station and by C-AFM (with the SSRM module) measurements carried out on the same sample (sample D). As seen, the linear region of the ln(*I*)-*V* curves is the same for both types of measurements.

Optical microscopy and AFM were used to study the morphology and surface roughness of the 3*C*-SiC epilayers. Structural defects arriving at the semiconductor surface were systematically investigated by studying conductivity changes on the 3*C*-SiC surface by local current measurements using C-AFM. The C-AFM setup allowed the simultaneous acquisition of surface morphology and current distribution by scanning a biased conductive tip in contact mode on the sample surface. Diamond-coated Si tips were used due to their excellent mechanical and electrical stability [56,59]. The microstructure and quality of the 3*C*-SiC layers were further investigated by transmission electron microscopy (TEM), both in plan-view and in cross-section view. TEM analysis was carried out after mechanical thinning and a final ion milling at low energy (5 keV Ar ions). Bright field images were recorded at 2-20 kV by a JEOL 2010F microscope equipped with the Gatan imaging filter.

3.2.2 Non-ideal behavior of 3*C*-SiC Schottky interfaces

A key factor for the conduction properties through a contact is the quality of the metal-semiconductor interface, e.g. a large surface roughness or structural defects reaching the semiconductor surface can lead to localized barrier lowering and increased leakage currents [41,60,61]. As an example, as observed in other wide bandgap semiconductor materials [41], defects can behave like preferential leakage current paths through the layer. It has recently been shown by SSRM measurements, performed in cross-section, that extended defects in 3*C*-SiC cause a localized lowering of the resistance through the layer [47]. Moreover, defects like dislocations, SFs, double positioning boundaries (DPBs) and microtwins have previously been identified as responsible for increasing the leakage currents and decreasing the Φ_B values specifically for Schottky diodes on 3*C*-SiC [40,62]. As a consequence, the crystalline quality of the 3*C*-SiC epilayer is pivotal for good device operation.

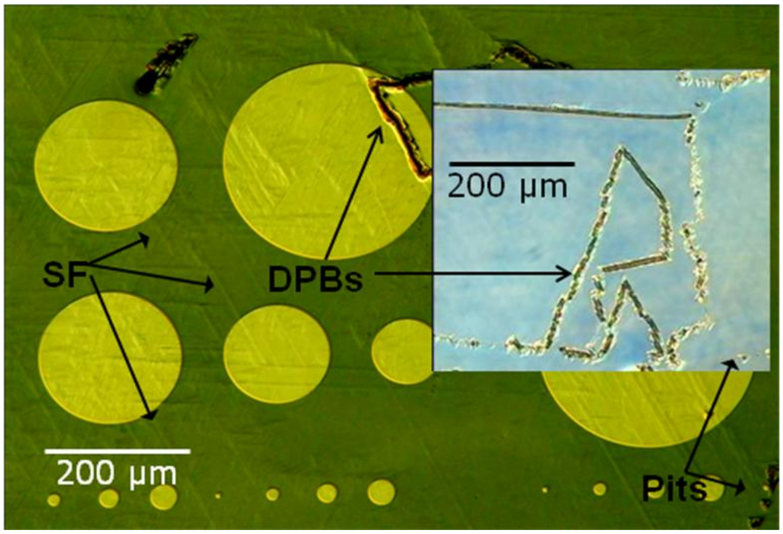

Figure 5. Optical microscopy showing the surface of the 3*C*-SiC on sample A, with patterned Au contacts. The visible defects include DPBs, SFs, and triangular pits. The inset shows a Nomarski microscope image of the semiconductor surface taken before metallization.

The optical microscopy reported in Fig. 5 shows the front (3*C*-SiC) side of sample A, where the circles are the fabricated Au contacts. Also various extended defects are visible, like SFs, triangular pits (due to screw dislocations reaching the surface) and DPBs. The current-voltage behavior is strongly influenced not only by the presence of defects under the contact, but also by the type of defect. As can be seen from the *I*-*V* curves in Fig. 6, DPBs typically result in large leakage currents and/or even Ohmic behaviors. Hence, these DPBs can be considered as 'killer defects' for the Schottky contact.

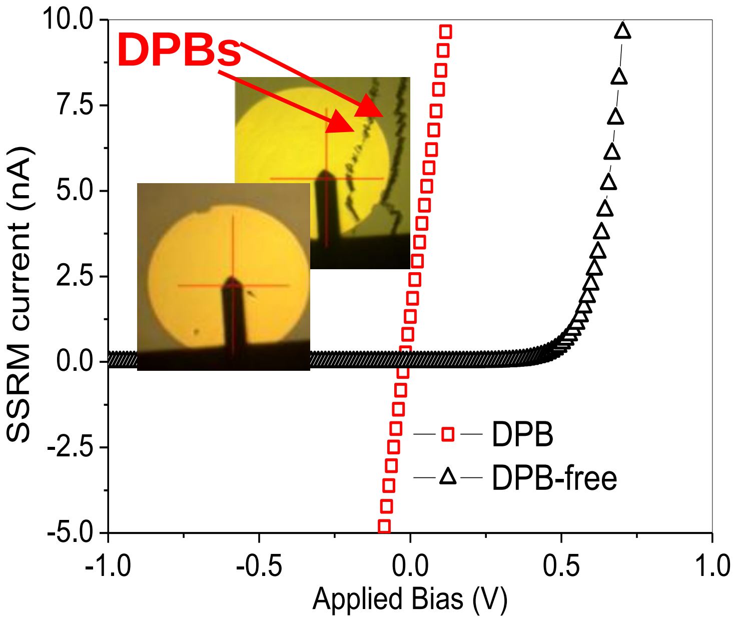

Figure 6. ***I-V* curves measured by C-AFM (with the SSRM module) on diodes with a contact radius of 150 µm, with and without the presence of a double positioning boundary defect. The DPB provides a preferential current path through the semiconductor that effectively destroys the rectifying properties of the contact.**

Consequently, these types of defects must be avoided, and hereafter the investigation will be limited to diodes free from DPBs.

Fig. 7 shows a comparison of the barrier height values extracted from *I-V* and *C-V* measurements on sample A. The barrier height is presented as a function of contact radius. The obtained ideality factors were just below 2. The value of the barrier height Φ_B obtained from *C-V* measurements depends on the built-in potential and the width of the depletion region [7], and is often ascribed to the ideal barrier height. As seen, *C-V* measurements resulted in higher values of the Schottky barrier heights than those extracted from *I-V* measurements, demonstrating that the ideal barrier is higher than the one measured by *I-V*.

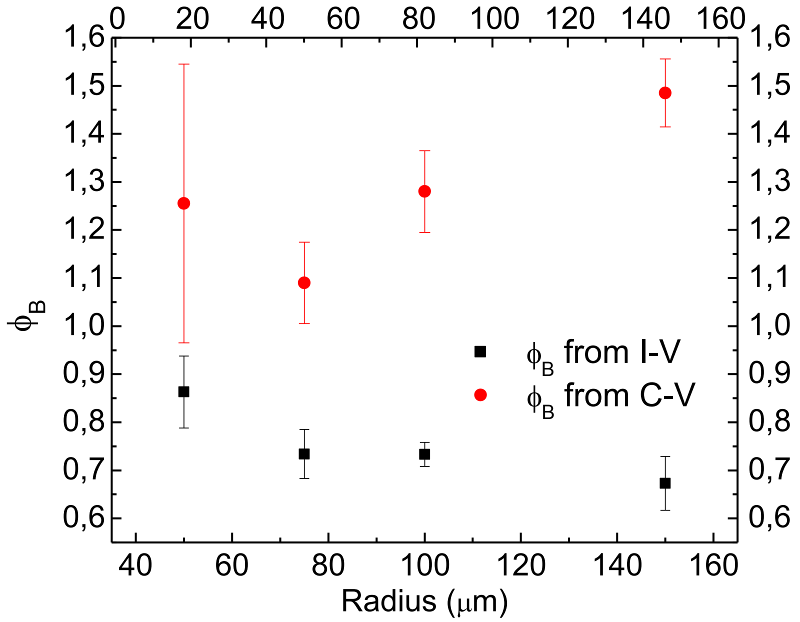

Figure 7. Schottky barrier heights versus contact radius measured for Sample A. The values were extracted from *I-V* (filled squares) and *C-V* (filled circles) measurements.

I-V characterization of the diodes analyzed in this work always resulted in non-ideal behavior, and the ideality factors varied from 1.1 (for very small diodes on the best material and after a surface treatment) to above 2. However, a strong improvement of the *I-V* behavior was observed after a UV irradiation of the semiconductor surface prior to metallization. These results suggest that the behavior of the diodes in general is strongly limited by defects at the contact interface, and that a partial passivation of some defects occur upon UV irradiation. Therefore, it is very important to understand the nature of this non-ideal behavior, investigating how the material quality and/or the surface preparations influence carrier transport through the interfaces.

3.2.3 Structural and electrical investigation of defects

As observed, DPBs are killer defects. On the other hand, though, they are both easily detected and relatively scarce, so their presence can be avoided. However, as seen in the bright field plan-view TEM images of sample A that are presented in Fig. 8a and Fig. 8b, upon closer inspection it is clear that the predominant type of extended defect in the epilayers investigated in this study is the stacking fault; the 60° angle between the dark lines in the micrograph indicates that these features are SFs arriving to the (111) surface. The SFs were found to originate from the 3*C*/4*H*-SiC interface, as can be noted in TEM image of the cross-section of the 3*C*/4*H*-SiC interface in Fig. 8c. While the SFs do not prevent the formation of a rectifying contact they can clearly influence the electrical properties of the epilayer and, consequently, of a contact formed on top of it. Moreover, it has previously been reported that microtwins in 3*C*-SiC grown in the (111) direction are visible as extra spots in the diffraction pattern in the (114) direction [63]. As seen in Fig. 8d, the diffraction pattern in the (114) direction shows a perfect singe crystal, where the absence of extra spots indicates no or very small amounts of microtwins in sample A.

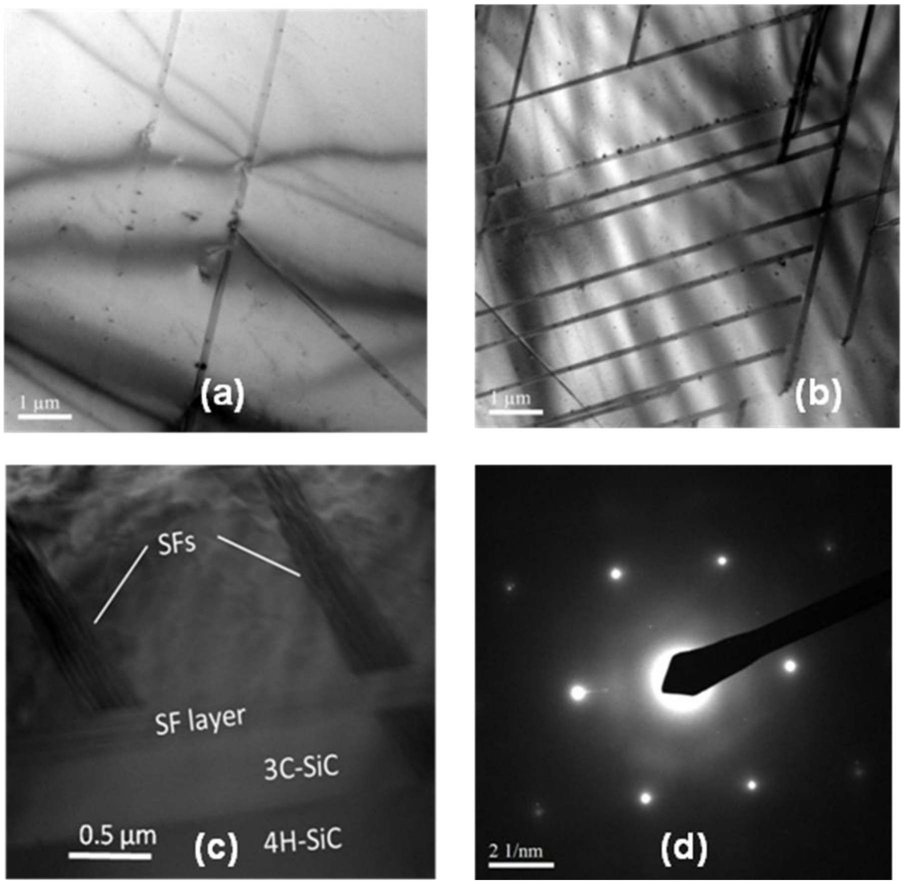

Figure 8. 8 × 8 μm plan-view transmission electron microscope images obtained in bright field condition on sample A, showing stacking faults arriving at the 3*C*-SiC (111) surface (a and b). As can be seen by comparing (a) and (b), large localized variations were observed in the stacking fault density. A cross-section TEM image of the 3*C*/4*H*-SiC interface is shown in (c), where SFs can be seen originating from the interface and propagating towards the 3*C*-SiC surface. The diffraction pattern in the (114) direction is shown in (d), where the absence of extra spots indicates no or very small amounts of microtwins.

The presence of extended defects that reach the semiconductor surface can worsen the behavior of a Schottky contact, especially in the case of electrically active defects. This latter particular aspect can be revealed in this thesis by C-AFM, where high conductivity areas in 2D current maps were identified at the defect location. Current maps of 50 × 50 μm^2 areas of the 3*C*-SiC surfaces of sample A and B, determined at a sample bias of -2V, are shown in Fig. 9. As can be seen in Fig. 9a, a preferential leakage current conduction through the SFs is observed, resulting in current peaks of around 1 pA, over a background of ≈ 50 fA. Fig. 9b and Fig. 9c show the current distribution in the presence of triangular pits and DPBs, respectively, illustrating that the leakage currents through both of these defects are significantly larger than through the SFs (by at least one order of magnitude.) Indeed, SFs are not visible in (b) and (c) due to the larger current scale.

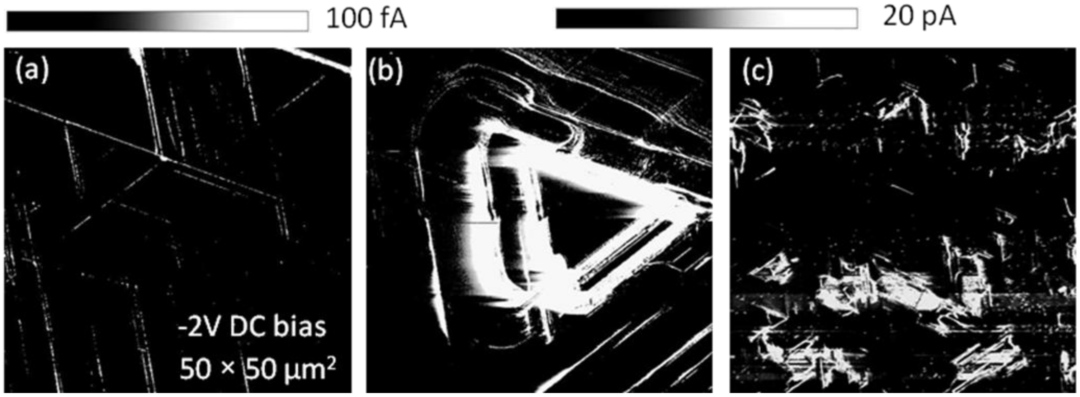

Figure 9. C-AFM current maps obtained over areas of 50 × 50 μm^2, showing conduction through SFs (a) and triangular pits (b) on sample A, as well as DPBs on sample B (c). SFs are not easily visible in (b) and (c) due to the larger current scale.

From multiple C-AFM-scans as the one in Fig. 9a, the statistical density of SFs, defined here as the ratio between the total lengths of all SFs in a micrograph and the scanning area, could be determined for the samples in this study. Table 2 summarizes the measured defect densities and the extracted Schottky barrier heights for Au contacts (determined from *I*-*V* measurements) for the four different types of 3*C*-SiC epilayers investigated in this study. The rightmost column specifies the average Φ_B values as the contact radius is reduced from 150 to 5 μm. The doping concentration N_D varied a bit from sample to sample but was always in the range from 3×10^{15} cm^{-3} to 5×10^{16} cm^{-3}, placing the conduction firmly in the thermionic emission regime (see section 2.1). Therefore, the doping concentration should not influence the Φ_B values extracted from Eq. 4. High defect densities and poor barrier height values are observed for all four types of layers. In particular, for sample B, where a large density of DPBs was observed, no rectifying *I*-*V* characteristics were obtained even when measuring on contacts with a radius of 5 μm (where the contribution of defects to the leakage currents should be minimal). The densities of the more pervasive SFs range from 3×10^4 cm^{-1} to 1×10^3 cm^{-1} for the studied samples. While these values seem high, the lowest SF densities are actually significantly better (by more than one order of magnitude for sample A) than what is normally obtained in 3*C*-SiC (111) layers grown on Si. However, these densities are surely high enough to guarantee that no contact will be free from SFs. It can be seen in Table 2 that as the presence of SFs is reduced, either by reducing the SF density or the contact area, the Schottky barrier height values gradually improve. From this result it is clear that these defects are indeed the most important device limiting defects in this material.

Table 2. Summary of the growth technique, substrate material, stacking fault densities and Schottky barrier height values for Au contacts, measured on the samples in this study. The rightmost column specifies the average Φ_B values, extracted from *I*-*V* measurements, as the contact radius is reduced from 150 to 5 µm. The values in parentheses correspond to results obtained after a UV-irradiation.

Growth technique	Substrate	Main defect	SF density (cm^{-1})	Φ_B (eV) *R*: 150-5 (µm)
CVD Sample A	4*H* (0001)	SF	$\approx 1 \times 10^3$	0.6-0.7 (0.7-1.4)
VLS Sample B	6*H* (0001)	SF, DPB	$\approx 3 \times 10^4$	N/A (Ohmic)
CF-PVT Sample C	3*C* (100)	SF	$\approx 1 \times 10^4$	0.3-0.6
CVD Sample D	3*C* (001)	SF	$\approx 3 \times 10^3$	0.5-0.7

3.2.4 Influence of UV-irradiation on the nanoscale electrical properties of the 3*C*-SiC surface

Given the pervasiveness of the SFs observed by TEM and C-AFM, it is clear that the presence of defects under the contacts is unavoidable, and consequently a process step that mitigates their detrimental influence was sought.

UV-irradiation/ozonization of SiC surfaces has been reported to eliminate surface defect states related to carbon due to oxidation [54,55]. We investigated if this could be utilized to electrically passivate the defects at the 3*C*-SiC surface by monitoring the effects of a near-surface oxidation treatment performed by UV-irradiation, during which ozone is generated. In other materials, i.e., gallium nitride, it has been reported that increased leakage currents arising from defects (specifically core dislocations) can be passivated by oxidation, significantly improving the device performance by reducing the leakage current values [64].

To study in what way UV irradiation affects the electrical activity of SFs and DPBs in 3*C*-SiC, a piece of the samples were subjected to a UV surface irradiation as described in the experimental section. Fig. 10 shows the morphology of the semiconductor surface of sample A along with the corresponding current maps, determined by C-AFM and measured over 50 × 50 μm^2 areas at 2 V reverse bias, before and after UV-irradiation. As seen, the SFs are barely visible in the current map determined on the UV-irradiated surface. Indeed, prior to irradiation current peaks in the range of a few pA (corresponding to current densities in the order of 100 mA/cm^2, assuming radius of tip curvature of 20 nm) are measured on the SFs (see insets in the current maps), whereas the irradiated surface shows no current variations exceeding 50 fA (current densities in the order of 4 mA/cm^2). Consequently, it is clear that the preferential current conduction on the SFs is significantly reduced by the treatment, and it is possible to conclude that the SFs have been electrically passivated.

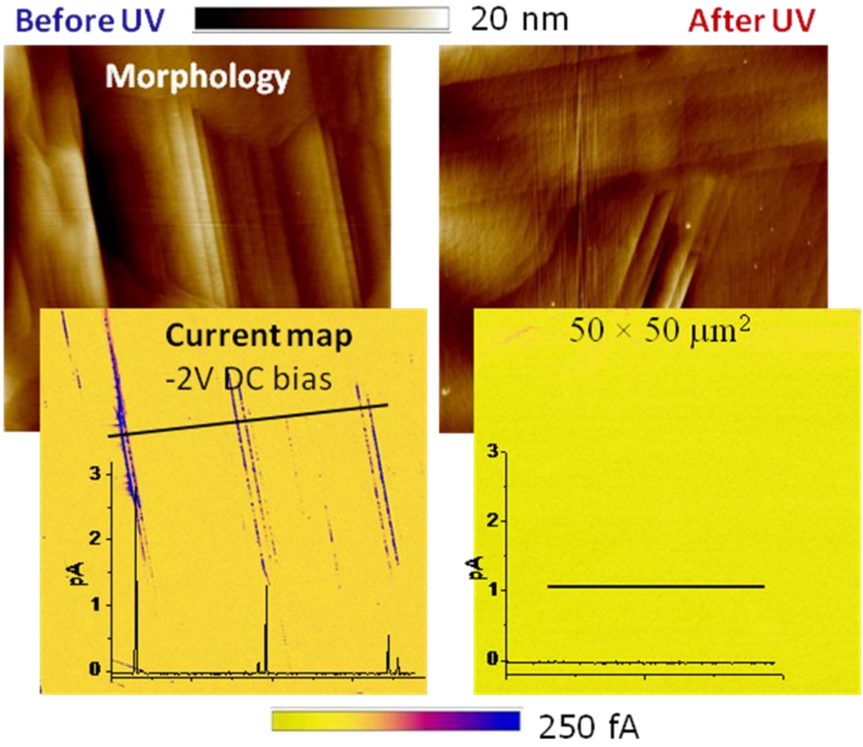

Figure 10. AFM morphology (top) and C-AFM current maps (bottom) measured on sample A at a reverse bias of 2 V, showing stacking faults visible on 50 × 50 µm^2 areas on the 3*C*-SiC surface before (left) and after (right) UV treatment. The insets in the current maps show how the current varies along the indicated lines, demonstrating that the leakage through the SFs has been notably reduced after the irradiation.

On contrast, UV irradiation has no mitigating effect on the leakage currents through DPBs, as seen in the morphology and current maps in Fig. 11, measured on sample B before and after the irradiation. While the SFs have been passivated also in this case, currents in the range of ≈ 10 pA are still measured on the DPBs at -2 V bias even after irradiation.

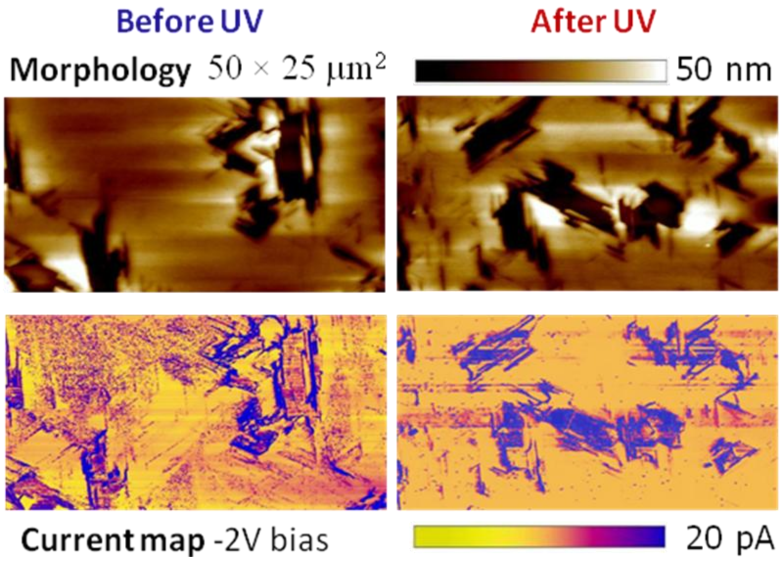

Figure 11. AFM morphology (top) and C-AFM current map (bottom) measured on sample B, at a reverse bias of 2 V. The micrographs were obtained before and after a UV-irradiation treatment, showing that, while the SFs are passivated, large leakage currents still pass through the DPBs.

3.2.5 Influence of UV-irradiation on the Au/3*C*-SiC Schottky interface

To evaluate how the passivation of the SFs affects the overall performance of the fabricated diodes, the changes in the characteristics of the Schottky contacts on sample A are illustrated in the *I*-*V* curves in Fig. 12, measured by SSRM on diodes with a contact radius of 20 μm before and after the treatment. As can be seen, strong improvements are observed under both forward (higher Φ_B value) and reverse (lower leakage current) conditions. Moreover, no significant reduction of the forward bias currents can be observed, showing that the passivation does not hamper the on-state operation of a device.

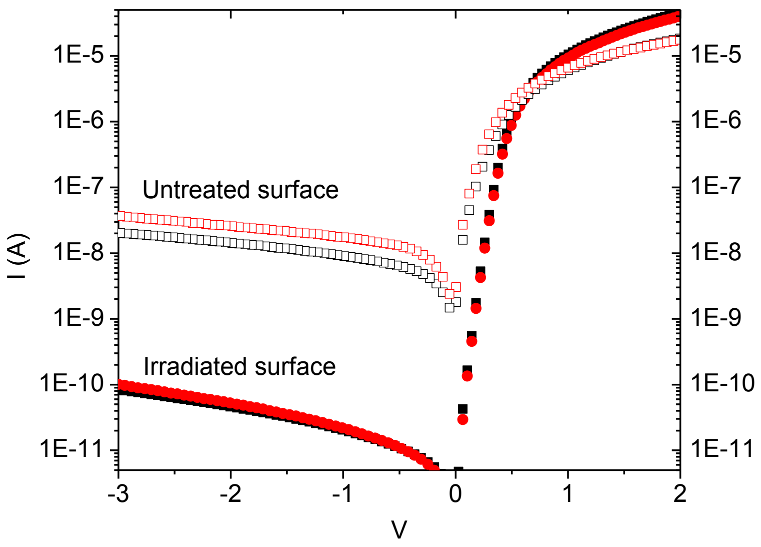

Figure 12. *I-V* characteristics measured by SSRM before and after the UV-irradiation on *R* = 20 µm diodes on sample A. The red and black curves were measured on different diodes.

Additionally, the experimental Φ_B values for sample A before and after UV-irradiation, measured on diodes free from DPBs, are plotted as a function of the contact radius in Fig. 13. In both cases, the ideality factor for the diodes with a contact radius between 75 and 150 µm is just below 2, and in this range the measured values of Φ_B are fairly independent of the contact area and are also significantly lower than the ideal value for the Au/3*C*-SiC interface, consistent with a large interface state density due to a high defect concentration underneath the contacts. This is likely due to low barrier patches forming near defective regions, affecting the current transport and, as a result, the average values of Φ_B determined by *I-V* [2]. When the contact area is reduced further, however, completely different trends are observed depending on the irradiation. For the non-irradiated surface only a slight dependence of Φ_B on the contact area is observed. On contrast, for the irradiated surface the Φ_B values improve considerably upon reducing the area, reaching a high value of 1.39 ± 0.20 eV for the smallest diodes with a contact radius of 5 µm. The lower barrier height values observed for the larger contacts can be attributed to increasing leakage currents flowing through the defective regions.

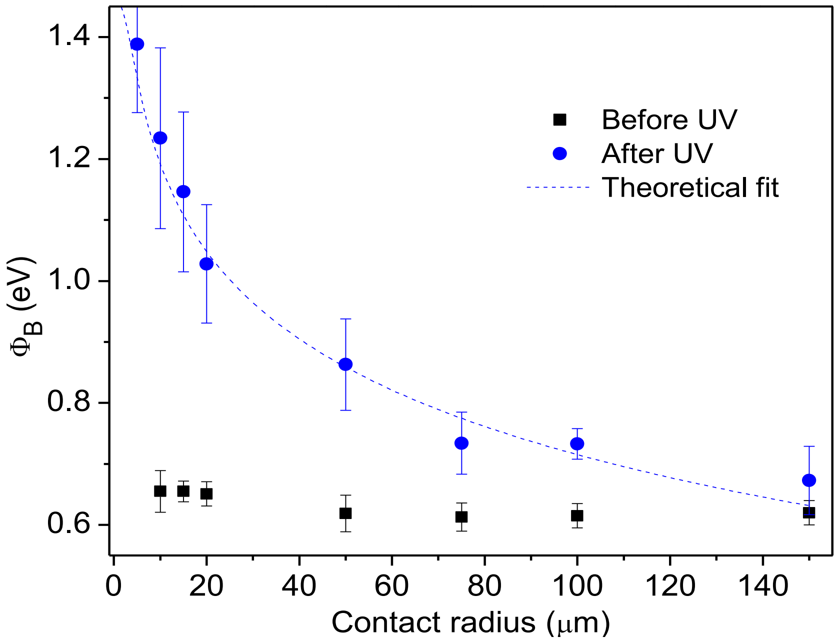

Figure 13. Schottky barrier heights versus contact radius for sample A before and after UV-treatment. The experimental Φ_B values (filled squares for the non-irradiated surface and filled circles for the irradiated one) were extracted from *I-V* measurements. The dashed curve corresponds to the modeled values obtained according to Eqs. 12 and 13, using 4.7 × 10^6 cm^{-2} as the value of the point defect density.

3.2.5.1 Contact area dependence of Φ_B

The high barrier height values measured on the smallest diodes after the passivation of the SFs demonstrates the possibility of fabricating functional Schottky diodes in 3*C*-SiC. However, the contact area dependence observed after irradiation leads to the conclusion that even after the passivation of the SFs there are still some electrically active defects contributing to deleterious leakage conduction, responsible for a worsening of the *I-V* characteristics of the larger diodes.

Starting from the yield formula discussed by Muller *et al*. [65] and using the thermionic emission theory, a model was developed to describe Φ_B as a function of the point defect density. A triangular modified Poisson distribution was considered. The resulting probability, *Y*(*D*), that a device is free from defects is given by

$$Y(D) = \left(\frac{1 - e^{-DA}}{DA} \right)^2 \tag{10}$$

where A is the area (in cm^2) of the diodes and D is the defect density (in cm^{-2}).

In our case, a reasonable starting point to define the yield is to base it on the ratio between the ideal and the experimental leakage currents, I_{LT} and I_{LE}, respectively. For I_{LE}, only the saturation current at 0V bias, extrapolated from the linear region of the forward bias ln(I) versus V curve, is considered, disregarding the effects of image force barrier lowering and voltage dependence under reverse bias. The resulting expression for the yield, according to TE, then becomes

$$Y(D) = \frac{I_{LT}}{I_{LE}} = \frac{A_T^*}{A_E^*} e^{\frac{-q(\phi_{BT} - \phi_{BE})}{kT}} \tag{11}$$

where Φ_{BT} and Φ_{BE} are the ideal and experimental barrier heights, while A_T^* and A_E^* are the theoretical and experimental Richardson's constants for the semiconductor, respectively. Hence, by combining Eq. 10 and Eq. 11, the experimental value of the Schottky barrier height Φ_{BE} can be analytically expressed as

$$\phi_{BE} = \phi_{BT} + \frac{kT}{q} \left[\ln\left(\frac{A_E^*}{A_T^*} \right) + 2 \ln\left(\frac{1 - e^{-DA}}{DA} \right) \right] \tag{12}$$

The experimentally measured values of the Richardson's constant are normally lower than what is predicted theoretically, which can be attributed to the presence of defect-induced low barrier patches [61]. This was accounted for by describing the ratio between the experimental and theoretical Richardson's constants by the same dependence that was used to describe the yield:

$$\frac{A_E^*}{A_T^*} = \left(\frac{1 - e^{-CA}}{CA} \right)^2 \tag{13}$$

where C is a scaling constant that was later found to be the same as the defect density, D. By inserting Eq. 13 into Eq. 12, using the value of $\Phi_{\mathrm{BT}} = 1.47$ eV, and assuming D

and *C* as fitting parameters, *C* and *D* were determined to be 4.71 × 10^6 cm^{-2} and 4.70 × 10^6 cm^{-2}, respectively, from the fit of the experimental data. The fact that the two constants have very similar values indicates that Eq. 13, by substituting *D* for *C*, describes a direct relation between A_E^* / A_T^* and the defect density. The fitted curve is plotted alongside the experimental values in Fig. 13.

3.2.6 Mechanism of SF passivation

As described in 3.2.4 and 3.2.5, a UV-irradiation treatment was found to suppress leakage currents through SFs but not DPBs. The observed passivation of the SFs could be due to the formation of a thin SiO_2 layer, caused by the ozonizing effect of the UV irradiation. However, this thin passivating layer is probably not continuous over the whole sample surface. In fact, patterning micrometric stripes by optical lithography and selective wet etch in hydrofluoric acid did not enable determination of the oxide thickness by AFM. On the other hand, UV-ozone treatment is known to remove surface defects in SiC related to carbon atoms due to oxidation [55], and SFs arriving at the 3*C*-SiC (111) have a C-termination [66]. Hence, the passivation of the SFs may result from a preferential oxidation occurring just on these defects, where the polarity is shifted with respect to the Si-terminated (111) surface, as imaged in Fig. 14. This interpretation is consistent with recent results that have shown that high temperature thermal oxidation of 3*C*-SiC (111) proceeds at a higher rate on the stacking faults [66].

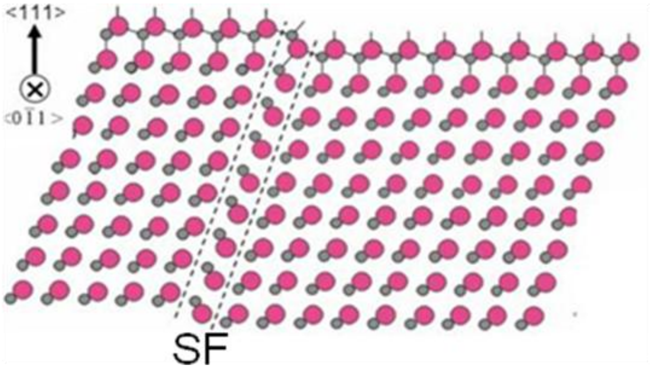

Figure 14. Schematic of the 3*C*-SiC surface in the (111) orientation, showing the local polarity inversion (C) at the SF with respected to the non-polar, Si-terminated (111) surface [66].

Contrary to 3*C*-SiC in the (111) direction, for 3*C*-SiC grown in the (100) direction (e.g. sample C in this work), SFs reaching the surface can be terminated either by Si or by C, and SFs of different terminations are separated by 90° angles at the surface. Current mapping on sample C (see Fig. 15) revealed leakage currents passing through the SFs also after the UV treatment. However, as can be noted by comparing Fig. 15a and Fig. 15b, only SFs of one surface termination are still conductive after the UV. Consequently, the observed passivation is likely related to a healing of C related defects at the surface.

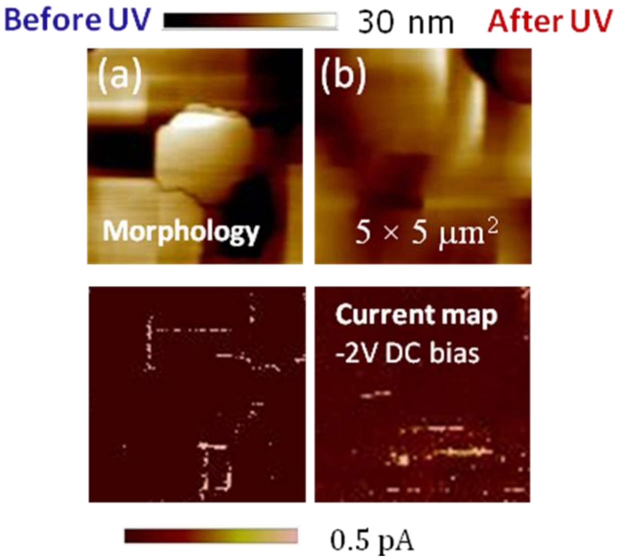

Figure 15. AFM morphology (top) and C-AFM current map (bottom) measured on sample C before (a) and after (b) UV irradiation. Only SFs of one surface termination (C or Si) are electrically active after UV.

To understand the mechanism of passivation, the AFM morphology of a chemical mechanical polishing (CMP) treated and UV irradiated 3*C*-SiC (111) surface was determined before and after selective wet oxide etching. As can be seen in Fig. 16a, after the UV irradiation the SFs produce line features of about 0.2 nm in height. The morphology determined after oxide etching (Fig. 16b) reveals trenches of a few nm at the SF locations. Hence, the passivation of the SFs may result from a preferential oxidation occurring locally inside these defects.

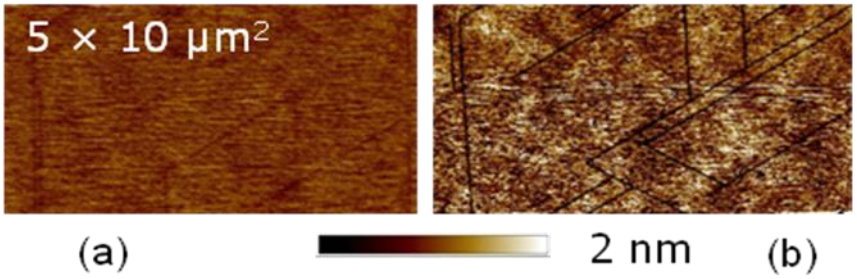

Figure 16. AFM morphology of the UV irradiated 3*C*-SiC surface before (a) and after (b) a wet oxide etch revealed trenches opening up in the SFs after etching, suggesting that their passivation is due to a local oxidation inside these defects.

Moreover, the *I-V* curves in Fig. 12 provide further information about the effects of the UV-irradiation on the overall oxidation of the 3*C*-SiC surface. The presence of a continuous insulating layer on the semiconductor surface would change the *I-V* characteristics from Schottky behavior into that of a metal-insulator-semiconductor (MIS) diode. For an intimate metal-semiconductor interface the current across the Schottky barrier can, in the ideal case, be described by thermionic emission theory [7] according to Eq. 1. However, it is known that when a metal contact is deposited onto a SiC surface the metal and semiconductor can be separated by an interfacial native oxide film of atomic dimensions. Indeed, it has been observed by performing in situ etching to remove this layer before metal deposition that the presence of the native oxide is beneficial for Schottky diodes [64]. According to Card and Rhoderick [67], in the presence of a thin (< 3nm) interfacial oxide layer Eq. (1) can be corrected by a transmission coefficient and becomes

$$I = AA^{*}T^{2}e^{-\sqrt{\chi\delta}}e^{-\frac{q\phi_{B}}{kT}}\left(e^{\frac{qV}{nkT}}-1\right) \tag{14}$$

where the transmission coefficient comprises the barrier height presented by the insulator, χ, and the thickness of the interfacial oxide, δ [67]. For an oxide thickness of less than about 2 nm the band structure of the SiO_2 bears little resemblance to that of bulk oxide (it varies not only with thickness but also with the type and density of interface states) and this coefficient needs to be determined experimentally from *I-V* data. For SiO_2 on Si it has been found experimentally that the coefficient term reduces from 0.25 to 0.08 as the SiO_2 thickness increases from 0.8 to 1.2 nm [67]. Assuming transmission coefficients in the same range in the case of SiO_2 on 3*C*-SiC, it is clear from the *I*-*V* curves in Fig. 12 that no continuous oxide layer of a significant thickness can be inferred after the UV-irradiation in our case. Therefore, the most likely explanation to the observed passivation effect is that a local oxidation has occurred preferentially just inside the SFs.

3.2.7 The Pt-3*C*-SiC system

The contact area dependence of Φ_B observed for the Au/3*C*-SiC system may result from an inhomogeneous interface between the metal and the semiconductor, or it could be caused by leakage currents related to surface states. Independent of its origin, this dependence should be mitigated if a "fresh" metal/3*C*-SiC interface if created instead of forming the contact interface at the original sample surface, which is exposed to chemicals, sputter damage and to air.

Pt is known to react with SiC at high temperatures to form platinum silicide [68]. This consumes a layer of the SiC by solid-state reactions, thus giving rise to an interface at a larger depth inside the material. Both Pt and its silicides have high work functions that should result in good barrier heights on 3*C*-SiC [68]. Hence, the electrical and structural properties of the Pt-3*C*-SiC system were investigated, where high temperature annealing can induce metal-SiC interface reactions and strongly affect the barrier homogeneity and/or leakage currents caused by semiconductor surface states.

3.2.7.1 Structural evolution upon annealing

Previous studies on Pt contacts to 3*C*-SiC have shown contradicting results; the onset of platinum silicide phase formation is reported to occur at annealing temperatures ranging from 650°C to above 750°C [69,70]. Moreover, also the effect of silicide phase formation on the contact properties is ambiguous; both increased [71] and reduced [37,70] leakage currents have been reported. Papanicolaou *et al*. found the barrier height value to gradually increase with increasing annealing temperature from as-deposited Pt up to 800°C, but the lowest leakage currents were found after 450°C [37]. Na *et al*. found that both the leakage currents and the Φ_B values gradually improved upon annealing between 500°C and 900°C [70].

In this study, the Pt_2Si phase was formed already after annealing at 500°C, as seen in the XRD patterns in Fig. 17. The Pt_2Si phase is thermodynamically stable in the studied temperature range [71] and the XRD patterns remain essentially the same also after annealing at 700°C and 900°C.

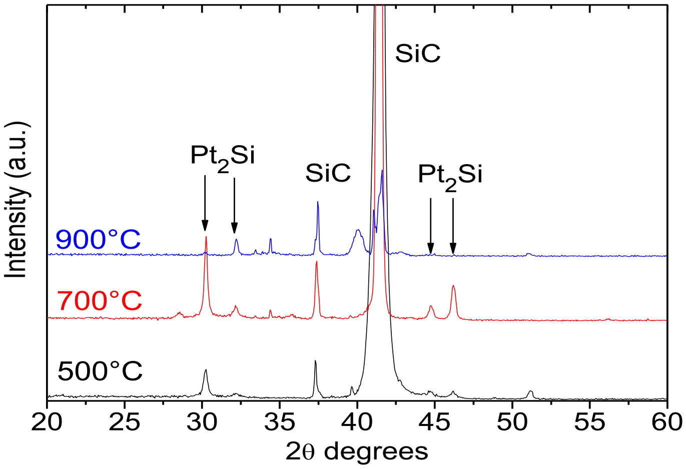

Figure 17. XRD patterns of the Pt/SiC system after annealing at 500°C, 700°C and 900°C. The Pt_2Si phase has formed already after annealing at 500°C, and the phase configuration remains essentially unchanged also after annealing at 700°C and 900°C.

3.2.7.2 Electrical evolution upon annealing

While XRD showed that all the Pt has been converted into the stable Pt_2Si phase already at 500°C, higher temperature annealing gives rise to increased localized high leakage current areas at the contact interface. Fig. 18a shows the AFM morphology of the SiC surface, where the large vertical lines are due to several stacking faults bunching together during the growth of the 3C-SiC substrate. Comparing Fig. 18a to the current map of an adjacent Pt contact (Fig. 18b) determined in the same sample orientation and at a tip bias of -5V, it is clear that the localized leakage spots occur preferentially along the direction of stacking faults.

The total area that is covered by these leaky spots (Fig. 18c) was determined from current maps measured after each annealing temperature, and increases from 12% at 500°C, to 28% and 55% after annealing at 700°C and 900°C, respectively. These leakage spots suggest a Schottky barrier inhomogeneity, characterized by local low barrier patches of about 0.5-1.5 µm in diameter. Clearly, the evolution of these low barrier patches will affect the properties of the fabricated diodes. Indeed, as discussed in 3.1.3, the existence of low barrier patches contributing to an overall lowering of the average barrier is a common way to model non-ideal macroscale diode behavior [2].

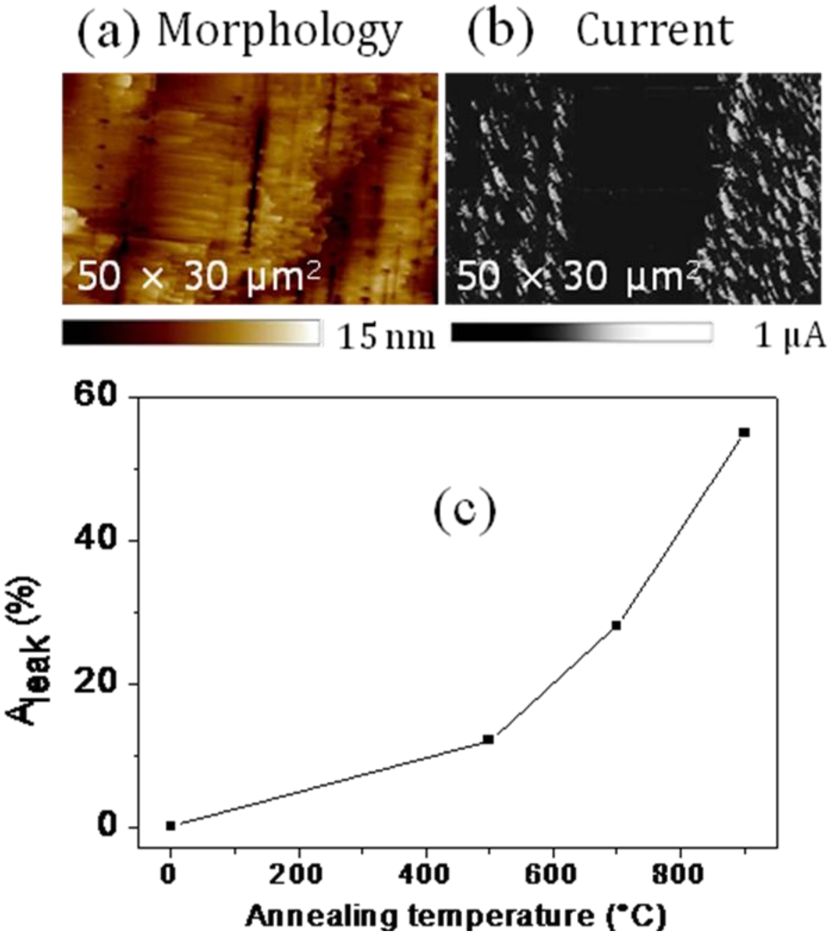

Figure 18. AFM morphology of the 3*C*-SiC (001) surface (a) and C-AFM current map determined at a tip bias of -5V on an adjacent Pt contact after annealing at 500°C (b). The total area covered by localized high leakage current spots depends on the annealing temperature according to the graph in (c).

Fig. 19 shows localized *I-V* spectroscopy measured by C-AFM at 25 different tip locations (separated by 1 µm) on the Pt contacts after annealing at 500°C (a), 700°C (b) and 900°C (c). Increased local variations are observed under both forward (barrier height) and reverse (leakage currents) bias as the annealing temperature increases, consistent with the increasing presence of localized low barrier patches at the contact interface.

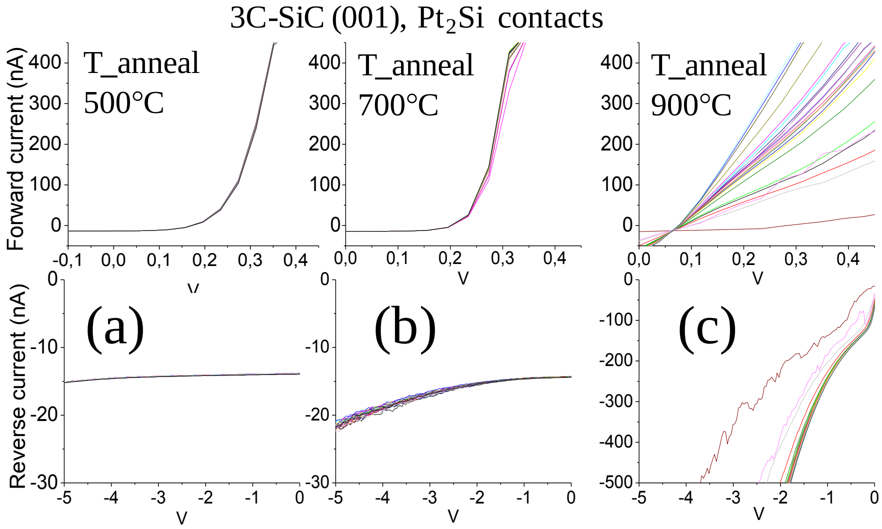

Figure 19. Localized forward (top) and reverse (bottom) *I-V* spectroscopy measured by C-AFM at 25 different tip locations on the Pt$_2$Si contacts after annealing at 500°C (a), 700°C (b) and 900°C (c).

I-V characteristics were also measured in an electrical probe after each annealing step on circular diodes with radii of 20 µm and 100 µm, and results obtained on the former are shown in Fig. 20a and Fig 20b. The average diode parameters, extracted from both areas, are summarized in Fig. 20c. For comparison, also the *I-V* behavior of as-deposited Au/3*C*-SiC diodes fabricated on the same original wafer (sample D) after UV irradiation is shown. As can be seen in (a) and (b), already the as-deposited Pt/3*C*-SiC contacts exhibited improved electrical properties with respect to the Au/3*C*-SiC system; the leakage current density at -3V measured for Au and Pt diodes on the same sample reduced from 1×10^{-6} A/mm^2 to 2×10^{-8} A/mm^2 (Fig. 20a and Fig. 20c). Moreover, the contact area dependence observed for the Au/3*C*-SiC system is absent for the Pt/SiC interface, at least while comparing diodes with radii of 20 and 100 µm, suggesting a better interface homogeneity. After annealing at 500°C, the leakage currents are slightly improved compared to the as-deposited Pt (Fig. 20a and c), whereas a strong improvement of the Schottky barrier height is observed for this annealing temperature (Fig. 20b and c). At higher temperatures (700°C and 900°C), both the reverse and forward *I-V* characteristics begin to degrade.

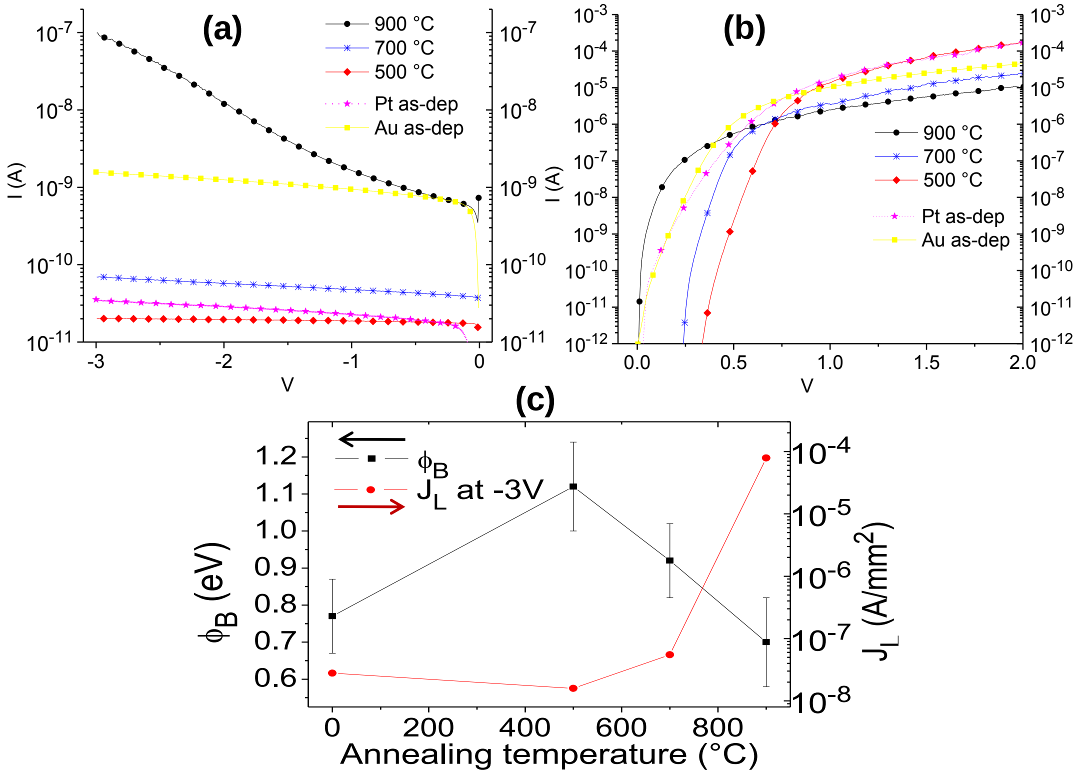

Figure 20. Reverse (a) and forward (b) *I-V* characteristics of as-deposited Au/3*C*-SiC diodes on sample D and Pt/3*C*-SiC and Pt_2Si/3*C*-SiC diodes on sample E (sample D and sample E are from the same wafer) after different annealing temperatures. The *I-V* curves are shown for diodes with a radius of 20 µm.. The Schottky barrier heights (black, left axis) and leakage current densities taken at -3V (red, right axis) extracted from I-V probe measurements for the different annealing temperatures are shown in (c).

3.2.7.3 Mechanisms of electrical evolution

To understand the electrical evolution upon annealing, the cross section of the Pt/3*C*-SiC interface was studied by TEM. As seen in the TEM images in Fig. 21, the Pt layer (Fig. 21a) has reacted completely after the 500°C anneal (Fig. 21b), and the consumption of Pt results in the formation of a polycrystalline Pt_2Si layer, characterized by the presence of interfacial protrusions penetrating into the underlying SiC [71]. However, additional changes are observed at higher temperatures. At 700°C (Fig. 21c), larger size variations are visible in the Pt_2Si protrusions and there is a formation of a carbon layer at the interface and carbon clusters inside the protrusions (also confirmed by energy filtered TEM). After annealing at 900°C (Fig. 21d) this layer is thicker, and more pronounced carbon clusters are observable inside the protrusions.

The TEM observations can be consistently correlated to the previously shown electrical results. Since Pt_2Si is the only phase observed by XRD for the different annealing temperatures, the evolution of the electrical properties after annealing above 500°C are likely unrelated to the silicide phase formation. More likely the changes in the electrical properties can be related to changes in the density of states at the contact interface. As reported by Mullins *et al*. [72], for the as-deposited contacts the surface states are presumed to behave as donor-like traps, generated during the sputtering of the metal. Hence, after annealing at 500°C the interface moves away from the original 3*C*-SiC surface and these states no longer affect the properties of the contact, causing a widening of the energy barrier that in turn causes the tunneling leakage current to reduce (see discussion in section 2.1 and Fig. 2.2 in particular). The gradual degradation observed at higher annealing temperatures can be explained by the increased amount of carbon clusters at the contact interface and in the Pt_2Si protrusions, due to incomplete diffusion of carbon upon further consumption of SiC, which has been shown to become an issue at annealing above 600°C [37]. The observed degradation can then be related to the electrical activity of the carbon clusters and/or the formation of carbon vacancies in the SiC resulting from the agglomeration of carbon at the interface, which could act as donors and cause a narrowing of the energy barrier and an increase of the leakage current.

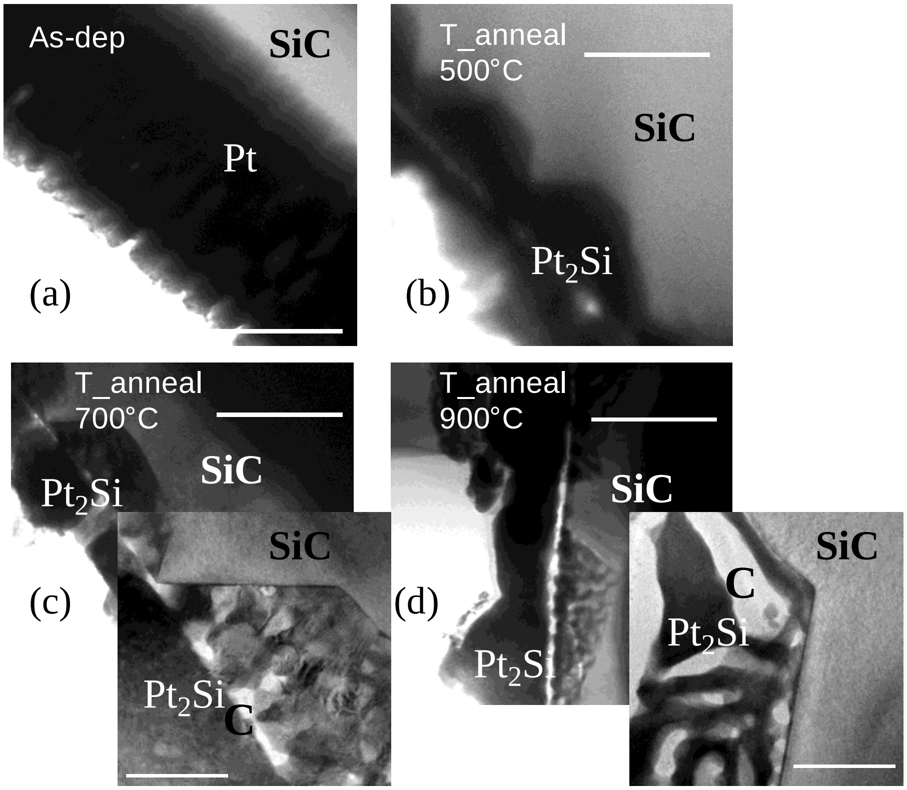
As-dep
SiC
Pt
(a)
T_anneal
500°C
SiC
Pt_2Si
(b)
T_anneal
700°C
Pt_2Si
SiC
SiC
(c)
Pt_2Si
C
T_anneal
900°C
SiC
SiC
C
Pt_2Si
(d)
Pt_2Si

Figure 21. Bright-field, cross-section TEM images of the Pt/3*C*-SiC interface for the as-deposited Pt (a), and after annealing at 500°C (b), 700°C (c), and 900°C (d).

3.3 Conclusion

Defects in cubic silicon carbide epilayers that were grown using different techniques and on different substrates (3*C*-SiC (001) or (100) or 4*H*- and 6*H*-SiC (0001)) were studied in terms of electrical activity and device limiting implications. The transport properties of metal/3*C*-SiC interfaces were monitored employing a nanoscale characterization approach, in combination with conventional electrical measurements.

I-*V* characterization of Au/3*C*-SiC diodes spanning a large range of contact area, coupled with defect analysis by TEM and C-AFM, demonstrated that the properties of Schottky contacts to 3*C*-SiC are limited by the abundance of defects in the available material. A structural analysis performed by TEM, coupled with an electrical characterization of the semiconductor surface by C-AFM, showed that stacking faults are normally the predominant type of defect that can affect the contact properties on these epilayers. Current mapping of the 3*C*-SiC surface showed that these defects form preferential paths for local detrimental leakage currents, in turn causing a reduction of the Schottky barrier height determined from *I-V* measurements to below 0.8 eV for the Au/3*C*-SiC interfaces in this study. It was also observed that in the presence of large quantities of double positioning boundaries, no Schottky behavior could be measured even when characterizing very small diodes (where the smaller amount of defects should reduce their detrimental influence).

C-AFM was also employed to show that a UV-irradiation treatment can be used to electrically passivate SFs that have a C surface termination, whereas such a treatment has no influence on the electrical activity of DPBs. UV-ozone treatment is known to oxidize SiC surfaces, however, no continuous oxide layer could be inferred from the experimental data. Consequently, the passivation of the SFs and subsequent improvement of the diode characteristics are presumed to arise from a local preferential oxidation 'inside' or 'on' these defects, related to their local polarity inversion with respect to the Si-terminated (111) 3*C*-SiC surface. From current-voltage (*I-V*) measurements performed on a sample where SFs were the only abundant type of defect, no significant dependence of the Schottky barrier height on the contact area could be observed for the non-UV-irradiated surface. On contrast, after the passivation of the SFs, Φ_B gradually increases with decreasing contact area, ultimately leading to a nearly ideal value of the barrier height for the Au/3*C*-SiC interface for diodes with a contact radius of 5 μm. Moreover, greatly reduced leakage currents were observed, while the forward currents were not affected, showing that the passivation reduces detrimental leakage through SFs without hindering the on-state operation of a device.

However, the contact area dependence of the Schottky barrier height found after this passivation indicates that other defects and/or inhomogeneities at the contact interface still remain electrically active. The contact area dependence of Φ_B was absent for the Pt/3*C*-SiC system, which also showed improved electrical properties with respect to the Au/3*C*-SiC system. Annealing of Pt/3*C*-SiC at 500°C resulted in further reduction of the leakage current and an increase of the Schottky barrier height. These changes are attributed to a consumption of the surface layer of SiC due to Pt_2Si formation. However, upon annealing at higher temperatures (700°C and 900°C) a degradation of the Schottky characteristics occurred. TEM analysis showed that this degradation can be ascribed to the aggregation of carbon clusters at the interface.

The results detailed in this chapter clearly demonstrate that surface preparations and interface reactions are important for the formation of good rectifying contacts to 3*C*-SiC. The conclusion is that a passivation of C-terminated SFs at the surface by UV irradiation prior to metallization, coupled with contact formation through a metal/3*C*-SiC interface reaction occurring at moderate temperature to avoid carbon clustering, is the best approach to achieve good Schottky contacts to 3*C*-SiC

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Chapter 4

Nanoscale probing of dielectric breakdown at SiO_2/3*C*-SiC interfaces

One of the potential applications for 3*C*-SiC is believed to be the fabrication of medium power (600-1200V), high-frequency metal-oxide-semiconductor field-effect transistors (MOSFETs). In the context of MOS devices, SiC in general has a great advantage with respect to competing compound semiconductors in the possibility to easily grow silicon dioxide (SiO_2) by thermal annealing in an oxygen ambiance. However, a high interface state density at the SiO_2/SiC interface leads to low inversion channel mobility in MOSFET devices, at least for the hexagonal polytypes. The mobility reduction is typically ascribed to the presence of large concentrations of near interface traps (NITs), energetically located near the conduction band edge in α-SiC [1]. The distribution of interface traps is shown as a function of the bandgap energy in Fig. 1a. As can be seen, for the 3*C* polytype, due to its lower forbidden bandgap, the NITs are located inside the conduction band and should therefore not significantly affect the channel mobility [2]. Moreover, α-SiC MOS devices have been found to be less stable than their Si counterparts, which can be partly attributed to the smaller conduction band offset (ΔE_C) at the semiconductor/SiO_2 interface. As can be seen in Fig 1b, $\Delta E_{C\text{-}4H\text{-SiC}} \approx 2.7$ eV compared to $\Delta E_{C\text{-Si}} \approx 3.15$ eV [3,4]. Consequently, for 4*H*-SiC less energy is required to cause electron injection from the semiconductor into traps in the oxide, resulting in faster accumulation of defects. For 3*C*-SiC, on contrast, the larger conduction band offset of about 3.6 eV [5] may promote better device reliability.

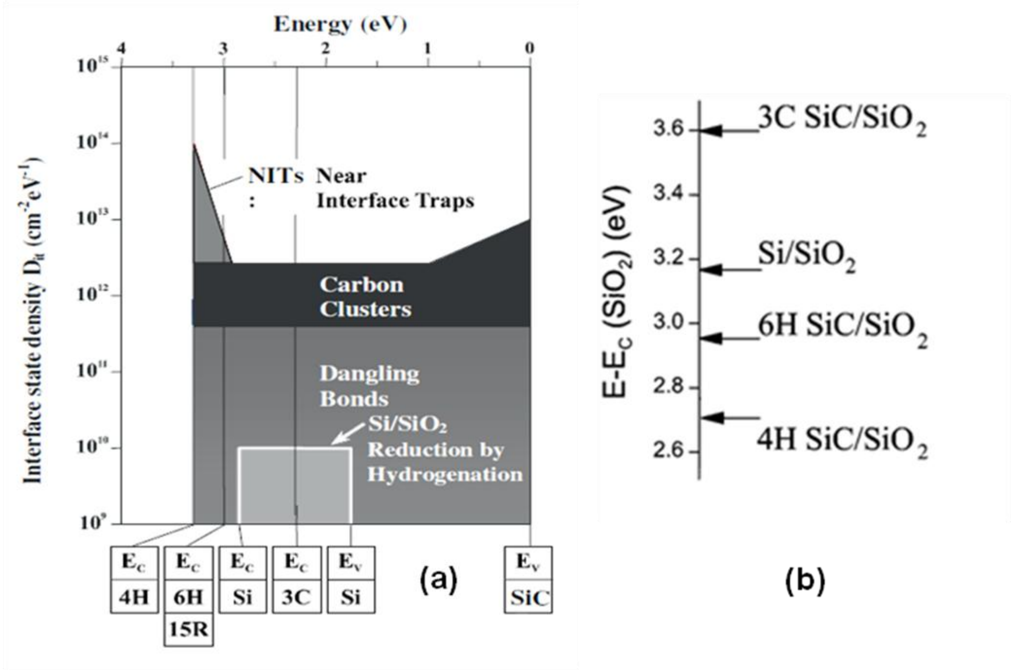

Figure 1. The distribution of interface traps is shown as a function of energy in (a). Fig. 1a is reproduced from Ref. [1].The conduction band offsets between SiO_2 and different semiconductors are shown in (b).

While there have been several studies focusing on the density of charges and traps, as well as the energy levels of traps in thermal oxides on 3*C*-SiC [6-13], the reliability and the premature breakdown (BD) generation mechanisms in thermal oxides grown on this polytype have not been addressed. In addition to the intrinsic properties of the dielectric, the BD event is controlled by defects at the semiconductor surface, the conduction band offset at the semiconductor/SiO_2 interface, and oxidation and post oxidation conditions [3,14]. The nature of the defects, the conduction band offset and the optimal oxidation and post oxidation conditions [7] are different for 3*C*-SiC compared to the better studied 4*H* polytype. In that context, deeper knowledge of the properties of SiO_2 gate oxides on 3*C*-SiC and of the reliability of the SiO_2/3*C*-SiC system is fundamental to ultimately understand the device behavior and to achieve optimal performances.

This chapter investigates the influence of the 3*C*-SiC surface morphology and specific surface defects on the premature local BD generation in thin (6-12 nm) thermally grown SiO_2 layers. Conductive atomic force microscopy (C-AFM) enables concurrent imaging of surface morphology and two-dimensional current distribution with nanoscale lateral resolution. This, in turn, allows localized breakdown to be directly observed as a function of stress time and correlated with the surface morphology. Additionally, capacitance-voltage (*C*-*V*) measurements, alongside scanning capacitance spectroscopy (SCS) characterization were used to quantify oxide charges and to study nanoscale variations in the charge distribution, respectively. These analyses permitted an evaluation of the influence of the pre-oxidation surface roughness, the presence of defects at the surface, and oxide charges on the BD generation in the oxides.

4.1 Experimental

Thin (≈ 2 μm), *n*-type 3*C*-SiC (111) heteroepilayers were grown at LMI in Lyon by vapor-liquid-solid (VLS) mechanism onto Si-face, 2° off 6H-SiC (0001) substrates by using a $Si_{50}Ge_{50}$ melt which was fed by propane at 1350°C for 10 min. Growing under these conditions led to a single-domain (twin-free) 3*C*-SiC layer [15]. An additional growth of a 10 μm thick epilayer was performed by chemical vapor deposition (CVD) at 1650°C under silane and propane [16], resulting in layers with a residual *n*-type doping ($N_D \approx 5 \times 10^{16}$ cm^{-3}). Then, ~1 μm thickness was removed by chemical-mechanical polishing (CMP) on one sample to reduce the surface roughness and the amount of epitaxial defects at the near-surface. The samples are hereafter denoted A, referring to the one with just the VLS layer, and B and C referring to the samples with the additional CVD layer before and after CMP, respectively. Prior to oxidation the samples were cleaned by etching for 5 min in $H_2SO_4 : H_2O_2 = 3 : 1$ solution followed by 5 min of etching in HF : H_2O = 1 : 10 solution. SiO_2 was then grown at 1150°C in dry O_2 for 10 min or 20 min, after which the temperature was ramped down to 800°C (5°C/min) in N_2. Oxide thicknesses were determined by AFM measurements with a PSIA XE-150 SPM on 10 μm wide strips that were opened in the oxides by means of optical lithography and wet etch. Several 80 × 80 μm^2 areas were scanned and the oxide thickness was measured at 25 different positions on the samples. Average oxide thicknesses of 12.0 ± 2.7 nm, 6.2 ± 2.5 nm and 7.0 ± 0.4 nm were determined for samples A, B and C, respectively. Lastly, a large area gold electrode was sputtered onto the heavily doped substrate side of the samples as Ohmic contact. The sample structures and designations are illustrated in Fig. 2.

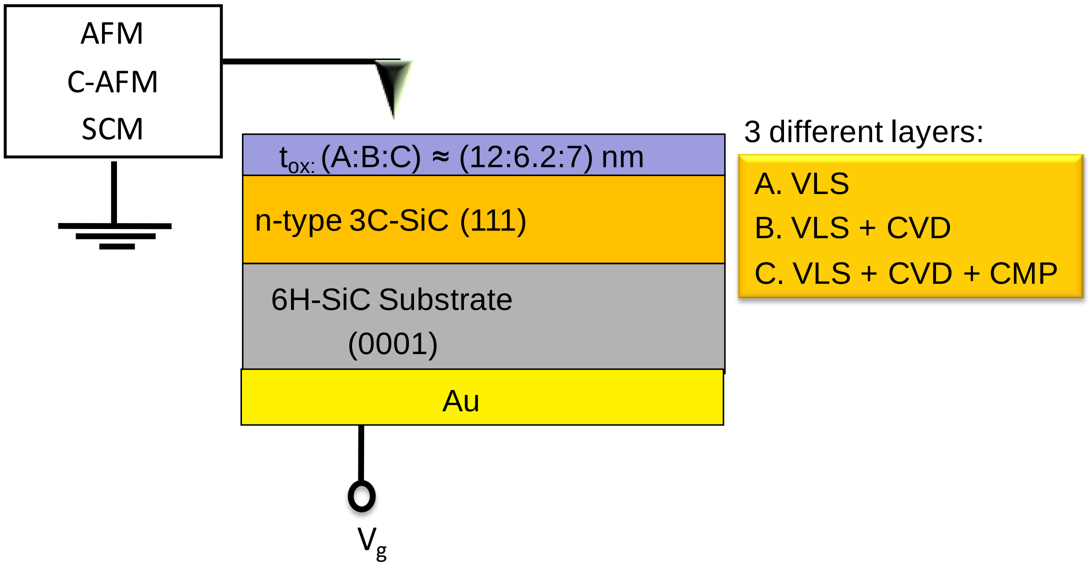

Figure 2. Illustration of the fabricated structures and the measurement approach.

The nanoscale morphological and electrical properties were determined with a Veeco DI dimension 3100, equipped with the Nanoscope V electronics and the C-AFM and scanning capacitance microscopy (SCM) modules, to measure local current and capacitance distributions, respectively. The measurements were performed using conductive, diamond-coated Si tips, due to their excellent mechanical and electrical stability [17,18]. Local constant-voltage time-dependent dielectric breakdown (TDDB) measurements were performed by stressing the sample utilizing the C-AFM instrument, which forms a 'nano-MOS' capacitor at each tip position as the biased probe tip is scanned in contact with the oxide-semiconductor system. C-AFM current mapping was performed while applying a constant DC bias of -10V to the back-contact of the sample, corresponding to accumulation conditions. Capacitors were fabricated by depositing a gold layer onto the oxide, which was patterned by lithography and wet etching to form arrays of dots of 50 and 150 μm in radius. The *C-V* characteristics were measured on the MOS capacitors (Au/SiO_2/3*C*-SiC/Au) using a HP 4284A impedance analyzer operated at an AC bias frequency of 1 MHz. The *C-*

V characteristics were obtained sweeping the DC bias voltage first from accumulation to inversion, and then back to accumulation. The local dC/dV - V_{DC} behavior of the SiO_2/3*C*-SiC systems was studied by scanning capacitance spectroscopy (SCS). The dC/dV characteristics were obtained sweeping the DC bias voltage first from accumulation to inversion, and then back to accumulation. Capacitance maps were determined by contact mode measurements using the SCM module. Both the SCS and SCM measurements were conducted with an AC-modulation bias of 800 mV with a frequency of 100 kHz applied to the tip-sample system, and the resonant frequency of the capacitance sensor was 880 MHz.

4.2 Material characterization

The 3*C*-SiC surface morphology of the samples was investigated before oxidation and AFM micrographs obtained by tapping mode measurements are shown in Fig. 3. The RMS roughness (measured over 50×50 μm^2 areas) for the three samples is reported Fig. 3 and in Table 1 on page 127. In addition to high roughness, the 3*C*-SiC surface of sample A showed large step-bunching edges (ranging from 10 to 30 nm in height) and high densities of triangular pits and stacking faults (SF). Sample B also exhibited similar step-bunching but showed reduced roughness and no triangular pits (Fig. 3b). As seen in Fig. 3c, after the CMP step the (111) surface is instead very smooth (RMS roughness = 0.2 nm). A closer view (10×10 μm^2) allowed observing dark lines making 60° angles which can be attributed to stacking faults.

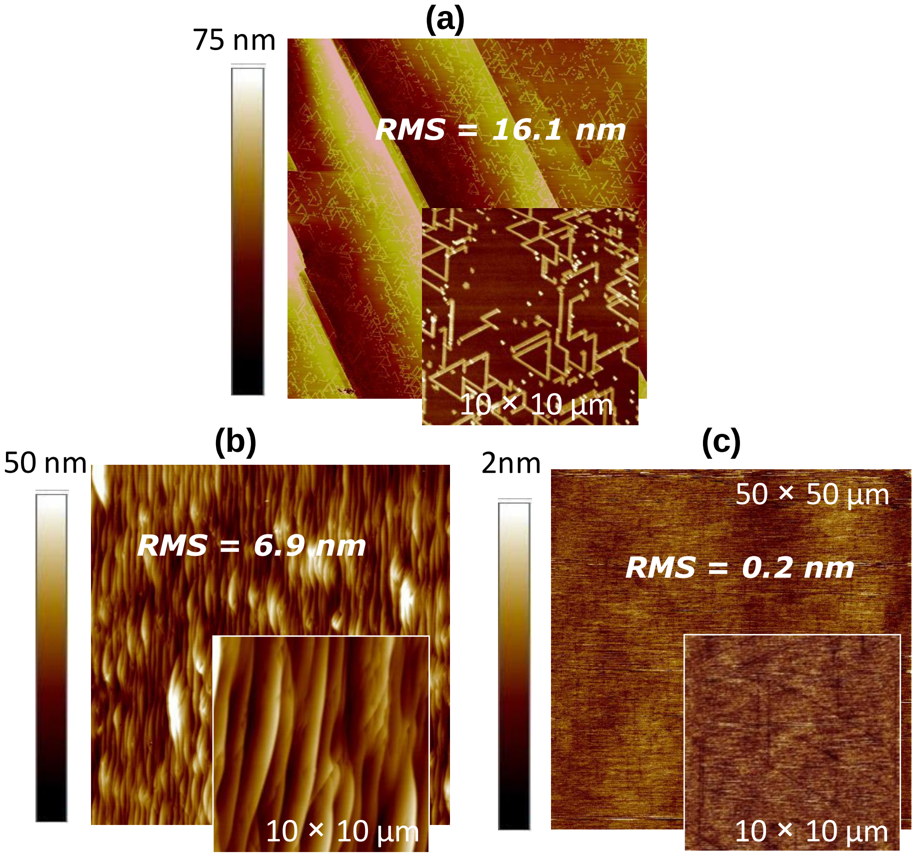

Figure 3. Morphology of 50 × 50 μm^2 areas of the 3*C*-SiC surface of sample A (a), sample B (b) and sample c (C) determined by AFM measurements performed in tapping mode before the oxidation. Then insets show magnifications of 10 × 10 μm^2 areas, where the step bunching edges (a and b) are clearly visible before the CMP on samples A and B, and stacking faults (c) are visible as dark lines separated by 60° angles after the CMP on sample C.

The micrographs in Fig. 4 show morphology (left) and corresponding capacitance (*dC/dV)* variations (right) measured by SCM on 10 × 5 μm^2 areas on the oxide of sample B and C. A DC bias of 0V and a 100 kHz AC bias of 800 mV were applied to SCM tip during the scans. As can be seen, the previously identified morphological features are visible also after the oxide growth. Moreover, the capacitance clearly exhibits larger lateral variations across the oxide on sample B. Indeed, the capacitance variations resemble the morphology, suggesting possible local oxide thickness variations near the step edges. As a matter of fact, it was shown in [19,20] that the main contribution to the capacitance variations observed during SCM mapping of dielectric/semiconductor structures comes from variations in the dielectric thickness, and that the capacitive contributions from defects and charges distributed in the dielectric layer are negligible. Using the approximation of a planar parallel capacitor, the local capacitance at each tip position is given by $C= \varepsilon\varepsilon_0 A/t$, where ε is the relative dielectric constant of the oxide, ε_0 is the vacuum permittivity, A is the area of the tip-SiO_2 contact, and t is the local oxide thickness at the particular tip position. The variation in the capacitance value must be related to thickness variations, since ε and ε_0 are physical constants, whereas the tip-SiO_2 contact area A is invariant. Thus, the variations in the capacitance signal in Figure 4b gives a two-dimensional map of the oxide thickness variations, where the different uniformities of oxides grown on the as-grown and the CMP treated 3*C*-SiC surfaces can be clearly seen. A quantitative evaluation of the *dC/dV* maps showed that the standard deviations of the capacitance signal are 42 % and 5 % of the mean value for samples B and C, respectively. This corresponds to thickness variations of 2.4 nm for sample B and 0.35 nm for sample C, which agree very well with the standard deviations of the thicknesses determined by AFM measurements on strips opened up in the oxides by selective wet etching. The inhomogeneous oxide thicknesses on samples A and B are expected to generate a spread in the BD kinetics determined by the C-AFM stress measurements, since not all nanoscale MOS devices, formed at each tip position during the scan, will have the same thickness and dielectric properties. For sample C the capacitance is decidedly more uniform, consistent with the much lower roughness of semiconductor surface at the oxide interface.

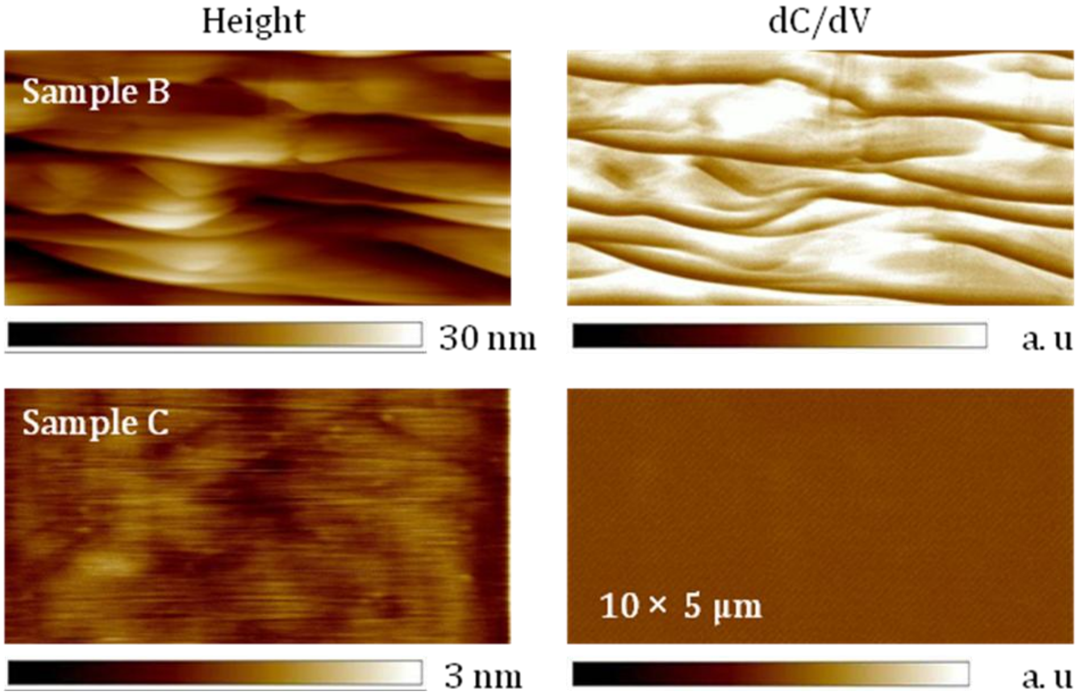

Figure 4. Morphology (left images) of the SiO_2 surface, with the corresponding capacitance variations measured by SCM shown on the right. A clear correlation can be seen between morphological peaks and drops in the capacitance signal on sample B. Due to the superior smoothness of sample C, the only visible variations in the *dC/dV* signal measured on this sample are the periodic lines related to the 50 Hz electrical noise in the lab environment.

4.3 Localized TDDB measurements by C-AFM

Two methods are commonly employed for stressing and testing the reliability of thin oxide layers. Both entail observing the oxide breakdown as a function of stress time while keeping either the oxide voltage or the Fowler-Nordheim (FN) current density, J_{FN}, through the oxide constant. During constant voltage stress (CVS) measurements, the oxide breakdown is observed as an abrupt increase of the current density, and the time-to-breakdown, t_{BD}, at a certain electric field strength becomes the figure of merit. In constant current stress (CCS) measurements, the BD event results in the drop of the applied voltage, and the charge-to-breakdown, Q_{BD}, is the figure of merit. The definition of t_{BD} is trivial, whereas Q_{BD} is defined as [21]:

$$Q_{BD} = \int_0^{t_{BD}} J_{FN}\, dt \qquad (1)$$

The breakdown event is commonly explained by percolation theory [22], which attributes it to defects (like electron traps, interface states, charged donor-like states, etc.) at random positions within the oxide gradually accumulating and forming a conductive path through the dielectric. When two defects, assumed to be spherical and of equal radius *r*, are separated by less than a certain fixed distance *D*, conduction between them is possible. As more defect states are generated during electrical stressing, conducting chains of neighbouring defects are linked. Eventually, this process results in the formation of a path that connects through the entire oxide layer, leading to the sudden destruction of the dielectric properties. Figure 5 schematically shows a non-conductive and a conductive percolation path within the oxide. Here, *t* denotes the transition-layer thickness to account for the conductive nature in the vicinity of the metal-oxide and oxide-SiC interfaces [23].

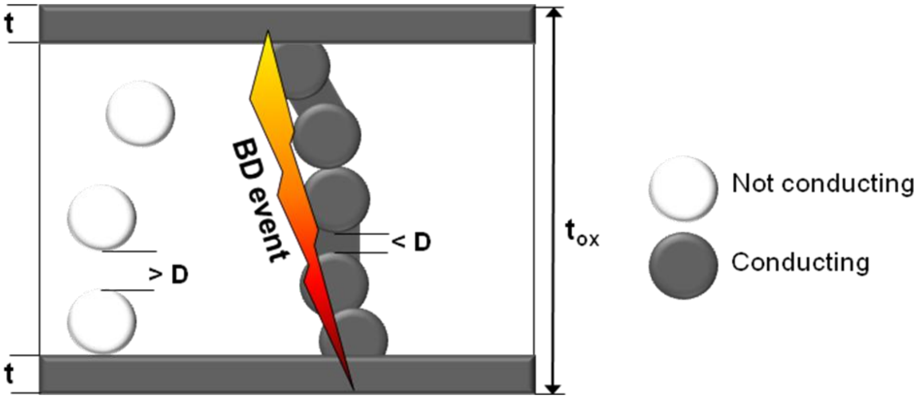

Figure 5. Illustration of the random defects sphere model (after Degraeve *et al*. [22]). A cluster of interconnecting defects spanning the whole oxide from top to bottom defines the breakdown event.

For SiO_2 on 4*H*-SiC, TDDB measurements on MOS devices usually result in reliabilities inferior to the intrinsic ones expected for ideal SiO_2 [3,22]. Possible causes of poor gate oxide reliability are considered to be crystalline defects reaching the oxide/semiconductor interface, residual carbon impurities in thermally grown SiO_2, or surface roughness. Since breakdown is a weakest link type of problem, any process-induced local weak spots will break a macroscale device, which could explain the bad reliability usually observed for 4*H*-SiC/SiO_2 MOS devices.

In this work, instead, localized constant-voltage TDDB measurements with high lateral resolution were performed by scanning a biased C-AFM tip in contact mode on the SiO_2 surface to locally stress the oxide. Each region scanned by the C-AFM tip can be considered as an array of 'nano-MOS' capacitors (pixels), the area of which is defined by the tip contact radius, assumed in this case to be ≈ 50 nm. The capacitors can be stressed and kept in accumulation by introducing a negative bias voltage on the sample substrate from the probe station chuck (i.e. the high potential is at the conducting tip). In these conditions, the breakdown phenomena can be observed as a function of stress time. The stress time per pixel (single nano-MOS), t, is defined as

$$t = \frac{T}{L/a} \tag{2}$$

where T is the scan time per line, L is the length of each scanned line, and a is the tip diameter [24,25]. The stress time was increased in a step-wise manner by repeatedly scanning the same areas while keeping the scan time and the bias voltage constant. This allowed direct observation of BD as a function of stress time while also revealing the surface morphology of the stressed area.

As discussed above, dielectric breakdown occurs due to the formation of conductive percolation paths. Consequently, localized BD events give rise to high conductivity spots that can be directly observed in the C-AFM micrographs. Fig. 6 shows current maps of the oxide surface of samples A, B and C after different stress times at a substrate bias voltage of -10V, where the dark spots correspond to local breakdown. As seen, the BD generation starts at lower stress times for samples B and C, attributed to the slightly thinner oxides. The more pronounced BD generation observed on sample B compared to sample C can be largely attributed to a larger amount of process-induced weak spots in the oxide layer, in turn related to the rougher pre-oxidation surface morphology. However, in all cases the density of BD spots increases upon increasing the stress time and the total area of the BD spots is proportional to the number of broken nano-MOS devices.

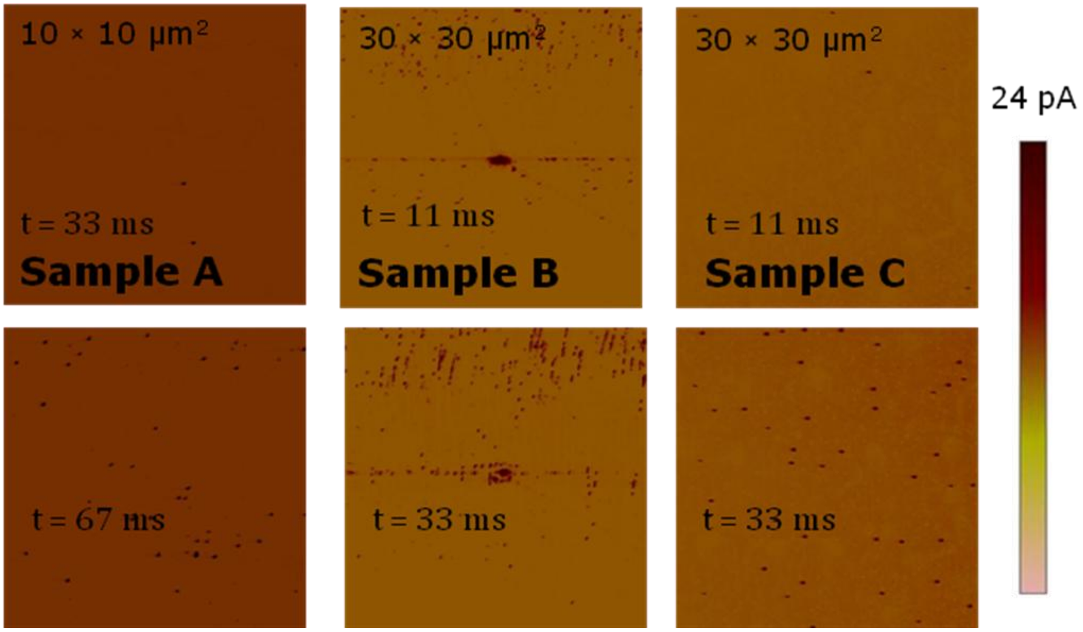

Figure 6. C-AFM current maps recorded on a 10 × 10 μm^2 area on sample A and on 30 × 30 μm^2 areas of the SiO_2/3*C*-SiC of sample B and sample C. The BD spot concentration increases with increasing stress times at -10 V bias applied to the sample back conta1ct. The black color corresponds to current density greater than 0.15 A/cm^2.

The cumulative failure ratio has been determined in different phases of electrical stress. The ratio between the number of failed devices and the total number of stressed devices can be described by:

$$F = \frac{N_f}{N_i} = \frac{A_{tf}}{A_{dev}} \cdot \frac{A_{dev}}{A_i} \qquad (3)$$

where F denotes the failure ratio, N_f is the number of failed devices and N_i is the total number of devices in the mapping region, A_{tf} is the total area covered by the failed devices, and A_i is the total area of the stressed region. The contact area (A_{dev}), governing the dimension of a single MOS device, is the same in the failed and the stressed regions and can be neglected. The ratio from Eq. 3 can then be determined from the C-AFM micrographs. Each micrograph comprises a 512 × 512 data points matrix, where each point represents the current value at a specific position in the 2D map. The statistical distribution of these data points results in two distinct peaks, one near zero current and another around the maximum current value in the micrograph, where the high current values correspond to BD spots. From these distributions, the failure ratio was estimated from the percentage of data points belonging to the high current peak. The statistical distributions after different stress times determined during a stress measurement on sample A are show in Fig 7a-c, while the cumulative failure ratio as a function of stress time from the same experiment is shown in Fig. 7d. It should be mentioned that the maximum current value of about 12 pA is limited by the compliance of the current sensor used for the measurement, and that the real BD current is likely larger. As can be seen in Fig. 7d, the BD generation ratio starts to increase abruptly after a certain stress time has been reached. This is when the "intrinsic" breakdown of the oxide starts to occur, following percolation theory. The BD spots observed at lower stress times are attributed to weak spots in the oxide layer, which may be for example due to the processing, due to defects at the oxide-semiconductor interface, or due to oxide traps or charges, causing enhanced percolation path formation. This type of breakdown is referred to as "extrinsic".

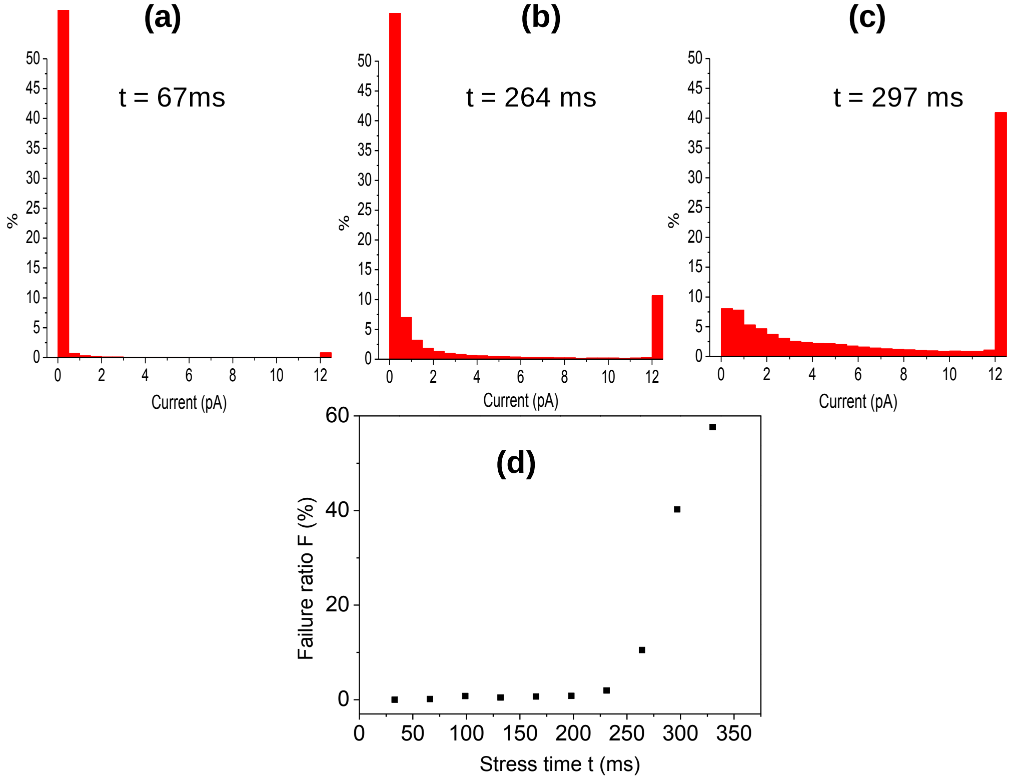

Figure 7. Statistical distribution of current over a 10 × 10 µm^2 scanning area on sample A after stress times of 67 ms (a), 264 ms (b) and 297 ms (c). The cumulative failure ratio *F* as a function of stress time *t* determined during the series of C-AFM scans is shown in (d). An abrupt increase in the failure generation ratio occurs after a stress time of about 250 ms.

The data in Fig. 7d suggests that almost 60 % of the nano-MOS devices are broken after being stressed for 333 ms at an electric field strength just under 10 MV/cm. This time to breakdown may seem low compared to the several minutes that are normally required to cause BD under these conditions for metal/SiO_2/4*H*-SiC MOS structures [3,26]. However, a direct comparison of the time to breakdown found in the literature concerning SiC MOS structures should not be considered for two reasons. First, in this work the investigation is focused on thin oxides (6 – 12 nm), whereas for MOS applications the thickness is usually ≥ 50 nm. A consequence of the thinner oxides is that the percolation path formation is much faster for the oxides studied in this work.

The time to breakdown for the same electric field strength increases with increasing oxide thickness because the minimum number of defect states needed to create a breakdown path through the oxide increases [27]. Secondly, the stress time according to Eq. 2 is determined from the tip dimension, which is an estimation. Moreover, the same pixel is likely stressed more than once during each scan, considering that 512 lines are scanned over 10 × 10 μm^2 areas. Consequently, the stress time according to Eq. 2 is likely an underestimation.

4.4 Statistical analysis of BD generation

Time-to-breakdown values are commonly assumed to be Weibull distributed, which is typical for "weakest link" processes. The BD kinetics of the oxides was evaluated by fitting our experimental failure ratio to the failure probability described by Weibull statistics:

$$F(t) = 1 - e^{\left(\frac{t}{\alpha}\right)^{\beta}} \qquad (4)$$

where t is the stress time, α is the characteristic lifetime of the dielectric (corresponding to the time where 63.2% of samples fail), and β is the Weibull slope, which is a useful parameter to characterize the reliability of dielectrics [27]. By plotting the value of $\ln[-\ln(1-N_f/N_i)]$ for the nano-MOS capacitors as a function of the natural logarithm of the stress time t, α and β can be obtained from the y-axis intersect and the slope of the fit, respectively. As discussed in 4.3, the estimated stress time is fraught with a large uncertainty, rendering life time estimations infeasible using the experimental approach in this work. However, a systematic error in the estimated stress time would not affect the calculated Weibull slopes, since it would only result in a shift of the data along the X-axis. Weibull plots are shown for the three samples in Fig. 8. For all samples it is possible to distinguish between the extrinsic and the intrinsic breakdown discussed in 4.3; at short stress times the failure generation proceeds at a lower rate until a certain point in stress time is reached, where the failure generation continues at a higher, constant rate. It should be mentioned that the data points presented in Fig. 8 are the average values of several series of stress measurements, and that the reported error bars are their standard deviations.

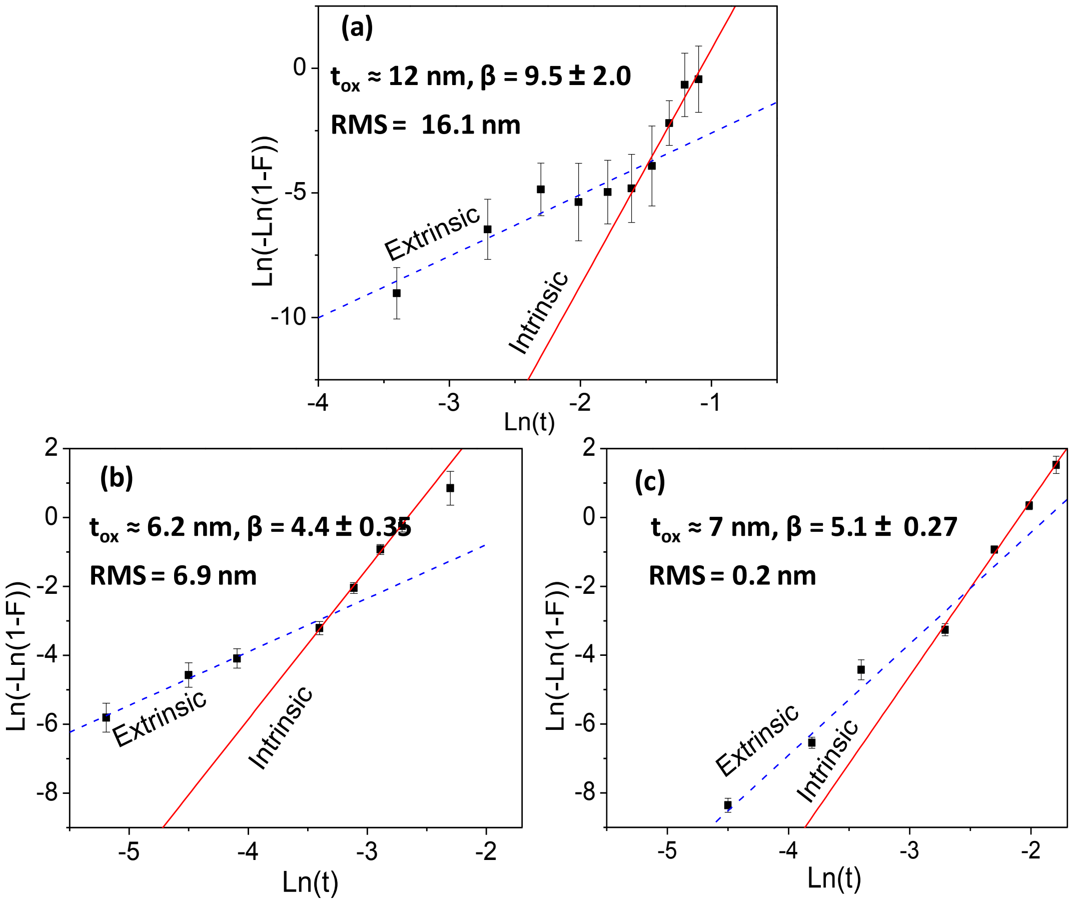

Figure 8. Breakdown kinetics and Weibull plots for sample A (a), sample B (b), and sample C (c). The dashed fit is attributed to breakdown caused by pre-existing defects or oxide weak spots, whereas the solid fit corresponds to the intrinsic breakdown of the oxide. The smaller error bars reported for the smoother surfaces are consistent with a higher degree of homogeneity of the oxide layer thickness. The smaller difference between the failure generation rate in the extrinsic and intrinsic parts indicates fewer process-induced weak spots in the oxide layer of sample C.

According to percolation theory the intrinsic Weibull slope should, for a given dielectric, depend only on the thickness. A plot of β versus the oxide thickness is shown in Fig. 9, where the values obtained in this work are compared to what is predicted by the percolation theory of dielectric breakdown [22]. In the same plot, previous findings for similar thicknesses of SiO_2 layers grown on Si are reported, i.e., where the oxide quality is close to ideal [28]. As can be seen, if the experimental data is fitted to Weibull statistics only considering the data after the onset of the intrinsic breakdown (see fits in Fig. 8), the obtained β values agree well with what is expected for an ideal oxide. This, in turn, confirms the validity of this unconventional experimental approach.

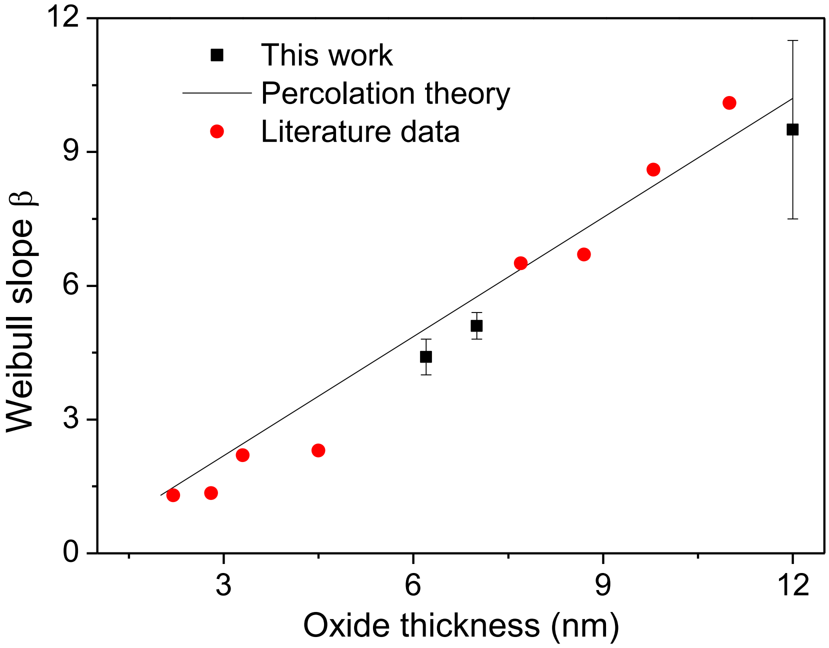

Figure 9. Comparison of the Weibull slopes determined in this work, in literature for SiO_2 on Si, and the values predicted by percolation theory [22,28].

We define here a criterion to estimate the reliability of our oxides on 3*C*-SiC, i.e., the difference between the extrinsic and intrinsic slopes, *E*/*I*; the smaller the difference the closer the oxide is to the ideal one with only intrinsic behavior. As seen in Fig. 8 and reported in Table 1, the difference is decidedly smaller for sample C, with the lower *3C*-SiC pre-oxidation surface roughness. For the oxides grown on the rough surfaces of sample A and B, the slopes fitted to the extrinsic BD regions are 26.3 % and 35.2 %, respectively, of the intrinsic slopes. This ratio increases to 62.7 % for the smoother pre-oxidation surface of sample C. Moreover, also larger statistical variations were observed for sample A, as seen in the error bars that were determined from the standard deviation. The latter can be attributed to the larger oxide thickness inhomogeneity due to the larger roughness, which was also observed by AFM and SCM morphology and capacitance mapping.

Table 1. Summary of the measured properties for the samples in this study.

t_{ox}	β	RMS (50 × 50 μm^2)	E/I
12.0 ± 2.7 nm	9.5 ± 2.0	16.1 nm	26.3 %
6.2 ± 2.5 nm	4.4 ± 0.4	6.9 nm	35.2 %
7.0 ± 0.4 nm	5.1 ± 0.3	0.2 nm	62.7 %

4.5 Causes of premature dielectric BD

4.5.1 Structural defects and morphological features

As discussed above, a marked reduction of the extrinsic BD population was observed upon reducing the pre-oxidation surface roughness from 16.1 to 0.2 nm. From this, a reasonable conclusion is that low pre-oxidation surface roughness and high uniformity at the oxide-semiconductor interface are important prerequisites for achieving ideal oxide reliability. However, an extrinsic BD population exists even for the oxide grown on the smooth surface of sample C, resulting in an initial Weibull slope that is only 62.7 % of the intrinsic slope. Since the BD event is a weakest link problem, the presence of any BD spot in a fabricated device will cause it to fail. In order to achieve the optimal device performance it is therefore important to understand (and possibly eliminate) the extrinsic population.

In the case of SiO_2 on 4*H*-SiC, Senzaki *et al*. [14] observed, after constant voltage TDDB measurement, that dielectric breakdown mainly occurred at basal plane dislocations in the epilayer. This result was contradicted by the study of Matocha *et al*. [3], reporting that the breakdown location observed after constant current Q_{BD} measurements was not correlated to any of the underlying epitaxial defects. These two contradicting results were observed on KOH etched SiC surfaces. Later Kozono *et al*. [29] performed local stress measurements using C-AFM to show that BD in 4*H*-SiC/SiO_2 interfaces occurs primarily on step-bunching edges. These different findings illustrate that the roots of the premature BD observed for SiC/SiO_2 structures are not entirely understood.

A possible cause for a local acceleration of the BD generation is that a concentration of the electric field occurs on top of some structural defects, due to their pronounced morphological features. As observed from the pre-oxidation surface morphology and the post-oxidation capacitive distributions (Fig. 3 and Fig. 4, respectively), the main defects observed on the 3*C*-SiC surfaces in this study are step-bunching edges and SFs, where the latter are the only abundant defects remaining after a CMP step. The locations of the BD spots, observed by C-AFM, are shown next to the simultaneously acquired SiO_2 surface morphologies in Fig. 10. For the rough pre-oxidation surfaces on sample A and sample B (Fig.10a and Fig. 10b) a preferential BD generation is observed in the vicinity of step-bunching edges. For the oxide grown on the CMP treated surface of sample C (Fig. 10c), no direct correlation between the location of the BD spots and that of the SFs can be established, and no accelerated breakdown generation can be inferred at these defects. In fact, due to the preferential oxidation proceeding at a higher rate on the SFs at a 3*C*-SiC (111) surface [30], BD generation is likely reduced on top of these defects due to a weaker electric field across the oxide. Therefore, the larger deviance between the extrinsic and intrinsic BD observed on samples A and B can be mainly attributed to the accelerated BD generation on top of step-bunching edges, while SFs cannot be considered responsible for the extrinsic population observed in the oxide grown on the CMP treated surface of sample C.

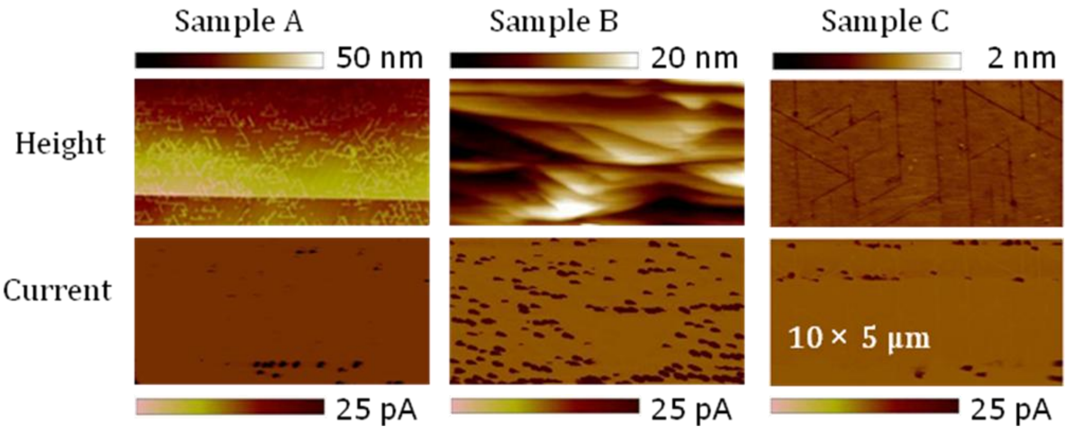

Figure 10. Morphology (upper images) of the SiO_2 surface with the corresponding current maps (lower images), showing the BD spots generated after a stress time of 67 ms on samples A, B and C. The black color in the current maps corresponds to current density greater than 0.15 A/cm^2. BD occurs preferentially along step bunching edges on sample A and sample B, whereas no correlation exists between BD locations and SFs on sample C.

To better understand the accelerated BD at the step-bunching edges, Fig. 11 shows the morphology of sample B determined on the 3*C*-SiC surface (a) and the SiO_2 surface (b), as well as line traces of the step-bunching edges for the two different surfaces (c). As can be seen, the step morphology is more pronounced at the semiconductor surface; the step height is typically 10-25 nm on the as-grown *3C*-SiC surface and 5-15 nm after oxidation. Considering the resulting cross section of the 3*C*-SiC/SiO_2 structure, which is schematically illustrated in Fig. 11d, a local electric field concentration can be assumed in the vicinity of these defects, caused by the abrupt change in height. Consequently, the accelerated BD generation at the step edges can be attributed to a local electric field concentration that enhances the defect generation in the oxide layer at the step.

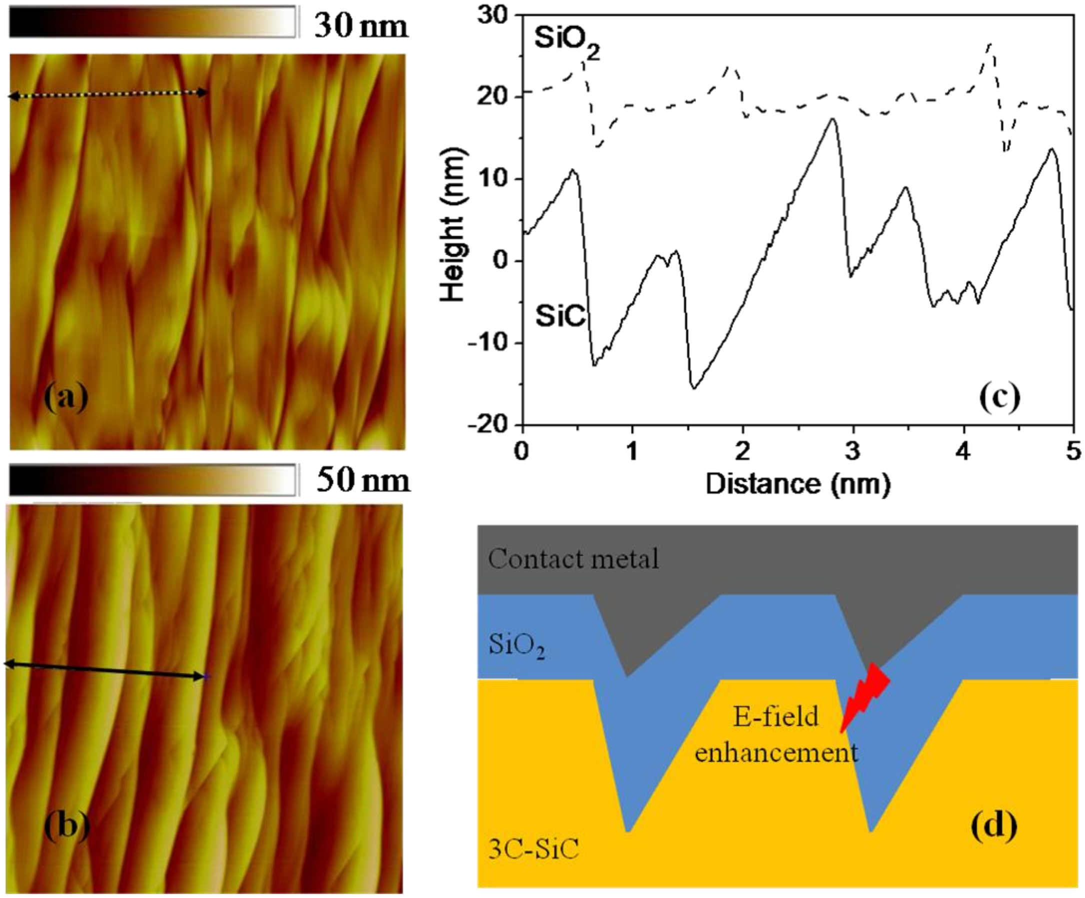

Figure 11. Comparison of the step bunching morphology on sample B before (a) and after (b) oxidation (micrographs not determined at the same position). As seen in the line traces (c), determined along the lines indicated in (a) and (b), the steps are significantly higher at the 3*C*-SiC surface than at the oxide surface. This leads to a local enhancement of the electric field at the step bunching edges, as illustrated schematically in (d).

4.5.2 Oxide charges and traps

A possible explanation to the extrinsic BD population observed at the smooth interface of sample C is that charges in the oxide or electron injection into traps near or at the oxide interface cause a localized acceleration of the formation of the percolation paths upon electrical stress. Fig. 12 shows the high frequency (1 MHz) *C*-

V curves measured on Au/SiO_2/3*C*-SiC capacitors fabricated on samples B and C. The characteristics were obtained sweeping the bias voltage first from accumulation to inversion, and then back to accumulation. As can be seen, there is a hysteresis between the sweep directions, with a reduction of the flatband voltage shift going back from inversion to accumulation. Moreover, this hysteresis is larger on sample B, indicating a larger concentration of charges or traps in the oxide or at the interface.

Afanas'ev *et al.* showed that the neutrality level of carbon clusters is energetically aligned with the conduction band of 3*C*-SiC [31]. Therefore, only donor-like states (carbon clusters or dangling bonds) are present at the SiO_2/3*C*-SiC interface in the gap of 3*C*. Donor-like states are positively charged when empty, resulting in a stored positive charge. The larger initial negative shift of the flat band voltage can be explained by the presence of positively charged carbon clusters or dangling bonds at the interface, and the smaller shift observed going back from depletion to accumulation suggest that a charge neutralization has occurred through electron injection from the semiconductor. The hysteresis remains even after the initial sweep, indicating that it is related to oxide defects located sufficiently close to the interface to be able to trap charges from the semiconductor and to emit them back into the semiconductor. Similar behavior has previously been related to slow near-interface traps at the SiO_2/3*C*-SiC interface [8].

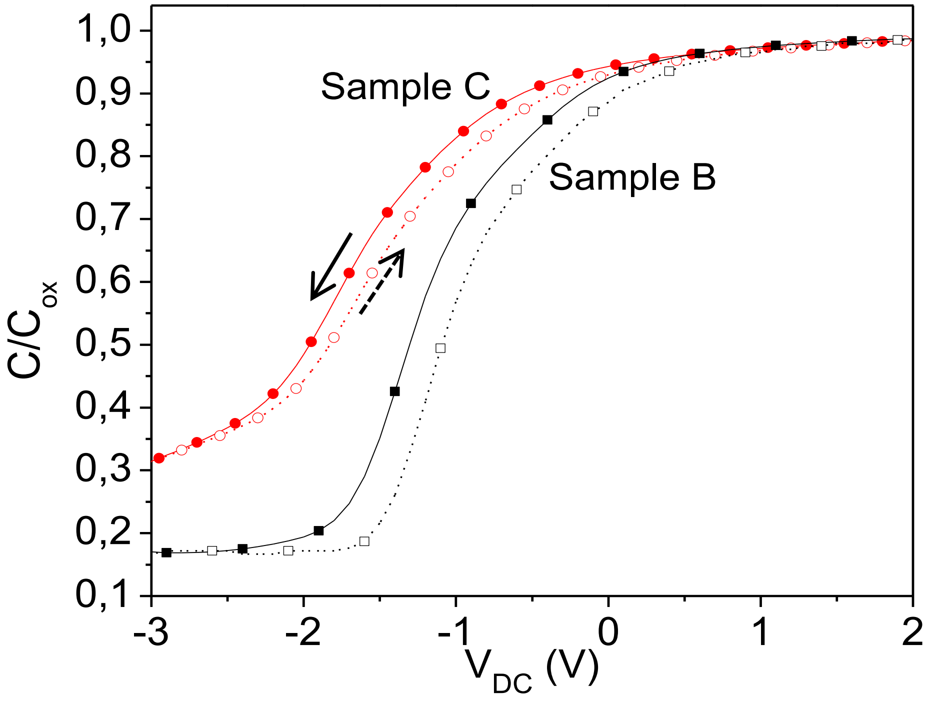

Figure 12. ***C-V*** **characteristics for sample B and sample C, measured on MOS structures comprising circular Au contacts with a radius of 150 µm. The larger hysteresis between the different sweep-directions measured on Sample B can be ascribed to a larger concentration of trapping centers.**

The density of the charges that are trapped upon the DC bias sweep can be calculated from the change in the flatband voltage shifts in Fig. 12, according to [7,32]:

$$N_q = \frac{Q}{q} = \frac{C_{ox} \times \Delta V_{FB}}{q} \ (\mathrm{cm}^{-2}) \qquad (5)$$

where N_q is the effective oxide charge density, Q is the total charge reduction, q is the elementary charge, C_{ox} the oxide capacitance and ΔV_{FB} the reduction of the flatband voltage observed between the different sweep directions. The N_q values were determined from *C-V* characteristics measured on five different capacitors on each sample, and the average values are $N_q = 5.9 \times 10^{11}$ cm^{-2} for sample B and $N_q = 4.3 \times$

10^{11} cm^{-2} for sample C. The larger value for sample B is consistent with the higher degree of interface roughness, in turn expected to result in a larger density of interface states. The effective oxide charge densities for both samples are comparatively high with respect to the findings of Esteve *et al*. [7], who subjected SiO_2 deposited by plasma enhanced chemical vapor deposition to post oxidation in wet O_2. Hence, it can be inferred that the higher charge densities in our thermal oxide is related to the generation of carbon clusters during the thermal growth of the SiO_2.

In order to monitor the presence of localized charge density variations in the oxide layer and at the interface, the dC/dV behavior of the SiO_2/3*C*-SiC system for samples B and C was studied by scanning capacitance spectroscopy (SCS). The characteristics were obtained sweeping the bias voltage first from accumulation to inversion, and then back to accumulation. Thus, the localized charging and discharging of electronic states in the oxide or at the interface can be evaluated from the dC/dV curves. A typical curve measured on sample C is shown in Fig. 13. The flatband voltage was evaluated from the position of the peak in the dC/dV curves. It should be pointed out that the position of the flatband voltage is different in Fig. 13 compared to Fig. 12, which is related to the different contact material. Indeed, the Si tip is coated by heavily boron-doped diamond, which has a different extraction potential than gold. This means that the nano-MOS has a different theoretical flatband voltage, and the data cannot be directly compared with the values obtained in the micro-MOS with a gold metal gate.

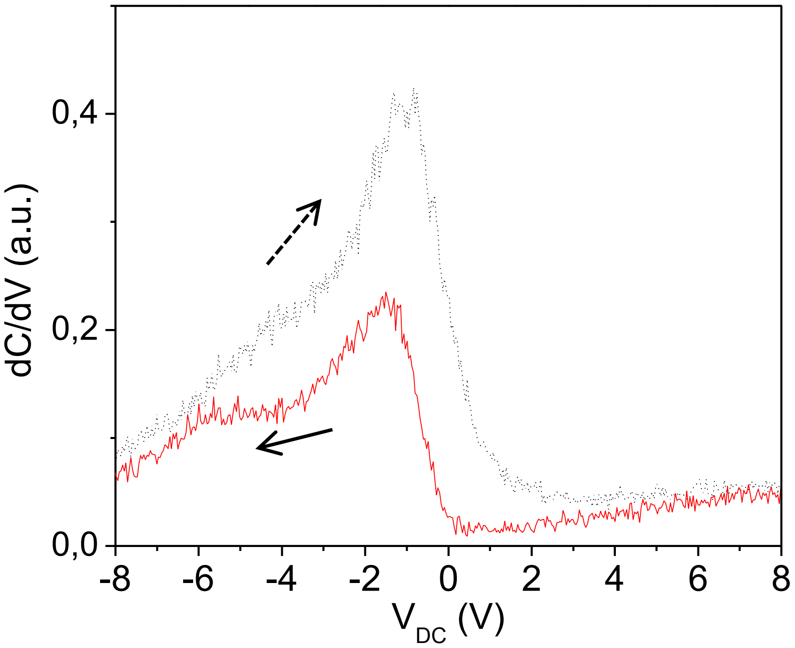

Figure 13. ***dC/dV*** **characteristics of a nano-MOS device formed between the SCM tip and the SiO2/3*C*-SiC system on sample C.**

The effective oxide charge densities were determined from *dC*/*dV* characteristics measured at 25 different tip positions, separated by 500 nm over a total area of 2.5 × 2.5 μm^2. The distributions of charge densities for samples B and C are presented in Fig. 14. The average densities are 6.1 × 10^{11} cm^{-2} for sample B and 4.5 × 10^{11} cm^{-2} for sample C, which is very close to the results obtained from *C*-*V* measurements, where the total area is much larger (by more than seven orders of magnitude) and should reflect the average behavior of many nano-MOS devices.

However, as can be seen in Fig. 14, large variations in the N_q values of individual nano-devices are observed at both interfaces, and spots of high charge density resulting from these variations can explain the aforementioned extrinsic BD population that could not be attributed to morphological features. As can be seen, the lateral variations in N_q are decidedly larger for sample B (FWHM of 1.8 × 10^{11} cm^{-2})

than for sample C (FWHM of 1.1 × 10^{11} cm^{-2}). This is also consistent with the larger *E*/*I* ratio reported in Table 1.

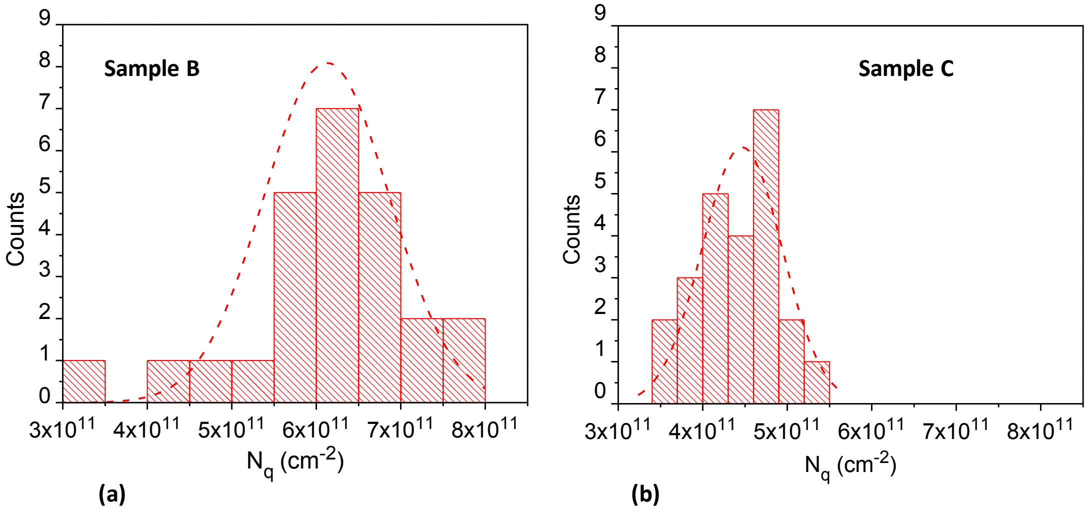

Figure 14. Localized variations in the effective charge densities on sample B (a) and sample C (b). The values were extracted from the *dC/dV* characteristics measured at 25 different tip locations by moving the SCM tip in 500 nm steps over an area of 2.5 × 2.5 μm^2.

The trapped charges can affect the BD generation in two ways; 1: they may contribute to the formation of a percolation path and, 2: the addition of charges during the electrical stressing may cause a concentration of the electric field, leading to a faster accumulation of additional charges in the oxide layer due to enhanced Fowler-Nordheim tunneling. Consequently, the extrinsic BD population observed in the oxide grown on a surface free from BD-generating morphological features can be attributed to these charges. Recent work has shown that the effective oxide charge density at the SiO_2/3*C*-SiC interface can be reduced to 1.7 × 10^{11} cm^{-2} with an adapted oxidation process comprising deposition of SiO_2 by plasma enhanced chemical vapor deposition and post oxidation in wet O_2 [7]. Adopting such a process could significantly reduce the charge-induced premature dielectric BD at SiO_2/3*C*-SiC interfaces.

4.6 Conclusion

The causes of premature dielectric BD in thin SiO_2 layers, thermally grown onto 3*C*-SiC (111), was investigated by locally stressing the dielectric at high electric field strength using C-AFM. The cumulative failure ratio as a function of stress time can be divided into two distinct regions: failure due to pre-existing defects or process-induced weak spots at low stress times, and failure due to intrinsic dielectric breakdown at higher stress times. The breakdown kinetics was evaluated by fitting the experimentally observed failure ratios as a function of stress time to the failure probability described by Weibull statistics. As the 3*C*-SiC surface roughness was reduced from 16.1 nm to 0.2 nm, the congruence between the extrinsic and intrinsic BD kinetics increased from 26.3 % to 62.7 %, indicating that the oxide reliability is greatly improved.

A preferential BD generation was observed in the vicinity of step-bunching edges, which is attributed to a local electric field concentration on top of these defects. However, an extrinsic BD population remains even when the oxide was grown on a smooth 3*C*-SiC surface where the only abundant type of defect is the stacking fault. No correlation could be found between the location of the BD spots and the stacking faults. In the absence of BD acceleration related to morphological features at the SiO_2/3*C*-SiC interface, the premature failure is attributed to an enhanced percolation path formation due electron injection into traps while the SiO_2/3*C*-SiC system is kept in accumulation. The *C*-*V* characteristics of the fabricated MOS capacitors showed high densities of effective oxide charge, likely related to interface traps and slow near interface traps. Scanning capacitance spectroscopy further demonstrated significant nanoscale lateral variations in the trapped charge density, which could ultimately explain the observed premature BD in the absence of BD caused by structural defects at the interface.

4.7 Rerefences

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Conclusion and outlook

In this thesis, some critical scientific issues related to the electronic transport at 3*C*-SiC interfaces were investigated. The transport properties of metal/3*C*-SiC interfaces and SiO_2/3*C*-SiC interfaces were monitored employing a nanoscale characterization approach, in combination with conventional electrical measurements.

The role of the crystalline quality in the properties of Ohmic contacts to 3*C*-SiC was investigated by studying the structural and electrical evolution of Ni-based contacts to high-quality 3*C*-SiC, heteroepitaxially grown on α-SiC and free from double positioning boundary (DPB) defects. By increasing the annealing temperature from 600°C to 950°C, a nickel silicide phase evolution and gradual improvements in the structural homogeneity of the contacts were observed by XRD. Indeed, the mechanism of good Ohmic contact formation in a Ni/SiC system is normally attributed to an interface reaction upon annealing, resulting in the formation of nickel silicide. This, in turn, results in the formation of carbon clusters in the semiconductor near the interface, leaving vacancies which act as electron donors for SiC. The presence of these carbon vacancies near the interface increases the net carrier concentration under the contact and reduces the contact resistance. However, a nanoscale electrical characterization approach allowed the visualization of a new aspect concerning the mechanism of good contact formation in Ni-based Ohmic contacts to SiC. Specifically, an increased uniformity of the nanoscale current distribution on the contacts was demonstrated with increasing annealing temperature. This, in turn, indicates that an increase of the effective contact area contributes to the improvement of the contact properties normally observed for Ni-based contacts to SiC upon annealing in the temperature range 600°C to 950°C.

After the gradual improvements in the structural and electrical homogeneities, a low specific contact resistance of 1.5×10^{-5} Ωcm^2 was obtained. In light of the high roughness and the relatively low doping of the grown layer, the low experimental value of the specific contact resistance hints towards very high crystal quality of the single-domain 3*C*-SiC film grown by the VLS mechanism. Indeed, equally low values of the specific contact resistance for Ni-based contacts to 3*C*-SiC, grown by other techniques, have only been obtained for contacts deposited on material with much lower surface roughness and much higher doping concentrations.

The biggest limitation for device fabrication in 3*C*-SiC, though, is related to difficulties with achieving good rectifying contacts, with acceptable blocking behavior. This has been attributed to the electrical activity of defects in the 3*C*-SiC epilayers and at the heterointerfaces.

DPB defects and triangular pits were identified as 'killers' for rectifying contacts to 3*C*-SiC. However, a structural analysis performed by TEM, coupled with an electrical characterization of the semiconductor surface by C-AFM, showed that stacking faults (SFs) are normally the predominant type of extended defect that can affect the contact properties on these epilayers. Current mapping of the 3*C*-SiC surface showed that these defects form preferential paths for local detrimental leakage currents, in turn causing a reduction of the Schottky barrier height determined from *I-V* measurements to below 0.8 eV for the Au/3*C*-SiC interfaces in this study.

C-AFM current mapping also demonstrated that a UV-irradiation treatment electrically passivates SFs that have a C-termination at the 3*C*-SiC surface. This passivation was shown to arise from a healing of C-terminated SFs due to a preferential oxidation occurring locally inside these defects. After the passivation of the SFs, the Schottky barrier height gradually increased with decreasing contact area, ultimately leading to a nearly ideal value of the barrier height for the Au/3*C*-SiC interface (1.39 eV) for diodes with a small contact area. However, the contact area dependence of the Schottky barrier height found after this passivation indicates that other defects and/or inhomogeneities at the contact interface still remain electrically active. The derivation of a semi-empirical model to describe the experimentally measured barrier heights as a function of the contact area allowed demonstrating the key role of point-like defects in the properties of the barriers on 3*C*-SiC. The nature of these defects could be related either to semiconductor surface states or inhomogeneities at the Au/3*C*-SiC contact interface.

The contact area dependence of Φ_B was absent for the Pt/3*C*-SiC system, which also showed improved electrical properties with respect to the Au/3*C*-SiC system. This was attributed to a more homogeneous metal/semiconductor interface. Annealing of Pt/3*C*-SiC at 500°C resulted in further reduction of the leakage current and an increase of the Schottky barrier height, whereas annealing at higher temperatures (700°C and 900°C) led to a degradation of the Schottky characteristics. The evolution of the electrical properties was related to the formation of platinum silicides and ultimately to changes in the density of states at the contact interface upon annealing. The reaction at 500°C consumes a thin layer of SiC, moving the contact interface away from the original semiconductor surface states, thereby removing their role in the electrical behavior of the contact. The degradation observed at higher annealing temperatures occurs due to increased carbon clustering at the contact interface, in turn increasing the carrier concentration in the semiconductor near the interface.

Consequently, it is clear that surface preparations and interface reactions are key issues for the formation of good rectifying contacts to 3*C*-SiC. From the results obtained in this thesis, the conclusion is that a passivation of C-terminated SFs at the surface by UV irradiation prior to metallization, coupled with contact formation through a metal/3*C*-SiC interface reaction occurring at moderate temperature to avoid carbon clustering, is the best approach to achieve good Schottky contacts to 3*C*-SiC.

The SiO_2/3*C*-SiC interface is interesting for the potential fabrication of high frequency power MOSFETs, an application where 3*C*-SiC, due to its intrinsic material properties, should perform better than any other SiC polytype. However, MOS structures utilizing the SiO_2/3*C*-SiC interface usually suffer from premature, non-ideal dielectric breakdown (BD). No satisfactory explanation exists to fully describe the mechanisms of premature oxide breakdown in SiO_2/SiC structures. Moreover, the statistical gate oxide reliability and the mechanisms of breakdown generation had never been addressed specifically for the 3*C*-SiC/SiO_2 interface. Therefore, the causes of premature dielectric breakdown in thin SiO_2 layers, thermally grown onto 3*C*-SiC (111) layers of different surface quality, were investigated by locally stressing the dielectric at high electric field strength using C-AFM, which forms a nano-MOS capacitor at each tip position.

A strong correlation was found between the oxide reliability and the 3*C*-SiC surface roughness prior to oxidation. As the 3*C*-SiC surface roughness was reduced from 16.1 nm to 0.2 nm, the congruence between the premature and the ideal BD kinetics increased from 26.3 % to 62.7 %.

Moreover, a preferential BD generation was demonstrated to occur in the vicinity of step-bunching edges, which was attributed to a local electric field concentration on top of these defects due to the abrupt change in height. However, a premature BD population was observed even when the oxide was grown on an atomically flat 3*C*-SiC surface where the only abundant type of defect was the stacking fault, which was found to not accelerate the BD. In this latter case, the premature failure was attributed to an enhanced percolation path formation due charges that are trapped while the SiO_2/3*C*-SiC system is kept in accumulation. Indeed, high densities of effective oxide charge with significant nanoscale lateral variations were demonstrated by a combination of *C*-*V* characterization and scanning capacitance spectroscopy.

The findings reported in this thesis clarified some previous scientific issues concerning Ohmic and rectifying metal-semiconductor interfaces in 3*C*-SiC, as well as the causes of premature breakdown often observed in SiO_2/SiC MOS structures. At the same time, they have also given rise to some new open points in need of scientific study.

For the future, it would be interesting to study how the passivation of stacking faults by UV irradiation affects the electrical behavior of these pervasive defects at *p*-*n* junctions. Indeed, since one of the most promising potential devices for this polytype is a MOSFET, the defect-related degradation at *p*-*n* junctions is more critical than that at Schottky junctions. Another continuation of that topic would be to optimize the reaction to form the Pt_2Si/3*C*-SiC contacts. In this study the best Schottky behavior was observed upon annealing of Pt contacts at 500°C, but C-AFM current mapping of the contact showed low barrier patches covering 12% of the contact area.

On the topic of premature oxide breakdown, the reliability of gate oxides should be investigated for an oxide grown and post-oxidized under optimized conditions, which would remove the main causes for premature breakdown identified in this thesis. Moreover, the study should be conducted using oxides with a thickness ($\geq$ 50 nm) needed for real MOSFET applications.

Lastly, β-α SiC heterojunction structures open up interesting possible applications, such as devices based on a two-dimensional electron gas (2DEG) at the heterointerface or dual wavelength optoelectronic utilizing the different optical properties of cubic and hexagonal SiC. The fabrication of a high electron mobility transistor based on the 2DEG requires a very smooth β-α SiC interface. Recent advances achieved both in CVD and VLS growth of 3*C*-SiC onto 4*H*-SiC should render this particular issue an interesting possibility. Concerning dual-wavelength optoelectronic devices, high Schottky barriers and low leakage currents are essential for achieving high optical sensitivity. The improvement of both these parameters demonstrated in this thesis shows the possibility to fabricate such devices.

Curriculum vitae

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Jens Eriksson was born in Västervik, Sweden. He has Master of Science in Electrical Engineering, specializing in Electronic Design (received in 2005), and a Bachelor of Science in Physics (received in 2006) from the Institute of Technology at Linköping University, Sweden. After receiving his degrees he joined the Swedish Sensor Centre (S-SENCE) and worked on the development of chemical sensors based on MOS structures and the characterization of sensing layers for applications in gas and liquid phase. In September 2007, he joined the Institute for Microsystems and Microelectronics of the Italian National Council of Research (CNR-IMM) in Catania, Italy, as a Marie Curie early stage researcher within the Research and Training network MANSiC. His work within this network focused on transport properties at 3*C*-SiC interfaces, which resulted in this thesis and his improved patience. The work performed for his thesis has led to 12 journal publications, and during the PhD he attended six international conferences, giving four poster presentations and five oral presentations.

Conferences

- European conference on silicon carbide and related materials (ECSCRM'08), Barcelona, Spain, September 2008. Contribution: Poster presentation
- HeteroSiC/WASMPE'09, Catania, Italy, May 2009. Contribution: One oral and one poster presentation
- International conference on silicon carbide and related materials (ICSCRM'09), Nuremberg, Germany, October 2009. Contribution: One oral and one poster presentation

- Workshop on compound semiconductor devices and integrated circuits held in Europe (WOCSDICE'10), Darmstadt/Seeheim, Germany, May 2010. Contribution: Oral presentation
- European materials research society spring meeting (EMRS spring '10), Strasbourg, France, June 2010. Contribution: One oral and one poster presentation

- European conference on silicon carbide and related materials (ECSCRM'10), Oslo, Norway, August 29th – September 2nd, 2010. Contribution: Oral presentation

Publications

1. *"Improved Ni/3C-SiC contacts by effective contact area and conductivity increases at the nanoscale*", J. Eriksson, F. Roccaforte, F. Giannazzo, R. LoNigro, V. Raineri, J. Lorenzzi, and G. Ferro, Appl. Phys. Lett. **94**, 112104 (2009)

2. *"Nano-Electro-Structural Evolution of Ni-Si Ohmic Contacts to 3C-SiC",* J. Eriksson, F. Roccaforte, F. Giannazzo, R. LoNigro, G. Moschetti, V. Raineri, J. Lorenzzi, and G. Ferro, Mater. Sci. Forum **615-617,** 569 (2009)

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